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K450B LOGIC ANALYZER
SERVICE MANUAL

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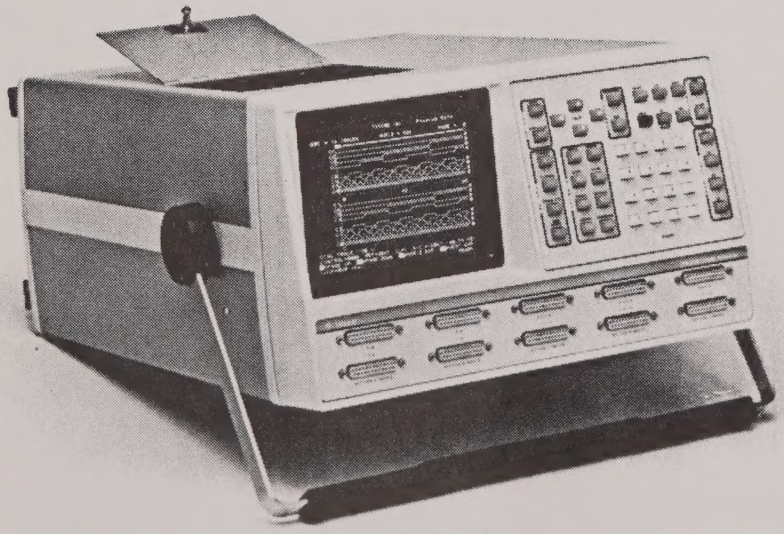

K450B Logic Analyzer with Single Disk Storage

PREFACE

This manual contains information for servicing and maintaining the Gould K450B Logic Analyzer. Procedures are provided for making adjustments and calibrating the control circuits for various functions. These procedures include the use of diagnostic tests to troubleshoot and isolate a malfunction to a circuit component. Theory of operation is presented for printed circuit board functions. Service aids in the form of schematic diagrams, wiring diagrams, assembly drawings, cable connection diagrams and parts lists are included for user reference.

The material in this manual reflects the Control Firmware level valid on July 15, 1987. This information is up-to-date at the time of publication, but is subject to change without notice.

Copies of this publication and other Gould Inc., Design and Test Systems Division Publications may be obtained from the Gould Inc., DTD sales office or distributor serving your locality.

RELATED PUBLICATIONS

The following support documentation may be used with this manual:

> K450B Logic Analyzer User's Manual, Publication Number 0121-0460-10. This manual describes the capabilities, functions, and operation of the K450B Logic Analyzer.

ASSISTANCE

If you require assistance on this product, please call Gould Inc., Design and Test Systems Division Customer Service on the toll-free, hot-line number listed below:

Telephone (800) 538-9320

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Chapter 1

GENERAL DESCRIPTION

INTRODUCTION

Overview of K450B Features

The Gould K450B Logic Analyzer (Figure 1-1) is a precision, high-performance test and development instrument, that monitors and records digital signals from the user's target system.

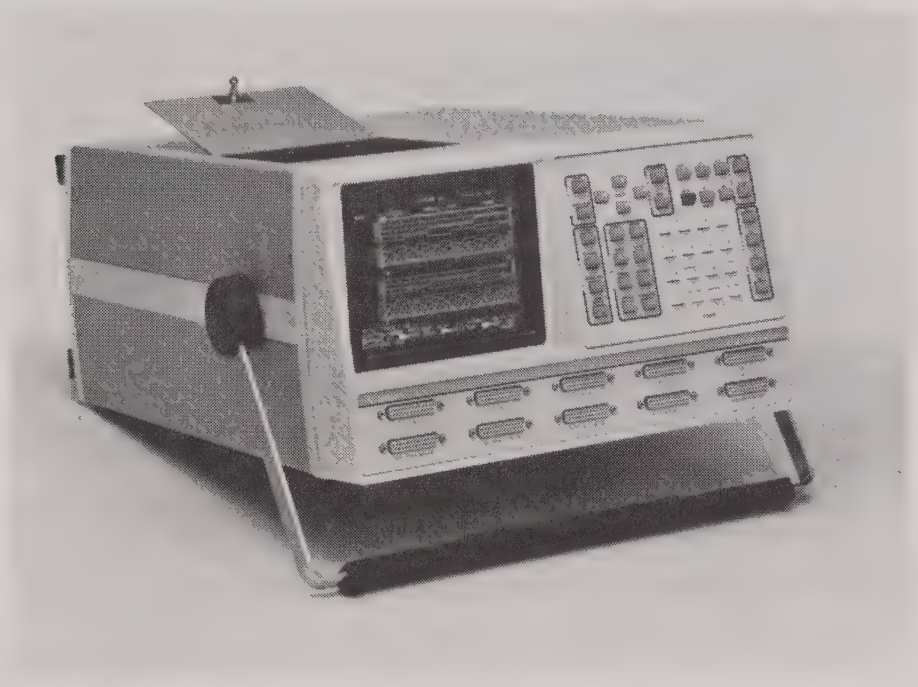


Figure 1-1. K450B Logic Analyzer, General Arrangement

The K450B may be configured to accept the following data inputs:

32, 64 or 80 Inputs @ 100 MHZ, Sections A/B, C/D and E.

16, 32, or 40 Inputs @ 200 MHz, Sections A/B, C/D and E.

The K450B also accepts the following external clock inputs:

2 Sample and 2 Latch clocks, Section A only.

6 Sample and 2 Latch clocks, Section A and B.

6 Sample and 6 Latch clocks, Sections A, B, and C.
(Clock inputs are not provided for Sections D and E)

The K450B control logic measures input signals to correlate data and timing characteristics. The K450B captures and compares data samples. The results are then recorded in memory. The features are menu-driven by resident firmware which is controlled by the Keyboard Panel. The menus allow the user to set up test conditions and capture the results of binary logic states through trace control for data-domain analysis. The pulse train waveforms are displayed for time-domain analysis. The display screen presents the results of analysis for examination and /or modification by the user.

Major Features of the K450B operation are:

- The K450B equipment functions are menu-driven under the control of a 16-bit, 8086 microprocessor.
- The operating system accommodates up to 512K bytes of RAM and 256K bytes of ROM.
- Five input sections, A, B, C, D and E provide 80 channels to accept user inputs through probe circuits. Each section is subdivided into two input groups. Each input group at sections A, B, and C accept 8 data and 2 clock signals to provide 48 data inputs and 12 external clocks. Each input group at sections D and E accept 8 data signals to provide 32 data inputs.
- Data inputs are capable of being sampled internally at frequency rates up to 200 MHz. Data may be displayed in 40-column Binary format, or in Hexadecimal, Octal, ASCII, EBCDIC, or user defined formats.
- Sample, Glitch, and Latch/Demultiplex input modes are selected in groups of 8 or 16 channels.
- Independent threshold-level selection is provided for each logic probe Section and associated group of clocks.
- Up to 16 different state levels for trace control are selected by using the display menus and front panel keys.
- The K450B tracks a 50MHz state machine, while comparing the machine state to four search patterns per level, every 20 ns.
- The trace is recorded in a 48-bit wide x 2051-word length memory.
- A 24-hour Real Time clock with battery backup feature allows the K450B to log the current time of day and date of each recording.
- The battery backup feature also drives the CMOS memory which preserves the current set up for recording parameters if power is interrupted.
- A self-contained frequency counter provides automatic measurement of external clock frequency and status.
- The K450B may be operated as a stand-alone unit or interfaced with the user's CPU system or peripherals through a RS-232-C or IEEE-488 communications link.
- An optional Disk Storage System (DSS) provides two disk drives with 312K bytes per disk to store set up information and data for later analysis. The DSS option replaces the single disk drive.

Overview of Manual Contents

The manual is arranged as follows:

Chapter 1. GENERAL DESCRIPTION - Presents an overview of the K450B operating features, organization of manual contents, service plan, maintenance features, and equipment specifications.

Chapter 2. SYSTEM COMPONENTS AND INTERCONNECTIONS - Describes the interconnection of printed circuit boards, power distribution, external I/O interface and special tools and test equipment.

Chapter 3. CALIBRATION AND POWER UP DIAGNOSTICS - Describes the power up Boot PROM check, Probe Test, calibration of the Data Display Board, Clock Board, Threshold/GPIB/RS-232 Board, and adjustment of power supply voltages.

Chapter 4. THEORY OF OPERATION - Presents theory of operation for each printed circuit board and associated circuitry.

Chapter 5. DISK DIAGNOSTICS - Describes each diagnostic module and its associated subtests.

Chapter 6 OPTIONS INSTALLATION - Provides procedures for installing the Input Expansion Option for C, D and E section inputs and the Dual Disk Storage System Option equipment

Chapter 7. SCHEMATICS AND DRAWINGS - Provides reference material such as schematic diagrams, assembly drawings, and parts lists.

SERVICE PLAN

The service plan for the K450B involves the use of diagnostic routines to isolate a defective circuit function for the repair or replacement of components at the user's site. The K450B has firmware diagnostic routines that perform a check of major circuit functions whenever the unit is reset or powered up from a cold start. Malfunctions detected by the diagnostics may be tested further by using the Disk Diagnostic routines to isolate the cause of failure.

The resident firmware also generates special displays which permit the user to conduct input Probe Tests and perform CRT alignment. The diagnostic should be rerun after a repair is completed to verify the problem is resolved before the unit is placed into operation.

The use of any diagnostic for troubleshooting does not eliminate the need for user interaction to visually inspect cable connections, ensure printed curcuit boards are seated properly and ensure calibration adjustments are made within prescribed limits.

Power Up Diagnostic Routines

The Power Up Diagnostic routines indicate system operational status. Messages are displayed on the screen to identify the type of error condition and the failed function. Since several interactive components may be associated with the malfunction, board swapping and re-running the diagnostic may fix the problem. To avoid possible damage to equipment, do not remove or install a printed circuit board while Vac or Vdc power is applied to the unit.

The following circuits are tested by the Power Up Diagnostic routines:

- MPU Board RAM Test
- MPU Board ROM Test
- Keyboard Matrix Test For Stuck Keys
- System Voltage Tolerance Test
- Display Board CMOS RAM Test
- Threshold/GPIB/RS-232 Board Check
- DSS Recognition Check
- Data Board Recognition Check
- Clock Board Recognition Check
- Control Board Recognition Check

Disk Storage System Diagnostic Routines

The K450B Disk Storage System (DSS) loads diagnostic routines from the disk to further isolate the cause of failure to a specific circuit or component. The DSS diagnostic provides flexibility for the user to set up test parameters that halt on error, loop on error and perform repetitive tests for a specified pass count. The DSS diagnostic is described in Chapter 5.

A separate diagnostic routine is provided for each component. The diagnostic does not assume any part of the system is functional until it has passed its associated subtests. If a failure is detected, the diagnostic generates an error message identifying the cause of failure. A Self Test menu is displayed when the DSS diagnostic is invoked.

The following software is contained on the diagnostic disk:

- Diagnostic/Operating System (K450B)
- Keyboard/Display Diagnostic Module (KDDIAG)
- Threshold/GPIB/RS-232 Board Diagnostic Module (THDIAG)
- Control Board Diagnostic Module (CBDIAG)
- Clock Board Diagnostic Module (CKDIAG)
- Data Board Diagnostic Module (DBDIAG)
- Storage Controller Board Diagnostic Module (SCDIAG)

When the user selects a test for execution, the diagnostic test monitor generates detailed sub-menus that direct the user in running the test procedure.

MAINTENANCE FEATURES

In addition to the power up diagnostics firmware, the K450B contains additional built-in features that aid in maintaining the equipment. These features, also driven by resident firmware, allow the user to test the sample and clock inputs at each probe and to align the CRT display characteristics. An overview of these features is presented in paragraphs that follow.

Probe Test

Two Probe Test connectors, located on the back panel, allow the user to verify that two clock inputs and eight data inputs supplied from each probe, operate within acceptable limits. A test pattern generated by the K450B firmware is supplied to the probe under test. Procedures for conducting the Probe Test are described in Chapter 3.

Display Calibration Pattern

Procedures for calibrating the CRT are described in Chapter 3. The Display Calibration Pattern, is accessed by pressing and holding the SHIFT key while powering up the unit. This pattern allows the user to make adjustments on the Data Display board for calibrating the following display characteristics:

- Video Contrast/Drive
- Brightness
- Horizontal/Range Hold
- Horizontal Scan Width
- Focus

SPECIFICATIONS

K450B Unit Configurations

Model #	Description
132:	Provides inputs for 32 data signals @ 100 MHz (16 data signals @ 200 MHz) and 8 clocks via input Section A/B.
164:	Provides inputs for 64 data signals @100MHz (32 data signals @ 200 MHz) and 12 clocks via input Sections A/B and C/D.
180:	Provides inputs for 80 data signals @ 100 MHz (40 data signals @ 200 MHz) and 12 clocks via input Sections A/B, C/D and E.
Expansion Option:	Each data board has probe inputs for 16 or 32 add-on data signals @ 100 MHz (8 or 16 data signals @ 200 MHz) via input Section C/D (32) or E (16).
DSS Option:	Dual Disk Storage System provides two 5 1/4" floppy disk drives mounted in an add-on assembly unit which provides 312K bytes of storage per disk. This unit replaces the standard single disk drive.

Power Requirements

Input Frequency:	50 or 60 Hz
Input Volts:	90 to 135 Vac or 180 to 270 Vac
Input Power:	500 Watts without DSS option or 550 Watts with DSS option

Fuses/Rated Voltage:

Voltage Range	Fuse
90 Vac to 135 Vac	3AG,6 AMP
180 Vac to 270 Vac	3AG, 3 AMP

Physical Dimensions and Weight

Height:	8.6 inches(21.8 Cm), 12 inches (30.1 Cm) with Dual Disk DSS
Width:	17.5 inches (44.5 Cm)
Depth:	24.7 inches (62.7 Cm) including handle
Weight:	45 lbs. (20 Kg) without probes 8.5 oz (240 gms) per probe 15.0 lbs (6.75kg) for Dual Disk DSS

Environmental Limits

Ambient Temp:	39 to 115 Deg.F (4 to 46 Deg.C) OPERATING 8 to 117 Deg.F (-20 to 50 Deg.C) STORAGE
Relative Humidity:	20% to 80% OPERATING 1% to 95% STORAGE
Max Wet Bulb:	78 Deg.F (25 Deg.C) OPERATING No condensation STORAGE

Signal Outputs

VIDEO, BNC:	One Vp-p into 75 ohms composite video output is available with 60 Hz vertical, 19.2 KHz horizontal (416 x 290 pixel) refresh.
CLOCK, BNC:	ECL active low corresponds to the internal clock
GET, BNC:	Group Execute Trigger pulse output, TTL, for IEEE-488
TRACE BNC:	TTL high output when trace is enabled
+5VDC:	+5V and -5.2V @ 300 mA Auxiliary Power

I/O Interfaces

One RS-232-C Serial I/OPort configured as Data Terminal Equipment. One Auxiliary Serial I/O Port for RS-232

One IEEE-488 Bus Interface, I/O Parallel Port

Features

Clock:	A 24-hour, time and date clock is backed up by a 2.9V battery
Back-up Memory:	CMOS Memory, driven by battery, which saves the setup of recording parameters if power is interrupted or when the unit is turned off

Probe

Input Resistance:	1 megohm referenced to threshold
Input Capacitance:	<=6pF (<=15pF with flying leads) input resistance may approach 500K ohms at voltages exceeding ±15 volts from threshold.
Max Input:	±50 volts, peak
Bandwidth to 90% V Out:	= > 100MHz
Min Swing for Output:	Threshold ± 0.20 V maximum
Threshold Variance:	±15 mV maximum, between input signals, ±30 mV maximum any two probes
Input Comp:	Even to 20% overcompensated
Thresholds:	Thresholds are independently selectable for each section and the clock group

TTL, +1.4 volts
ECL, -1.3 volts
VAR A and VAR B

Variable thresholds may be set from -9.99 to +9.99 volts in 0.01 volt Increments. Accuracy of all threshold voltages is 30mV.

Polarity:	+ or - is selectable for each signal

Chapter 2

SYSTEM COMPONENTS AND INTERCONNECTIONS

INTRODUCTION

This chapter describes individual printed circuit boards and components that comprise the K450B Logic Analyzer. Information is also included for the interconnection of these boards and recommended test equipment. Front and rear views of the K450B chassis are shown in Figures 2-1 and 2-2.

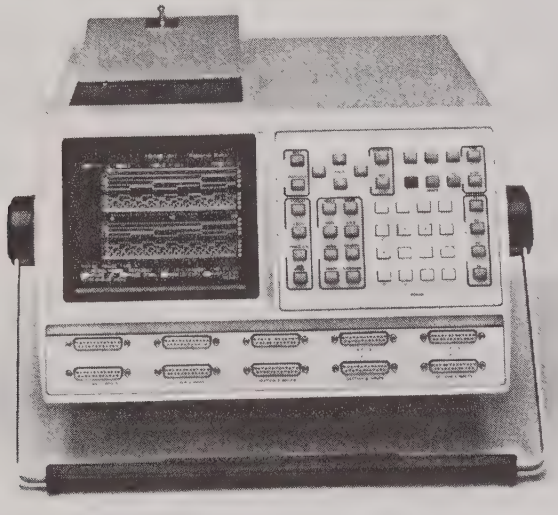


Figure 2-1. K450B Front Panel Arrangement

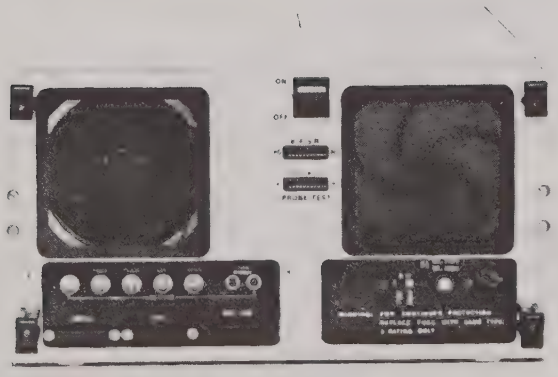


Figure 2-2. K450B Rear Panel Arrangement

BOARDS AND COMPONENTS

The Following boards and components are used for K450B hardware configurations:

- Keyboard:

  The keyboard has 48 keys; several keys can be shifted to perform a secondary function. Because of the shift capability, 20 keys can perform as a full alpha-numeric keyboard.

- Front Connector Panel:

  The front connector panel has the following components:

  -Ten DB-25 female connectors for external data/clock input

  -Power LED indicator which also indicates the presence of the +5 Vdc when Vac power is applied.

  -The data/clock input connectors available for 32, 64, or 80 input configuration are established by the number of Data Boards installed. The unit may be configured with one, two or three Data Boards respectively to provide 32, 64, or 80 data inputs. The Configuration Display screen indicates the number of active connectors present for a given instrument.

- Display Assembly:

  The display assembly has a 8-inch P31 CRT and a CRT deflection yoke with cable harness. The mounting bracket for the assembly is an integral part of the CRT glass envelope.

- Rear Casting Assembly:

  The rear casting assembly has the following components;

  -Vac Power Switch

  -Two card-edge female connectors for probe test output

  -Two fan assemblies and connector panels

- Rear Connector Panel:

  The rear connector panel provides external interface for signal I/O and power through the following circuit components:

  -Signal output is provided for VIDEO, CLOCK, TRACE, and GET through four BNC connectors

  -The + 5Vdc and -5Vdc output is provided by each of two LEMO connectors

  -Signal I/O is provided by one IEEE-488 connector and two RS-232 connectors. One RS-232 connector is labeled AUX and is intended for the future options.

  -Power Interface is provided by the 115V/230 Vac line voltage input socket and the line voltage select switch (for 115V/230Vac). The power fuse is rated at 6 Amp, 3AG for 115 Vac or 3 Amp, 3AG for 230 Vac power input.

- Power Supply:

  The power supply provides the following regulated outputs, each of which can be adjusted as described in chapter 3:

  +5.1Vdc at 11 Amps

-5.35Vdc at 36 Amps

-15Vdc at 0.2 Amps

+15Vdc at 3.0Amps

-2.14Vdc at 17Amps

Socket pins for measuring these voltages are located on the solder-side of the Mother Board on the bottom of the chassis. The access points for adjusting these voltage levels are also located on the bottom of the chassis.

- Data Board:

The Data Board Assembly interfaces probes to the high speed memory and Control Board. The Data Board processes up to 32 inputs. Either one, two or three Data Boards will be installed in a given system configuration as determined by the 32, 64 or 80-channel input configuration. The Data Board main memory (M) is 2,048 bits deep by 32 bits wide and gathers data at up to 200 MHz.

- MPU Board:

The MPU Board Assembly contains the 8086 microprocessor and operates as the controller for K450B operations. The firmware resides in ROM located on the MPU Board. The MPU Board operates with a clock frequency set to control the fast vertical scan rate for CRT components, A jumper at location on J1 is placed across pins 2 and 3 to select the 60Hz clock rate.

- Control Board:

The Control Board Assembly provides 16 trace levels to be programmed by the user. A selection of qualifiers enables the user to pick and choose the information that will be recorded. The Control Board also provides an output signal to the rear panel TRACE BNC connector.

- Threshold/GPIB/RS-232 Board:

-The Threshold/GPIB/RS-232 Board Assembly provides fixed and variable threshold voltages for the probe pods. This board provides two RS-232 ports and one IEEE-488 Talker/Listener port. This board also contains adjustments for threshold voltages and provides an output signal to the rear panel GET BNC connector.

- Data Display Board:

The Data Display Board Assembly contains the keyboard scanning circuitry and the horizontal, vertical and high-voltage circuitry for the CRT. In addition, this board contains interface connectors for two 5 1/4 -inch floppy disk drives and the Keyboard Assembly. This board provides a video composite signal (19.23 KHz frequency) to the rear of the panel VIDEO BNC connector. Adjustments for brightness, linearity, etc, are located on the CRT driver, Piggyback Board Assembly. Adjustment for Focus is located on the CRT Satellite Board which is plugged into the CRT input connector.

- Clock Board:

The Clock Board Assembly processes the external clocks from the probes and provides a range of internal clocks for the system. This board also provides an output signal to the CLOCK BNC connector and a test pattern signal to the two PROBE TEST sockets on the rear panel.

BOARD AND COMPONENT INTERCONNECTIONS

Boards

The K450B printed circuit boards are contained in an eight-slot card cage, and are interconnected through a mother board. Interconnection of the printed circuit boards to the front and rear connector panels is provided by flat cables that mate to connectors located along the upper edges of the board. See Figure 2-3 for the system interface.

Components

The K450B is a compact unit and the cable harness to the mother board and Data Display Board are short. The mother board is connected to the keyboard by a short, flat cable.

The optional Disk Storage System (DSS) has two disk drives and a disk controller interface board. The DSS I/O signal interface is provided by a flat cable that mates to a connector (P4) located on the Data Display Board. The power supply harness interfaces to a harness connector located on the base of the chassis. All interface cables required for the DSS installation are included with the DSS kit.

CARD CAGE ARRANGEMENT

The K450B card cage arrangement is shown in Figure 2-4. The Board ejector tabs on each printed circuit board are numbered to correspond to the assigned slot location in the card cage.

Data Board Configurations

Three Data Boards reside in slot locations A2, A3, and A4. The ejector tabs are not numbered on these boards. Two of the boards (for slot locations A3 and A4) are identical and accept 32 inputs each. The remaining data board (for slot location A2) is configured to accept 16 inputs and is not interchangeable with Data Boards at slots A3 and A4.

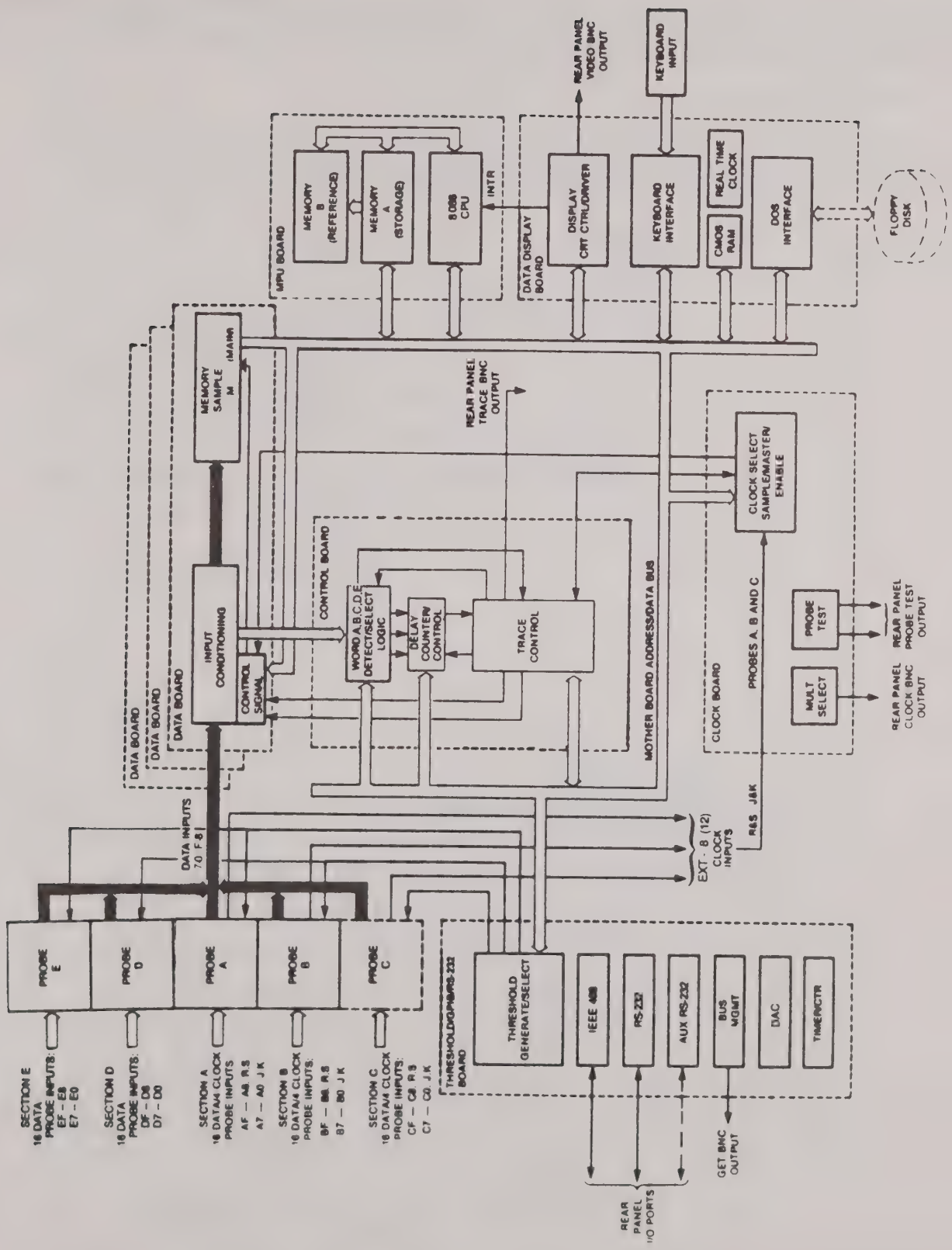


Figure 2-3. K450B System Interface of Components to Mother Board

The K450B configured for 32 inputs (Section A and B) use one data board installed in slot A4. An instrument configured for 64 data inputs (Sections A, B, C, and D) uses two data boards installed in slot locations A4 and A3. Instruments configured for 80 data inputs (Section A, B, C, D, and E) uses an additional data board installed in slot location A2.

Board Calibration Controls

The Data Display Board, Threshold/GPIB/RS-232 Board and Clock Board have controls for calibrating various circuit functions. The location of these controls is shown in Figure 2-4. The procedure for performing the calibration adjustments is described in Chapter 3. The following circuit functions are adjusted by these controls:

CARD CAGE LOCATION	BOARD NAME	CIRCUIT FUNCTION ADJUSTMENT
A8	Data Display (Piggy Back)	VR 101 Vertical Size (pot.) VR 103 Video Contrast/Drive (pot.) VR 105 Brightness (pot.) VR 106 Horizontal/Range Hold (pot.) L101 Horizontal Scan Width (Coil) R56, Audio Alarm Volume (pot.)
	CRT Satellite (CRT Connector)	VR 200 Focus (pot.)
A6	Threshold/GPIB/RS-232	R1,R2, Variable B Threshold R3, R5, ADC Voltage R6, R9, Variable A Threshold R7, ECL Threshold R8, TTL Threshold R44, Reference Voltage (+ 10V)
A5	Clock	R19, C8 100 MHz Clock (Oscillator Circuit)

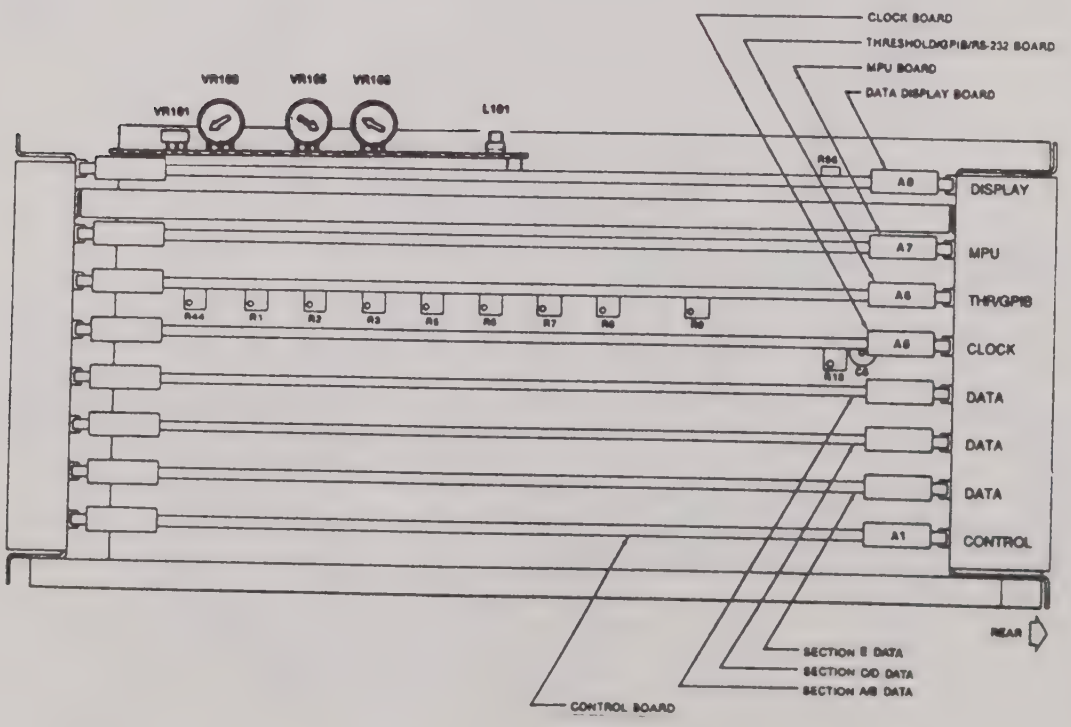


Figure 2-4. K450B Card Cage Arrangement

SUGGESTED TEST EQUIPMENT

The following is a list of the suggested test equipment for servicing the K450B Logic Analyzer:

ITEM	DESCRIPTION
Extender Board	Gould Part Number 0117-0195-01
Digital Multi-meter	4 1/2 Digits, Vdc Accuracy of +/- (0.03% of reading + 2 digits)
Frequency Counter	Capable of 0.01% accuracy on ECL at 100MHz
Oscilloscope	350 MHz band width, Horizontal Resolution to 1 ns/DIV
Logic Analyzer	Any current Gould Production model
20-Pin, 0.3" IC Clip	Standard
3 Mini Clips/Grabbers	Standard
4.7K-Ohm, 1/4 W, 5% Resister	Standard
Ball Chart Overlay	Gould Part Number 0113-0017

Chapter 3

CALIBRATION AND POWER UP DIAGNOSTICS

GENERAL

This chapter describes the K450B Power Up diagnostic test routines and procedures for calibrating system components. This information is organized as follows:

- Power Up Diagnostic
- Probe Test
- Display Calibration
- Power Supply Voltage Adjustments
- Threshold Voltage Calibration
- ADC Circuit Calibration
- Internal Clock Adjustment

POWER UP DIAGNOSTIC

The Power Up Diagnostic test verifies the readiness of hardware components whenever the K450B is powered up from a cold start or restarted. The power up diagnostic is implemented by a resident program in the EPROM firmware located on the MPU printed circuit board.

Diagnostic Operation

As soon as the AC POWER switch is turned ON, the K405B beeps and executes the diagnostic test routines. As each test is completed, the next test is run. When all tests are successfully completed, the Configuration screen displays the current hardware configuration. The K450B is ready to accept user inputs.

The power up diagnostic is also initiated when the SHIFT and DEFAULT keys are pressed to reset system operations. The power up diagnostic runs for approximately ten seconds to check certain components and perform a series of tests. The following tests and checks are performed by the power up diagnostics:

- Microprocessor RAM Test
- Microprocessor ROM Checksum Test
- Keyboard Stuck Key Test
- System Voltage Test
- Display Board CMOS RAM Test
- Threshold/GPIB/RS-232 Board Recognition Check
- DOS Recognition Check
- Data Board Recognition Check
- Clock Board Recognition Check
- Control Board Recognition Check

User Interaction

If an error is detected in any of the tests, the name of the failed test is displayed and testing is stopped. To run the remaining power up tests, or to attempt operation of the instrument despite the error condition, press the NEXT key to resume testing. Press the PREVIOUS key to repeat the test. After the last test is executed, the Configuration screen is displayed. Since an error was detected, the disk-based diagnostic test is used to further isolate the cause of the error.

As each power up diagnostic test is executed, the name of the test is displayed on the CRT. If the test is run successfully, PASSED is printed after the test name. The first failure in a test is indicated by FAILED, which is printed after the test name. A test-results header is then printed on the next line and the results of the test are printed on subsequent lines. Any more failures causes the results to be printed on successive lines.

Microprocessor RAM Test Description

The microprocessor RAM Test is executed by writing and reading bits in a test pattern as follows:

1. Write 0000 to address locations 0000-FFFF.
2. Read 0000 from address locations FFFF-0000 and write FFFF at each location.
3. Read FFFF from address locations 0000-FFFF and write 0000 at each location.
4. Read 0000 from address locations 0000-FFFF and write FFFF at each location.
5. Read FFFF from address locations FFFF-0000 and write 0000 at each location.

This test is repeated, changing the segment registers so that RAM address locations 0:0000 to 7000:FFFF are all tested. If all test patterns are read back successfully, the following is displayed:

MICROPROCESSOR RAM TEST - PASSED

If any bits fail, the following is displayed:

MICROPROCESSOR RAM TEST- FAILED

MPU MEMORY FAILURE

MAP OF RAMS ON MPU BOARD (G = GOOD, X = BAD)

COL-->	4	6
ROW ↓		
A	G	X
B	G	G
C	G	G
D	G	G
E	G	X
F	G	G
G	G	G
H	G	G

Please press NEXT to continue. PREV to repeat.

Where: COL and ROW positions correspond to the RAM socket locations on MPU board.

Microprocessor ROM Checksum Test Description

The ROM Checksum Test computes 16-bit checksums for each of the ROMs which are numbered from 1 to 10. The computed checksum values are then compared with the expected values which are stored in the top of ROMs 1 and 2. If the values match, the test is successful and the system proceeds to the next test.

If the values do not match, the error display indicates the ROM numbers, the expected checksum value, and the actual checksum value. Note that a missing ROM generates the following:

ROM CHECKSUM TEST- FAILED

ROM NUMBER	EXPECTED CHECKSUM	ACTUAL CHECKSUM
2	463B	ALL "FF"

Keyboard Stuck Key Test Description

This test performs a check of the keyboard matrix for stuck keys.

If one or more keys are stuck, the affected key(s) is displayed below the test failed message, in a matrix that is continuously updated.

If all keys were stuck, the following information is displayed on the CRT screen:

KEYBOARD STUCK KEY TEST- FAILED

NE	^	>	CN	SH	IO	ED	AR
PR	<	v	RF	HL	SP	IN	ST
FO	MA	MB	C	D	E	F	F1
CL	DA	AB	8	9	A	B	F2
TR	TI	SE	4	5	6	7	F3
AM	GR	CM	0	1	2	3	F4

When all the keys are unstuck, the test is successful and the system goes to the next test.

Voltage Test Description

The following voltages are checked by the power up diagnostics:

+15.00 Vdc
-15.00 Vdc
-10.00 Vdc
+ 5.04 Vdc
- 5.28 Vdc
- 2.08 Vdc
VBATT

Tolerance for the +15V test is +0.5 Vdc. The tolerances for remaining voltages have been set to +/- 10%. The testing sequence is as follows:

1. The +15V test is repeated up to 100 times. If the voltage returned is not within the tolerance limit on or before test 100 occurs, the test has failed.

2. If the +15V test is successful, remaining voltages are tested. A failed condition occurs if any of the voltages are not within acceptable limits.

3. For each voltage that fails, the following is displayed on the CRT:

- Name of voltage being tested
- The minimum voltage limit
- The maximum voltage limit
- Measured voltage value (average and peak-to-peak) which was read.

Display Board CMOS RAM Test Description

The CMOS RAM is backed up by batteries to store setup parameters for recording information. This test compares stored data with a stored checksum value. A failure displays an error message:

CMOS RAM TEST FAILED

An error indicates the K450B will not restore the recording setup parameters nor correctly save new parameters. The error does not always indicate a component has failed. The source of failure could be a soft error. Pressing the NEXT key resumes the diagnostic. If the original error was not caused by a component failure, the CMOS RAM TEST ERROR will not appear on the next power up and CMOS memory will operate correctly.

PROBE TEST

The rear panel connectors, labeled PROBE TEST, are used to check the probe circuitry. The test is performed on eight sample data input signals of each probe and continuity for J and K clock input using the external clock set-up.

NOTE: The integrity of clocks are not checked by this test.

Probe Test Pattern Generator

The Probe Test Pattern Generator is always enabled. The pattern generator circuits send an output signal to the PROBE TEST sockets consisting of a known ring-counter loop and clocking sequence. The pattern generator outputs two clock signals and eight data signals for each PROBE TEST socket. These signals are supplied as input to the probe tip. The clock and data signals output from the PROBE TEST sockets have a voltage swing from 0 to -5 volts.

Probe Connections

The two PROBE TEST sockets allow the low order (bits 7-0) probe and high order (bits F-8) probe of each input section to be tested concurrently. To avoid noise pulses at the other input sections, connect the probe cables to these input sections while conducting the probe test. Use the following procedure to connect the probe cables:

1. Connect the low order bit probe cable to lower front panel socket labeled SECTION A INPUTS (J, K, 7-0).

2. Connect the high order bit probe cable to upper front panel socket labeled SECTION A INPUTS (R, S, F-8).

3. Plug the lower order bit probe tip of SECTION A INPUT cable into the lower PROBE TEST socket. Ensure the label faces upward.

4. Plug the high order bit probe tip of SECTION A INPUT cable into the upper PROBE TEST socket. Ensure the label faces upward. See Figure 3-1 for A J external clock.

5. Repeat steps 1 and 2 to connect probe cables to front panel sockets at Section Inputs B and C.

6. To test Section D and E, use CJ as external clock (low-order probe) then move high-order bit probe to the section input to be tested.

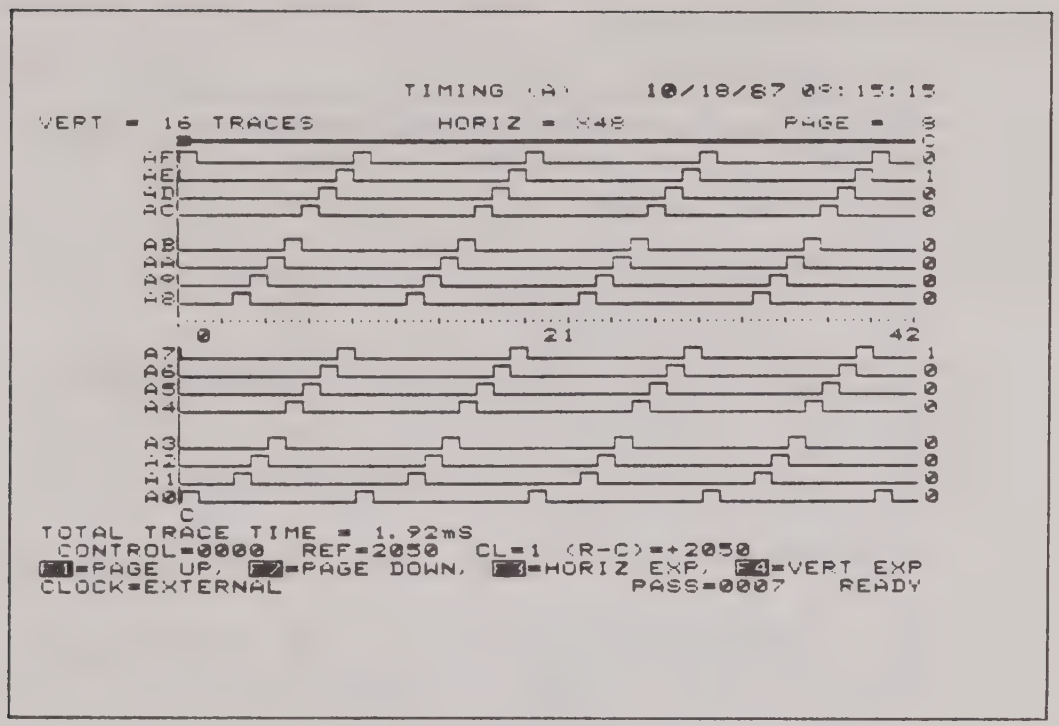


Figure 3-1. Typical Probe Test Recording Using An External Clock

Default Setup

The K450B has CMOS memory backed up by battery to retain the previous set-up parameters. Whenever the unit is powered up from a cold start, the previous set-up parameters are restored. It is necessary to initialize all set-up parameters to their default value as follows:

1. Press the SHIFT and ARM MODE/DEFAULT Keys to select the Configuration Screen.

2. Press the F1 Function key to select the Default Setup Parameters.

3. Watch for the following message at the top of the screen:

   Default Setup M and Display values locked in. . .

Fixed ECL Threshold Setup

1. Press the FORMAT key. Verify that the Format Display shows Data Inputs for AF through A0 and Threshold at TTL level.

2. Change the threshold for inputs AF through A0 to ECL moving the blinking cursor to the AF-A8 line of the Data Inputs display and change TTL to ECL as follows:

   a) Press the F1 Function key to select top of threshold.

   b) Press the FIELD down-arrow key four times to move the cursor downward to the AF-A8 line.

   c) Press 1 (numeric) key twice to change the entries to ECL level at lines AF-A8 and A7-A0.

Trace Control Setup

To setup the trace control, perform the following:

1. Press the TRACE CONTROL key.

2. Press the FIELD down-arrow cursor key once. Press the FIELD right-arrow cursor key twice.

3. Press the 2, 0, 5 and 0 numeric keys.

Record/Review Test Results

1. Press the ARM key to start a recording.

2. Watch the status message located in the lower right area of the screen. This status indicates a recording has occurred with the following condition:

   -READY ready for an ARM signal

   -BUSY Setup internally for a recording

   -EOR End of recording activity

   NOTE: The actual recording occurs quickly. Press the Timing key to view the display. Press the F1 key to scroll through the input displays until the input signals are shown on the screen.

3. Observe a staircase pattern of pulses (shown in Figure 3-2) appears on the screen. This pattern begins at any point on the screen as determined by the Default Setup. Memory is filled with samples starting at Location 0 in the data stream.

4. Use the Control and Reference cursors to measure the total trace time of 10 microseconds and pulse width of 0.9 microsecond. These conditions indicate the probes under test are properly accepting inputs for recording.

5. Verify a pulse is present for each channel. If no pulse occurs, reverse the upper and lower probes and repeat the test. A generator malfunction is isolated by swapping the probes. A probe malfunction is isolated by swapping the probe at the input connector. A failure means a problem with cabling or the Data Boards.

6. Repeat the Probe Test for inputs at Sections B, C, D, and E. Verify if these probes are accepting inputs for recording.

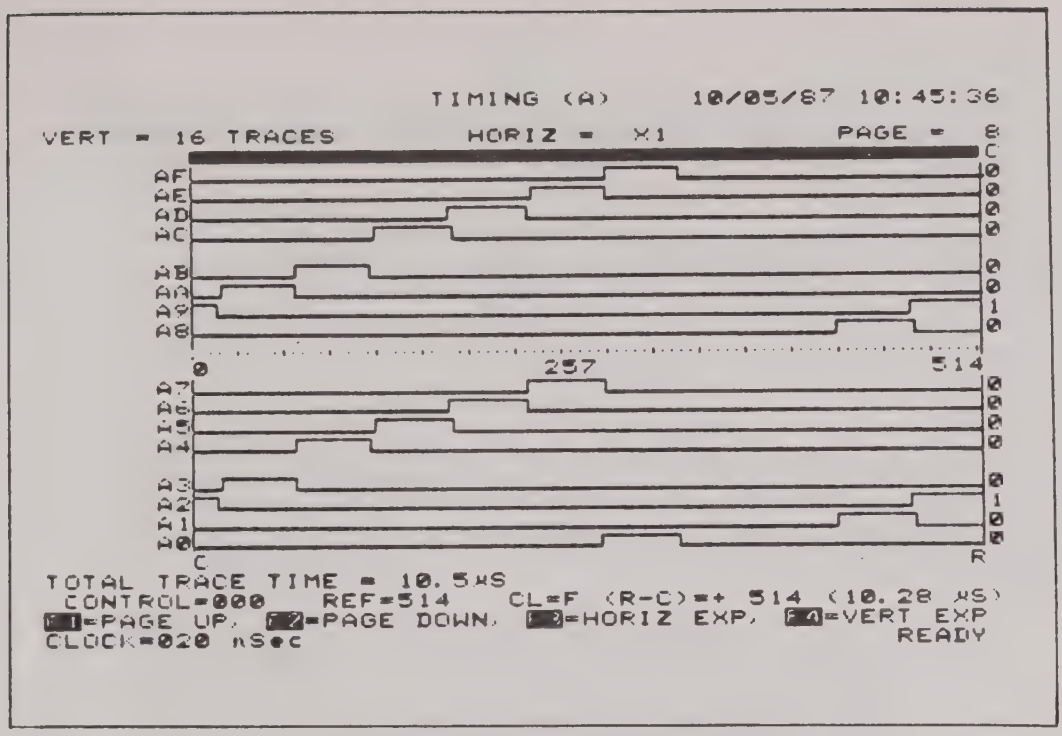


Figure 3-2. Typical Probe Test Recording Using Internal Clock

DISPLAY CALIBRATION

The Data Display Board circuitry performs the following functions:

- Generates signals that drive the CRT
- Reads the front panel Keyboard
- Controls priorities for interrupt levels
- Controls the Real Time Clock
- Drives the Audio Alarm

****

WARNING

Hazardous voltages dangerous to life are present on the Data Display board and CRT. Avoid body contact in these areas which could result in injury.

****

Calibration Requirements

Use extreme caution when calibrating the Data Display Board. The adjustment controls are located near an area where high voltages are generated for operating the CRT. Body contact with the printed circuit board and flyback transformer must be avoided. It is further cautioned to use non-metallic tools when making raster adjustments.

The display calibration consists of making adjustments for the following conditions:

Horizontal Range/Hold Adjustment

CRT Brightness and Video Contrast Drive Adjustment

CRT Alignment

These adjustments must be accomplished in sequence; e.g. The Horizontal adjustment must be completed before adjusting the CRT Brightness and Video Contrast/Drive. Likewise, the Brightness and Video contrast must be adjusted before doing the CRT Alignment.

Audio Tone and CRT Horizontal Adjustment

1. Turn power on and verify unit passes the power-up diagnostic test. Ensure the following message is presented on the screen:

   GOULD K450B LOGIC ANALYZER
   * * POWER UP DIAGNOSTICS COMPLETE * *

2. During power-up test, adjust R56 VOLUME pot. for good sound. Pressing an illegal key with the Error Beep on causes a brief tone to be generated. The Error Beep is turned on and off by accessing the Data screen and pressing the FIELD right-arrow and NEXT keys to select the Beep parameter.

3. Adjust VR106 HORIZONTAL RANGE/HOLD pot. (Figure 3-3) to lock in the picture. Adjust screen so the vertical dots that make up each character are straight. Ensure there are no problems with the characters displayed at the far left and right-hand side of the display. To do this, press the TIMING, F3 and EDIT keys and view the entire screen.

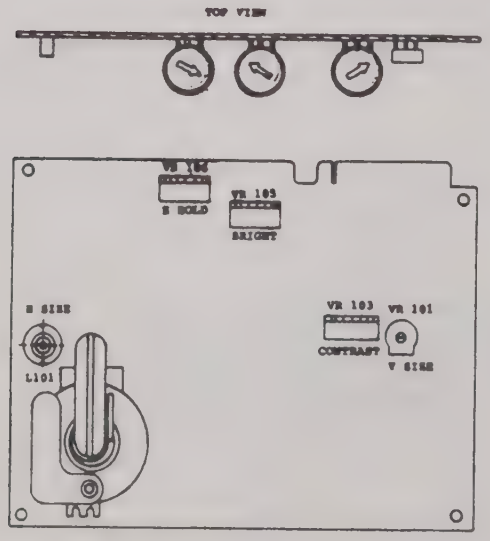


Figure 3-3. Data Display Board Adjustment Points

CAUTION

The K450B power supply is synchronized to operate with the 60 Hz display frequency voltage and may become damaged if the 50 Hz frequency is selected on the MPU board.

4. If the HORIZONTAL RANGE/HOLD adjustment does not lock in the picture (i.e. tearing of the picture results), check that the 50Hz/60Hz vertical scan select shorting-plug jumpers are installed properly on both the MPU board and Data Display Board for 60 Hz operation. Ensure the Synchronization cable from the power supply to the data display board is connected securely. This cable connection prevents power supply switching noise from appearing in the display.

CRT Brightness and Video Contrast/Drive Adjustment

1. Press the SHIFT, DEFAULT and F3 (system screen) keys. Position cursor over the CRT Brightness field, and press the up-arrow cursor key until full CRT intensity is obtained.

2. Turn the VR103 VIDEO CONTRAST pot. fully counterclockwise initially. Adjust the VR105 BRIGHTNESS pot. until the raster lines just begin to disappear. No raster nor retrace lines should be visible.

3. Verify the operation of the keyboard controlled brightness control function by using the down-arrow cursor key. Holding the key down will lower the CRT brightness level. Pressing and holding the up-arrow cursor key increases the brightness.

4. Turn the unit off and then on again. Verify the CRT intensity is at the same level it was before the unit was turned off.

5. Probe the video signal at the J3 interconnect cable, pin 8, with a scope. Set the minimum peak-to-peak video amplitude level to 1.2Vp-p when the down-arrow cursor key is held down for the minimum brightness level. Use the VR103 VIDEO CONTRAST pot. to set the amplitude to 1.2Vp-p.

CRT Alignment

1. Decrease the horizontal width of picture by adjusting the tuning slug L101, HORIZONTAL SCAN WIDTH coil inward approximately 1/8 inch. Use a non-metallic adjustment tool for this purpose.

2. Turn off power to the unit. Display the CRT Alignment Screen by holding down the SHIFT key while turning on the power. A grid pattern (Figure 3-4) will appear on the screen. Use the centering rings on the deflection yoke (Figure 3-5) to center the grid pattern on the screen. Use the Ball Chart Overlay (Figure 3-6) with display filter retainer to secure the overlay to the screen.

3. Re-adjust the screen centering position by rotating the L101 HORIZONTAL SCAN WIDTH COIL as necessary to obtain the size requirements. Adjust the vertical size of the picture by adjusting the VR101 VERTICAL HEIGHT pot. using the non-metallic adjustment tool.

4. Adjust the VR200 FOCUS pot. on the CRT Satellite board to the approximate setting indicated in Figure 3-7. Characters in the corners of the display and in the center of the screen should be as sharp as possible. Use the Timing screen with EDIT on to adjust the focus.

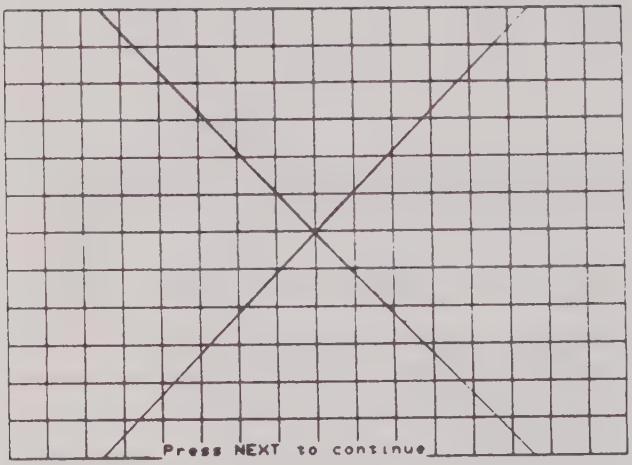


Figure 3-4 CRT Alignment Screen

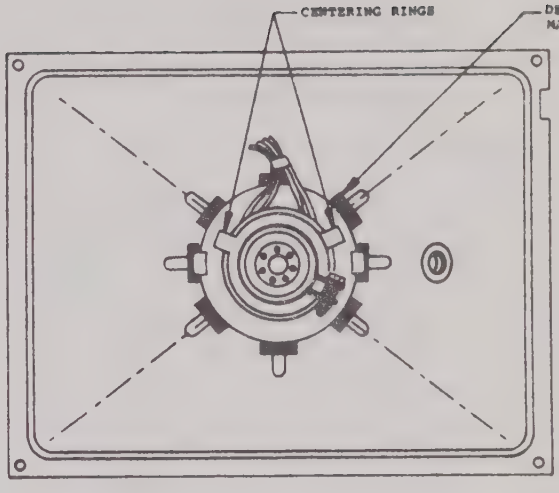


Figure 3-5 CRT Centering Rings

5. Rotate the magnets on the posts around the collar of the deflection yoke to adjust out the horizontal non-linearity caused by the power supply being located in close proximity to the CRT. Use care while rotating the magnets to avoid touching the deflection yoke wire terminals.

6. Verify the alignment is acceptable in accordance with the Ball Chart Overlay in conjunction with the built-in CRT alignment grid pattern. The intersections of the CRT grid lines must be aligned within the balls (donuts) in the Ball Chart Overlay as the screen is viewed head-on. This alignment condition provides the 2% linearity requirement.

7. If the alignment is not acceptable, repeat the steps as necessary to obtain the correct alignment. Carefully glue the magnets in place around the yoke, being careful not to move any of the magnets while applying the glue.

8. Verify the VIDEO output signal at rear panel BNC connector is present as follows:

   a. Connect a 50-ohm coaxial cable from the Composite Video Out BNC connector to one input of scope.

   b. Use 1-Megohm input scope termination and set scope for 1 volt/division and trace centerline (ground).

   c. Verify approximately 1.6V pp pulse occurs every 52 usec.

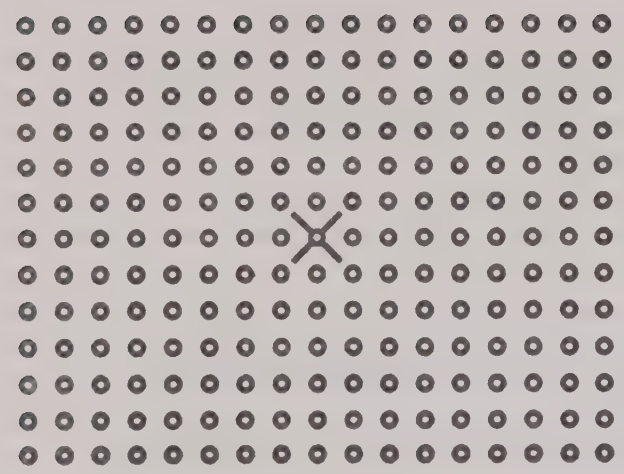


Figure 3-6. Ball Chart Overlay

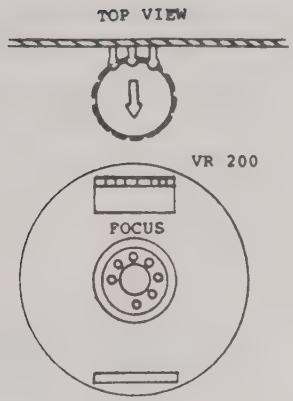


Figure 3-7. CRT Satellite Board Focus Adjustment

POWER SUPPLY VOLTAGE MEASUREMENT

A voltage measurement check is conducted to determined if the power is functioning properly. If the measured voltages are not within the specified limits, the power supply must be adjusted as described in the next paragraph.

NOTE: **The power supply must be allowed to warm up for at least 10 minutes prior to checking the supply voltages. All probes should be installed on the front panel for loading.**

Voltages are measured at pins on sockets J22 and J23 located on the solder-side of the Mother board, Figures 3-8 and 3-9. Access to the solder-side of the Mother board is obtained by removing the bottom cover from the chassis. The measurement is taken between the specified voltage signal and its respective return using an external DVM. The measured voltages must be within the following ranges:

NOMINAL VOLTAGE	RANGE LOW		HIGH
+15.00V	+14.40	to	+15.60
+5.00V	+4.48	to	+5.24
-2.00V	-2.16	to	-1.90
-5.24V	-5.48	to	-5.00
-15.00V	-15.60	to	-14.40

POWER SUPPLY VOLTAGE ADJUSTMENT

The power supply voltage is to be adjusted whenever the measured voltage levels are not within the specified range. The adjustment potentionmeters are accessible externally from the bottom of the chassis when the lower chassis cover is removed. It is mandatory that the power supply is operated under full load with all the probes connected to the unit when making the adjustments. Pin locations on the solder side of the Mother board for sockets J23 and J22 are shown in Figures 3-8 and 3-9 respectively. The following procedures describe the sequence for adjusting individual voltage levels.

-5.35 Volt Adjustment

To adjust the -5.35V power supply output;, connect a digital voltmeter (DVM) to pins on the Mother board as follows:

1. Connect the ground lead of the DVM to the -5.35V Return pin at socket J22 (choice of five pin locations available at pins 12, 14, 16, 18 and 20).

2. Connect the positive lead of the DVM to the -5.35V pin at socket J22 (choice of five pin locations available at pins 11, 13, 15, 17 and 19).

3. Adjust the -5.35V potentiometer to obtain -5.35 volts +/- 100mv.

-2.14 Volt Adjustment

To adjust the -2.14V power supply output, connect a DVM to pins on the Mother board as follows:

1. Connect the ground lead of the DVM to the -2.14V Return pin at socket J22 (choice of three pin locations available at pins 6, 8 and 10).

2. Connect the positive lead of the DVM to the -2.14V pin at socket J22 (choice of three pin locations available at pins 5, 7 and 9).

3. Adjust the -2.14 potentiometer to obtain -2.14 volts +/- 50mv.

+5.10 Volt Adjustment

To adjust the +5.10V power supply output, connect a DVM to pins on the Mother board as follows:

1. Connect the ground lead of the DVM to the +5.10V Return pin at socket J23 (choice of four pin locations available at pins 4, 6, 8 and 10).

2. Connect the positive lead of the DVM to the +5.10V pin at socket J23 (choice of four pin locations available at pins 3, 5, 7 and 9).

3. Adjust the +5.10 potentiometer to obtain +5.10 volts +/-100mv.

+15 Volt Adjustment

To adjust the +15V power supply output, connect a DVM to pins on the Mother board as follows:

1. Connect the ground lead of the DVM to the +15V Return pin at socket J22 (pin location 4).

2. Connect the positive lead of the DVM to the +15V pin at socket J22 (pin location 3).

3. Adjust the +15V potentiometer to obtain +15 volts +/- 300mv.

-15 Volt Adjustment

To adjust the -15V power supply output, connect a DVM to pins on the Mother board as follows:

1. Connect the ground lead of the DVM to the -15V Return pin at socket J22 (pin location 2).

2. Connect the positive lead of the DVM to the -15V pin at socket J22 (pin location 1).

3. Adjust the -15V potentiometer to obtain -15 volts +/- 300mv.

VOLTAGE LEVEL	MOTHERBOARD J23 PIN #
–	1
–	2
+5.10V	3
+5.10V RETURN	4
+5.10V	5
+5.10V RETURN	6

NOTE: **Refer to Mother board Schematic Diagram, Drawing Number 0121-0481 for arrangement of J23 pins.**

Figure 3-8. Mother board Pin Arrangement at Socket J23

VOLTAGE LEVEL	MOTHERBOARD J22 PIN#
-15V	1
-15V RETURN	2
+15V	3
+15V RETURN	4
-2.14V	5
-2.14V RETURN	6
-2.14V	7
-2.14V RETURN	8
-2.14V	9
-2.14V RETURN	10
-5.35V	11
-5.35V RETURN	12
-5.35V	13
-5.35V RETURN	14
-5.35V	15
-5.35V RETURN	16
-5.35V	17
-5.35V RETURN	18
-5.35V	19
-5.35V RETURN	20

NOTE: Refer to Mother board Schematic Diagram, Drawing Number 0121-0481 for arrangement of J22 pins

Figure 3-9. Mother board Pin Arrangement at Socket J22

THRESHOLD VOLTAGE AND ADC CALIBRATION

The following adjustments are made on the Threshold/GPIB/RS-232 Board:

- 10V Reference Voltage Adjustment
- TTL Threshold Adjustment
- ECL Threshold Adjustment
- Variable A Threshold Adjustment
- Variable B Threshold Adjustment
- ADC Adjustment

The location of potentiometers is shown in Figure 3-10. The following tools and test equipment is required:

o Extender Board:	Gould Part Number 0117-0195-01
o Digital Multimeter	4 1/2 Digits, Vdc accuracy of +/- (0.03% of Reading plus 2 digits)
o 4.7K-Ohm, 1/4 W, 5% Resistor:	Standard
o External voltage source of +/- 20.000 Vdc +/- 3mV	

Use the following procedures to make the adjustments:

NOTE:

To set proper values for Threshold adjustments, turn the K450B power off. Turn the power on to obtain the Configuration screen. Press F1 key to set default parameters. Press FORMAT key to get into Format Screen. Now pressing the F1 key moves the cursor to the top Threshold location on the screen.

10V Reference Voltage Adjustment

1. Turn power off, remove the Threshold/GPIB/RS-232 Board from card cage and install on an extender board.
2. Turn power on and verify unit passes power-up diagnostic test by displaying the Configuration screen.
3. Connect the external DVM reference (-) to the board A GND test point. Connect the DVM (+) input to the right side of resistor R38. See figure 3-10.
4. Adjust R44 for a DVM reading of +10.00 +/- 0.01V.

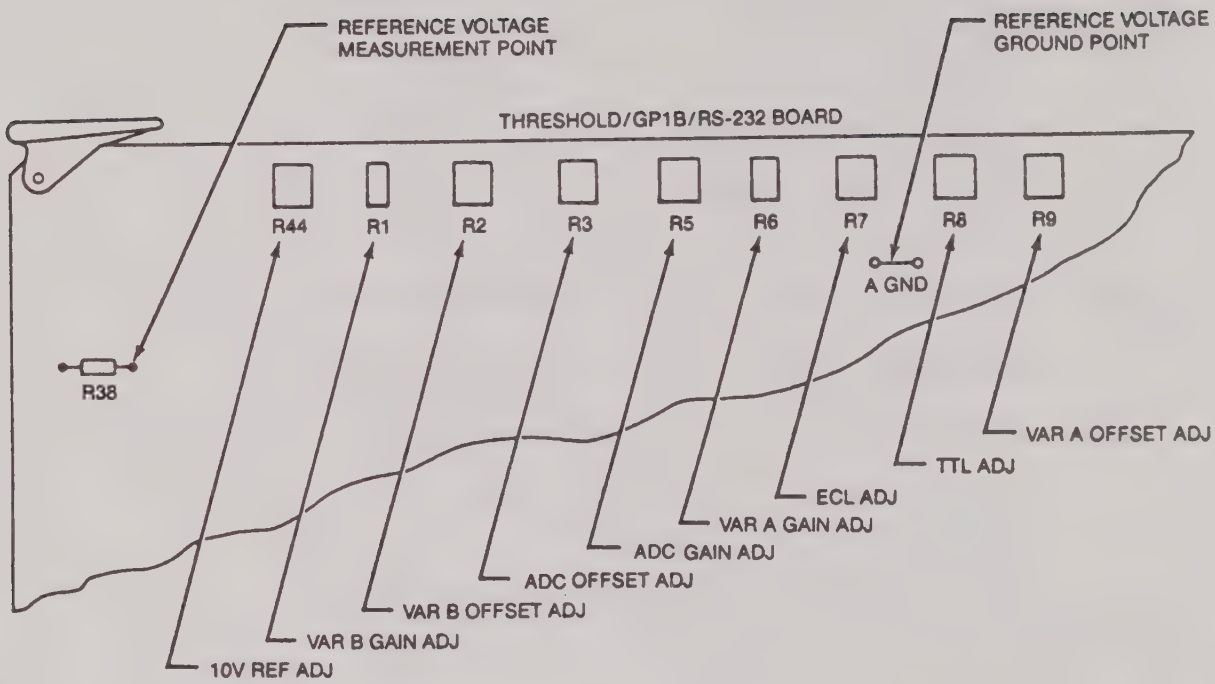


Figure 3-10. Threshold/GPIB/RS-232 Board Adjustments

TTL Threshold Adjustment

Remove all input cables from the unit. This procedure uses a 4.7K-Ohm resistor which serves as a load for adjustment of threshold voltages. All voltages are measured across the resistor. The TTL adjustment procedure also verifies that no shorts are present between High and Low inputs, and between Data and Clock inputs. The TTL adjustment is performed on each front panel input connector as follows:

1. Configure the K450B unit with three Data Boards to provide 16 inputs at each SECTION Input (A, B, C, D and E).

2. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 14 (Clock Threshold input) at SECTION A (bits 7-0). Connect the DVM positive (+) lead to socket 2 and the DVM negative (-) lead to socket 14 so that the voltage measurement is taken across the resistor. See Figure 3-11.

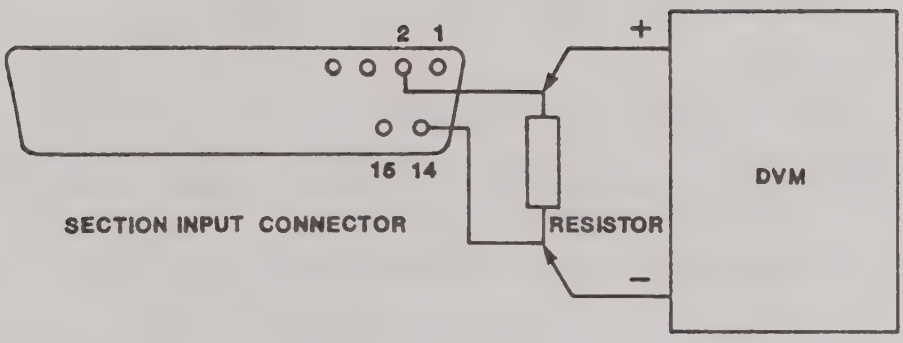


Figure 3-11. Test Connections for Threshold Voltage Adjustment

3. Press the FORMAT key and verify that all Thresholds are set to TTL.

4. Press the ARM key on keyboard.

5. Adjust the TTL THRESHOLD (R8) for a DVM reading of +1.400 +/- 25mV.

6. Relocate the resistor to SECTION A inputs (bits F-8) connector and verify the TTL Threshold of +1.400 +/- 5mV is present.

7. Check the TTL level of other inputs by moving the load resistor to input connectors at SECTIONs B, C, D and E. Verify the TTL Threshold of +1.400 +/-25mV is present at sockets 2 and 14 of each low-byte (bits 7-0) and high-byte (bits F-8) connector.

8. Install the 4.7K-Ohm resistor between sockets 2 and 15 (Data Threshold). Repeat steps 3 through 7.

9. Ensure no shorts are present between Low and High inputs, as well as between Data and Clock inputs by performing the following test:

   a. Press the FORMAT key to select the Format M screen. Press the F1 key to move cursor to top Threshold location. Press quick key 1, to change TTL level to ECL.

   b. Move the cursor down by pressing the FIELD down-arrow key once and press quick key 1 to change TTL level to ECL.

   c. Press the ARM key.

   d. Install the 4.7K-Ohm resistor between sockets 2 (ground) and 15 (Data Threshold) of SECTION C upper INPUT connector. Connect external DVM positive (+) lead to pin 2 and negative (-) lead to pin 15. Verify that the ECL Threshold of -1.300V +/- 25mV is present.

   e. Install the 4.7K-Ohm resistor between pin 2 and 14 of the same connector. Connect the DVM leads and verify that the TTL Threshold of +1.400V +/- 25mV is present. If the DVM reads ECL Threshold instead of TTL Threshold, this indicates a short is present between Data Input and Clock Input lines.

f. Install the resistor between pin 2 (ground) and 15 (Data Threshold) of SECTION C lower input connector. Connect the DVM leads and verify TTL Threshold of +1.400V +/-25mV is present. If the DVM reads ECL instead of TTL, this indicates a short is present between High and Low Data Input lines.

g. Repeat substep e for this connector.

h. Repeat substeps d through f for SECTIONs A, B, D, AND E.

ECL Threshold Adjustment

The ECL Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of SECTION A input connector (bits 7-0). Connect the DVM positive (+) lead to socket 2 and the DVM negative (-) lead to socket 14 so that the measurement is taken across the resistor.

2. Make the following keyboard entries to change all thresholds from TTL to ECL:

   a. Press the FORMAT key to access the Format screen.

   b. Press the F1 FUNCTION key, to move the cursor to the Top Threshold location.

   c. Press and hold quick Key 1 until ECL is selected for all threshold voltages

   d. Press the ARM key to change DVM reading to ECL level. Select ECL levels for all inputs.

3. Adjust the ECL THRESHOLD (R7) for DVM reading of 1.300 +/- 25mV.

4. Relocate the resistor to SECTION A (bits F-8) input connector and verify the ECL Threshold of 1.300 +/-5mV is present/

5. Check the ECL level of other inputs by moving the load resistor to input connectors at SECTION B, C, D AND E. Verify the ECL Threshold of 1.300 +/- 5mV is present at sockets 2 and 14 of each low byte (bits 7-0) and high byte (bits F-8) input connector.

Variable A Threshold Adjustment

The Variable A Threshold adjustment is performed for each front panel input connector as follows:

1. Install the 4.7K-Ohm resistor at sockets 2 and 14 of the SECTION A Input connector (bits 7-0). Connect the DVM positive (+) lead to socket 2. Connect the DVM negative (-) lead to socket 14 so the measurement is taken across the resistor. See Figure 3-11.

2. Make the following keyboard entries:

   a. Press the FORMAT key to access the Format screen.

   b. Press the FUNCTION key, F1, to move the cursor to the top threshold location.

   c. Press and hold quick Key 2 until VARA is selected for all threshold voltages.

   d. Press the ARM key to change DVM reading to VARA level. All inputs should read VARA = 9.99V.

3. Adjust the VARA GAIN (R6) for DVM reading of 9.990 +/- 5mV.

4. Make the following keyboard entries:

   a. Press the FIELD right-arrow key to move the cursor to 9.99.

   b. Press and hold Quick Key 0 until 9.99 inputs are set at 0.00.

c. Press the ARM key. All inputs should read VARA = 0.00V.

5. Adjust the VARA OFFSET (R9) for DVM reading of 0.00 +/- 5mV.

6. Make the following keyboard entries:

   a. Press and hold Quick Key 9 until 0.00 inputs are set at 9.99.

   b. Press the ARM key.

7. Adjust the VARA GAIN (R6) for DVM reading of 9.990 +/- 5mV.

8. Make the following keyboard entries:

   a. Press the FIELD left-arrow key to move cursor to the +position.

   b. Press the NEXT key to change positive (+) to negative (-) value.

   c. Press the ARM key.

9. Read the DVM and adjust the VARA GAIN (R6) for -9.99V + 1/2 the difference of actual reading and -9.99V. (For example, if the actual DVM reading is -9.98V, subtract this value from -9.99V. The difference of -0.01V is divided by 2 to obtain -0.005V and R6 would be adjusted for -9.995V.)

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages +/- 30mV.

Variable B Threshold Adjustment

The Variable B Threshold adjustment is performed for each front panel input connector. The procedures are the same as steps 1 through 10 for the Variable A adjustment, except as follows:

1. Install the 4.7K-Ohm resistor at SECTION A input connector as described in Variable A Threshold adjustment procedure.

2. Make the following keyboard entries:

   a. Press the FORMAT key to access the Format screen.

   b. Press the F1 FUNCTION key, to move the cursor to top of threshold.

   c. Press and hold Quick Key 3 until VARB is selected for all threshold voltages.

   d. Press the ARM key to change the DVM reading to the VARB level. All inputs should read VARB = 9.99.

3. Adjust the VARB GAIN (R1) for a DVM reading of 9.990 +/- 5mV.

4. Make the following keyboard entries:

   a. Press the FIELD right-arrow key twice to move the cursor to position 9.99.

   b. Press and hold Quick Key 0 until 9.99 inputs are set at 0.00.

   c. Press the ARM key. All inputs should read VARB =+0.00V.

5. Adjust the VARB OFFSET (R2) for a DVM reading of 0.000 +/-5mV.

6. Make the following keyboard entries:

   a. Press and hold Quick key 9 until 0.00 inputs are set at 9.99.

   b. Press the ARM key.

7. Adjust the VARB GAIN (R1) for a DVM reading of +9.990 +/- 5mV.

8. Make the following keyboard entries:

   a. Press the FIELD left-arrow key to move the cursor left to the (+) position.

   b. Press the NEXT key to change from a positive (+) to a negative (-) value.

   c. Press the ARM key.

9. Note the value of the DVM reading and adjust the VARB GAIN (R1) for -9.990V +1/2 the difference of actual reading and -9.990V.

10. Repeat steps 6 through 9 until the offset is the same for both positive and negative voltages, +/- 30mV.

ADC Circuit Adjustment

The ADC adjustment procedure is used to calibrate the Analog-to-Digital Converter circuit and is accomplished using the Disk Diagnostic described in chapter 5. The diagnostic routines allow the user to display regulated voltage levels and adjust the ADC GAIN (R5) and ADC OFFSET (R3) to obtain the specified voltage ranges.

INTERNAL CLOCK ADJUSTMENT

This adjustment is performed on the Clock Board. This board selects internal and external clocks and enable circuits.

The following tools and test equipment are required to make the clock adjustments:

- Frequency Counter: Capable of 0.01% accuracy on ECL at 100 MHz
- Oscilloscope: 350 MHz Band Width, Horizontal Resolution to 1 ns/Div
- Extender Board: Gould Part Number 0117-0195-01

Adjustment is as follows:

1. Turn the power off on the K450B and remove the Clock Board from the card cage. Install on the Extender Board.

2. Connect input cables and probes to front panel connectors at SECTIONS A,B,C,D and E.

3. Turn the power on and verify unit passes the power up diagnostic test by displaying the Configuration screen.

4. Set the oscilloscope to 0.05V/div. Use the Tektronix P6106 X10, 1 megohm probe. Set the time base to 2ns/div. Set the trace base line at +1.30V above the center line so that the ECL threshold (-1.30V) is at the center line of the screen.

5. Connect the oscilloscope probe tip input to pin 12 (output) on the 100102 IC device at board location 12C. Connect the probe ground lead to the ground lug at board location 11B. See Figure 3-12 for clock board component locations.

6. Adjust pot R19 for approximately 50% duty cycle, symmetrical about the ECL threshold.

7. While probing IC 12C, pin 12, adjust trimmer cap C8 for maximum peak-to-peak frequency amplitude.

8. Re-adjust symmetry pot R19 for a 50% +/- 2% duty cycle about the ECL threshold. Monitor IC 12C, pin 12 or 13 with an oscilloscope. Verify that the rising and falling edges are sharp, not fuzzy.

9. Connect a frequency counter (use non-metallic adjustment tool) with a 1 megohm input to IC 12C, pin 12 or 13. Verify for a frequency of 100 MHz +/- 0.1% (99.9 MHz to 100.1 MHz).

10 Turn the unit off.

11. Turn on the unit and check for a frequency of 100MHz on the oscilloscope. If the frequency is not stable, repeat steps 4 through 10.

12. Turn off the unit and remove the clock board from the extender board. Install the clock board inside the K450B chassis. Turn on the unit.

13. Check for the proper frequency and duty cycle (symmetry) at IC 12C, pin 13. Re-adjust if necessary. Use the oscilloscope probe tip with insulated ground. Use the same ground lug location with short ground lead attached.

14. If readjustment is necessary, turn the unit on and off. Re-check the frequency to verify the frequency is stable.

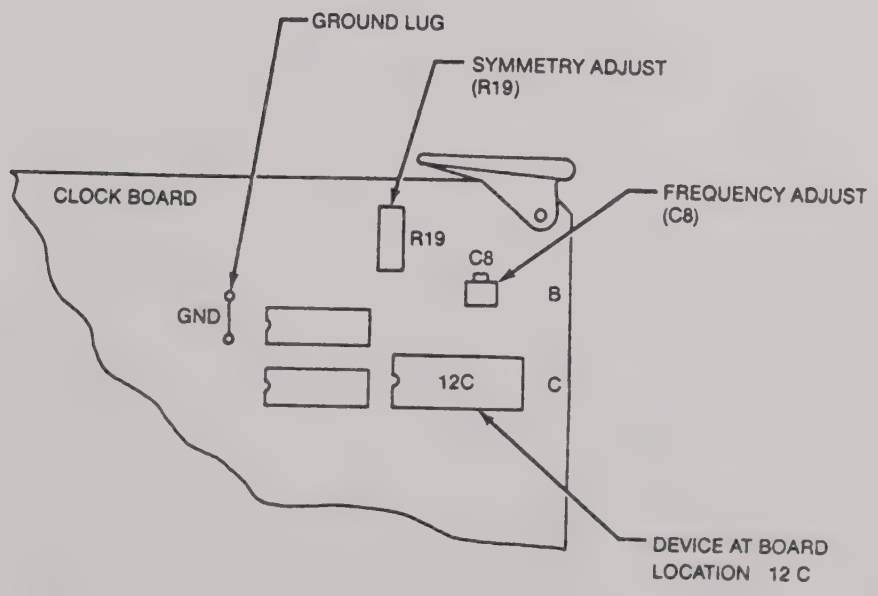


Figure 3-12. Clock Board Internal Clock Adjustment

Chapter 4

THEORY OF OPERATION

GENERAL

This chapter describes theory of operation for the K450B Logic Analyzer. An overview of the operation is presented to show the relationship of the various circuit functions. The overview is followed by a description of internal circuit functions for each printed circuit board. These descriptions are referenced to specific board components and circuit functions found in schematic diagrams of chapter 7. In most cases a block diagram is provided to support these descriptions. Where signal names are described throughout this chapter, an asterisk (*) after the signal name indicates active-low logic level. Theory of operation is provided for the following printed circuit boards:

- Data Display Board
- MPU Board
- Threshold/GPIB/RS-232 Board
- Clock Board
- Data Board
- Control Board
- Storage Controller Board

OVERVIEW OF K450B UNIT OPERATION

The block diagram of Figure 4-1 presents the overall K450B system data flow and control operations. This diagram also shows the K450B system architecture and interaction of board circuit functions.

MPU Board Interaction

The K450B Logic Analyzer employs a 16-bit, 8086 microprocessor for controlling system operations. The 8086 CPU is located on the Master Processor Unit (MPU) board. The MPU Board addresses all other boards in the system as I/O devices. The MPU Board communicates with the circuit boards through the multiplexed address/data bus interface on the mother board. The operating system uses up to 256K bytes of ROM and 512K bytes of RAM on the MPU board.

The K450B operating system and power-up diagnostic routines are resident firmware programs stored in the 14 EPROM chips located on the MPU board. This firmware executes the K450B operations that perform digital circuit analysis and processing of external data and clock signals supplied by the user's target equipment.

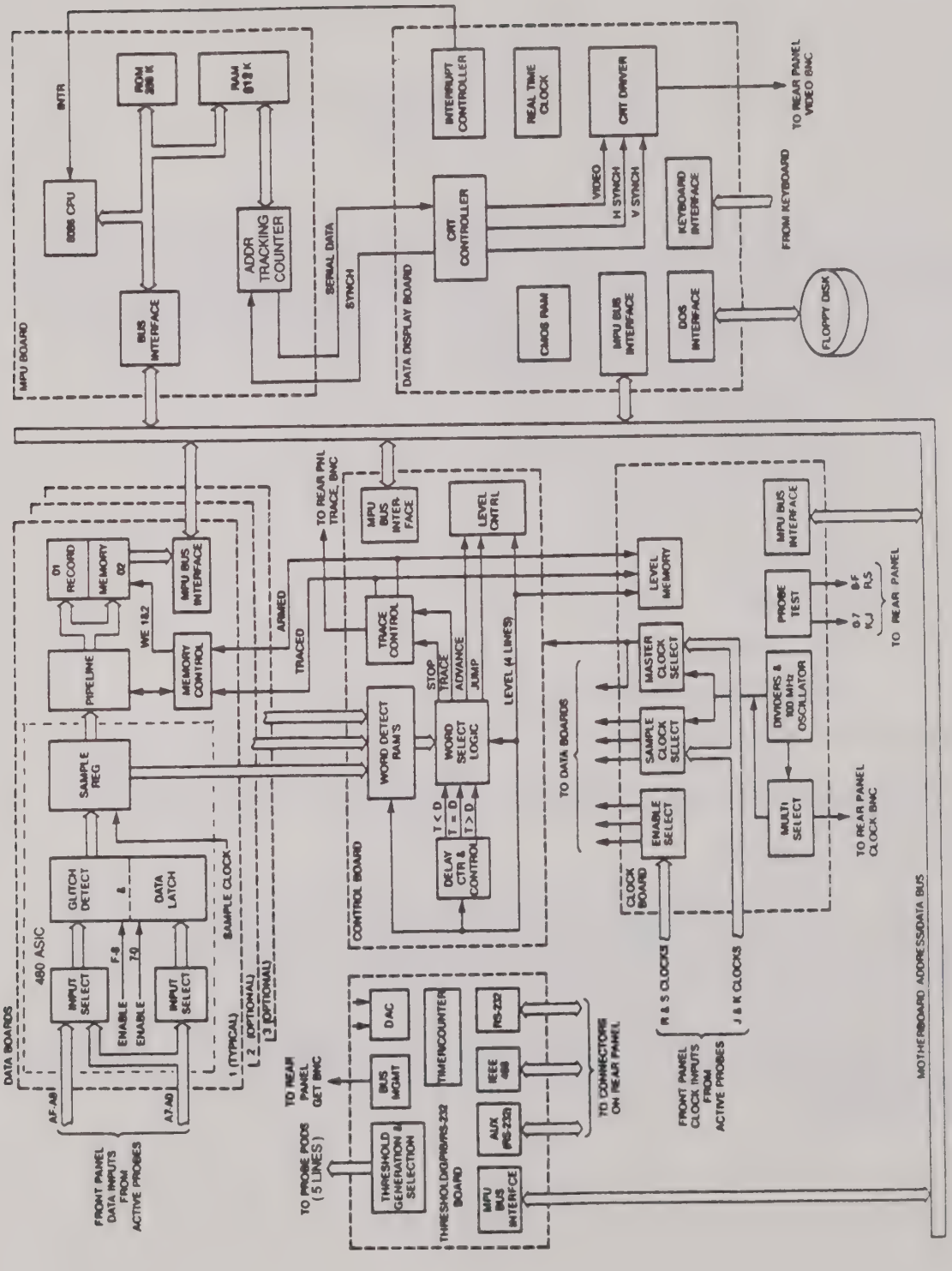


Figure 4-1. K450B System Block Diagram

Information collected and analyzed by the system is recorded in main memory. The results are selectively accessed by the user and displayed on demand. The MPU Board provides the control functions for display, display setups, memory transfer, memory control, memory compares and keyboard input.

Data Board Interaction

The external data and clock input signals collected by the probes are supplied to the input panel. The data input signals (7-0 and F-8) are directed to the Data Board. Each Data Board accepts up to 32 channels of data. The clock input signals (J & K and R & S) are sent to the Clock Board. The Data Board uses Gate Array circuits that receive input data signals, select high/low bytes and detect glitches. These functions define the sample content through pipeline control circuits to main memory and word detection RAM on the Control Board. Control signals from MPU holding registers select the data source that is passed through the sampling circuitry. Input signals from the Control Board initiate the ARMED and TRACED condition so that the sample is recorded in Memory.

Clock Board Interaction

The Clock Board combines and selects clock signals to generate Latch, Sample and Master clocks. The J & K clock inputs and R & S latch inputs are combined in user defined AND/OR Boolean expressions. The internal clock is generated on this board. It is always available at the CLOCK output BNC connector on the rear panel.

The 100MHz internal clock is also generated on this board. The user selected clocks and combined clocks are routed to the Data Boards and the trace Control Board. The PROBE TEST output signal at the rear panel connector is generated by the pattern generator on the Clock Board.

Control Board Interaction

The Control Board contains decision making logic for control of the trace and recording process. This includes word recognition circuits that detect the sample data supplied from the Data Boards. Delay counter logic combines delay conditions with detected words to set up sequencing for Stop Recording and to Jump or Advance to another recording level with different parameters. Delay counter logic also enables or disables recording for input sample data. The trace control logic resolves these conditions to initiate the ARMED and TRACE signals. These signals are sent to the Data Board to enable recording of the traced information. The Control Board also generates the TRACE output signal supplied to the BNC connector on the back panel.

Threshold/GPIB/RS-232 Board Interaction

The Threshold/GPIB/RS-232 Board generates two variable, and two fixed threshold voltage sources that are supplied to the probes. The variable voltages are VAR A and VAR B. The fixed voltages are TTL and ECL. Threshold control circuits enable each probe to select one of these voltage sources. The VAR A and VAR B threshold levels are driven by software-controlled, digital-to-analog converter (DAC) circuits. A comparator circuit performs the analog-to-digital conversion (ADC) that is used by the power-up diagnostic to measure power supply voltage levels.

The TTL and ECL Threshold sources use a voltage divider network and +/- 10V reference voltage for generating the fixed levels. Both the RS-232 and AUX serial communication links are driven by a Universal Synchronous/Asynchronous Receiver/Transmit (USART) chip. The GPIB (IEEE-488) parallel interface for Talker/Listen modes transfer data under control of an Interrupt line. The GPIB control circuits generate the interrupt signal supplied to the Data Display Board. The GPIB control circuits also generate the GET (Group Execute Trigger) output signal supplied to the BNC connector on the rear panel.

Data Display Board Interaction

The Data Display Board presents a display pattern that is derived by the MPU processing and stored in the RAM as a complete dot map. Each dot location of the CRT is represented by a bit in the RAM (where 1 = white, 0 = black). Each dot is supplied to video control circuits on the Data Display Board. The video control circuits accept CRT address clocking information and serial input data supplied by the MPU. The circuits generates the video control signals that drive the horizontal, vertical, and synchronization for the CRT. The CRT controller circuits continuously interact with processor circuits to generate direct memory access cycles from the RAM. This data is translated to the CRT. A 16-bit word is read from the RAM every 2 us and converted into a string of 16 dots on the CRT. The Data Display Board also accepts interrupt signals generated by other board circuits. The interrupt signals are used by the Data Display Board interrupt processor to send an interrupt to the MPU.

The Data Display Board provides the Keyboard interface and DOS interface. The Real Time Clock and CMOS Memory Save circuits are backed up by battery power. These batteries drive the circuits when facility power is interrupted or removed from the K450B unit. The Audio Error Alarm circuit is also contained on the Data Display Board.

DATA DISPLAY BOARD OPERATIONS

Overview

This section describes Theory of Operation for the K450B Data Display Board assembly, Part Number 0121-0200-30. The Board Assembly Drawing, Schematic Diagrams and List of Material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions of circuit functions. The Data Display Board block diagram is shown in Figure 4-2. The following board circuit functions are described:

- CRT Controller (Schematic Sheets 1)
- Interrupt Processor (Schematic Sheet 2)
- Keyboard and Front Panel Interface Circuit (Schematic Sheet 2)
- CMOS RAM Save Circuit (Schematic Sheet 3)
- Audio Error Alarm Circuit (Schematic Sheet 2)
- Real Time Clock (Schematic Sheet 4)
- DOS Interface Circuit (Schematic Sheet 4)

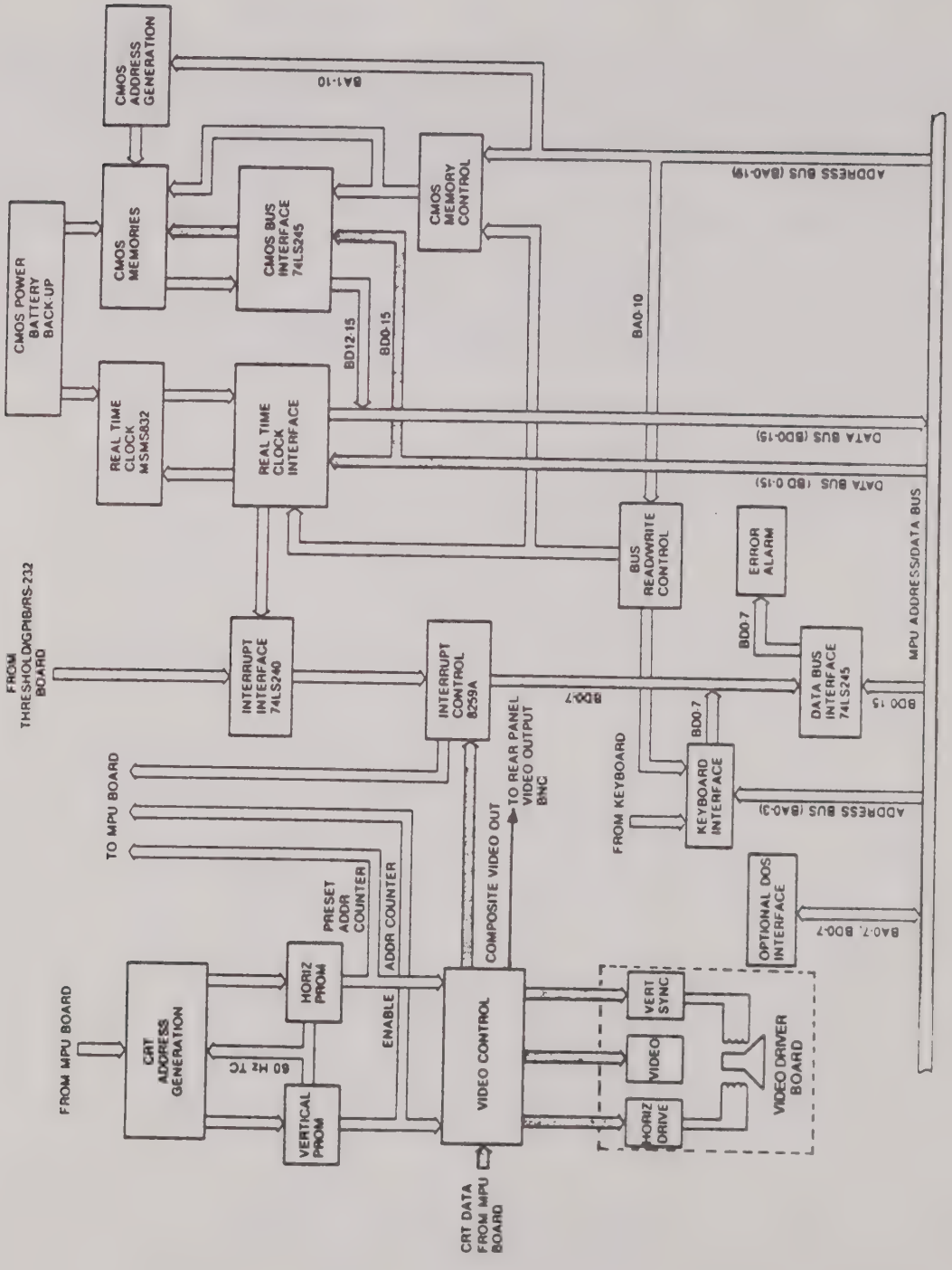


Figure 4-2. K450B Data Display Board Block Diagram

CRT Controller

The CRT Controller circuit (sheet 1 of schematic diagrams) generates a standard raster scan display format with data presented as a series of horizontally scanned lines. Each line starts at the left of the screen and goes to the right. The first line is at the top of the screen and the last is at the bottom. Standard sync and blanking signals are generated. The K450B operates at a 60Hz scan rate at all times.

Horizontal Timing: Each horizontal scan line is 51.2 usec long. Each scan line has 41.6 usec of video with 9.6 usec blanked and a 4.8-usec sync pulse during the blank time. The LS161 Horizontal Counter at location 9A and 10A runs continuously at a 625 KHz rate generating the five address lines for the horizontal ROM at 10B. The Horizontal ROM decodes the address to produce the blanking, sync and top count (end-of-line) pulses (74LS175 location 9B). The horizontal blanking interval occurs for the first 9.6 usec after the counter rolls over, states 0 through 5 (pin 7 of 9B). The sync pulse at pin 3 of 9B starts 1.6 usec after the blanking and lasts for 4.8 usec. In addition to addressing the ROM, the fifth address line is used by the horizontal drive for the deflection (pin 10, location 10C).

Vertical Timing: The vertical timing cycle begins with counters preset to E200 Hex. The horizontal and vertical PROMs decode top count after counting 290 lines, and reset the counter to E200 Hex. Simultaneously with the vertical top count, the vertical PROM generates the PRESET ADDRESS COUNTER * signal which synchronizes the tracking address counter on the MPU board. The The vertical sync pulse is decoded to occur at line 35 Hex.

Horizontal Deflection and High Voltage: The horizontal drive signal from the CRT controller synchronizes the horizontal scanning with the retrace blanking by controlling the horizontal drive transistor, Q108 (See schematic diagram 9000-0163). The horizontal drive transistor (Q 108) provides energy to the flyback transformer (T100) and it draws current from the horizontal deflection coil to generate the scan from left to right. The Flyback Transformer, provides the energy for rapid retrace from right to left. It serves as an ac to dc converter for generating the operating voltages for the CRT. The following voltages are supplied to the CRT:

+14.5KV	CRT Anode
+350V	Focus
+48V	Cathode
-200V	CRT Grid

The horizontal deflection and high voltage circuit allows adjustment of the Focus (VR200) and Brightness (VR105). The Horizontal Width adjustment (L101) and Linearity adjustment (L102) are also present. The CRT brightness can be increased and decreased by the software using the Date and Time, Setup display. The minimum brightness, however, is set by VR105.

Vertical Deflection: The vertical processor (sheet 1 of schematic diagrams) generates and synchronizes the vertical scanning. The vertical processor drives the vertical deflection coil directly, and senses current by means of the coil through a sense resistor. The vertical control circuitry contains an oscillator that is synchronized to the vertical sync pulse, an adjustable constant current source ramp generator, an emitter follower, and a power amplifier to drive the coil. The vertical processor circuitry allows adjustment of Vertical Size (VR101).

Video: The CRT brightness is controlled by combining the digital data with the horizontal and vertical blanking signals and switching the cathode voltage between zero volts (white) and +48V (black). The video is modulated by a 10MHz clock signal to provide a sharper display presentation. A composite video signal is also generated at the rear panel BNC connector for use with another video monitor.

Video Operation: Transistor Q104 (Schematic diagram 9000-0163) operates as the video amplifier and applies the video signal to the cathode of the CRT. R155 is the load resistor connecting Q104 to the 48 Vdc supply. The 48 Vdc supply is composed of D102 and ZD148. The -200 Vdc grid bias supply for the CRT consists of C200, C123 and C124. D105 and D104 comprise the 350 Vdc focus electrode supply.

The source voltage for these supplies is the high-voltage transformer, T101. Note also that T101 supplies the 14.5KV for the second-anode of the CRT. The rectifier for the high-voltage is an integral part of the second-anode lead. The filter capacitor for the high-voltage is the 600pF capacitance of the CRT aquedag coatings.

Transformer T101 and transistors Q107 and Q108 drive transformer T100. When Q108 is conducting, energy is stored in the primary of T100. When Q108 is switched off, the energy stored in the T100 primary is transferred to the secondary.

When Q108 switches off, the voltage at its collector rises to approximately 120 Vdc and is impressed upon the horizontal deflection coil through L101 and L102. This voltage causes a current to flow in the deflection coil, which in turn causes the electron to deflect to the left side of the CRT. The positive current flow decays in a linear manner, being zero at center screen. Because of the resonant circuit, C136 and the deflection coil, the current increases in the negative direction for the right side of the screen. At center screen Q108 again switches on and remains on until the beam is deflected to the right side of the screen. At this time, Q108 again switches off, and the process is repeated.

Interrupt Processor

The Interrupt Processor circuit (sheet 2 of schematic diagrams) accommodates up to eight levels of interrupts (INT0 - INT7) using a 8259A Interrupt Processor chip (2E). Seven levels of interrupts are used with the following assignments:

INTERRUPT LEVEL	ASSIGNMENT
INT7	Floppy Disk Controller
INT6	1 Second (Time of Day Clock)
INT5	(Not used)
INT4	Timer #0
INT3	Auxiliary, RS-232 (USART#2)(RXRDY+TXRDY)
INT2	RS-232 (USART #1) (RXRDY+TXRDY)
INT1	GPIB
INT0	60Hz (CRT Interrupt)

Keyboard and Front Panel Interface Circuit

The Keyboard and Front Panel Interface (sheet 2 of schematic diagrams) are addressed simultaneously by the microprocessor. The interface circuit decodes eight addresses out of the I/O map. Each row is read as a byte at a 60Hz rate. Any key contact that is closed is stored as a zero within the selected byte. Each bit of the byte corresponds to a column on the keyboard.

CMOS RAM Save Circuit

The CMOS RAM Save circuit (sheet 3 of schematic diagrams) provides 8K x 16 memory storage. If the K450B unit is powered down, the save circuit stores the parameters displayed on the screen. A 2.9V battery (location B1) provides power to the two 64K CMOS RAMs and the Real Time Clock when the unit is powered down. Data to and from the 64K CMOS RAMs is transferred over a bi-directional data bus through the two 74LS245 Three-State Transceivers at locations 3C and 4C.

Real Time Clock

The Real Time Clock circuit (sheet 4 of schematic diagrams) is controlled by the MSM5832 IC module (location 2D) which drives the real time clock. A 32.768 KHz crystal (location Y1) is used to generate the clock frequency. The variable capacitor (C10) provides for adjustment of the frequency. The adjustment of C10 is set by the factory and is not available to the user. The clock is set by the software through the Date and Time Set-up display.

Audio Error Alarm Circuit

The Audio Error Alarm circuit (sheet 2 of schematic diagram) produces a low level beep tone when improper keyboard entries are made. The tone volume is controlled by R56. Enabling and disabling the tone is controlled by software selection through the Date and Time setup display.

DOS Interface Circuit

The DOS Assembly contains the Floppy Disk Controller board which communicates with the K450B through a signal cable link. The connector P4 on the Data Display Board (sheet 4 of schematic diagrams) provides the I/O link for the DOS Assembly. Information for Address (BA0-BA7) and Data (BD0-BD7) is supplied from P4 to the MPU Address/Data Bus on the mother board through the P15 and P16 edge connectors. The Interrupt control (INTR 7) signal is supplied to the 8259A Interrupt Processor (location 2E, sheet 2 of schematic diagram) where it is then directed to the MPU through the control bus.

MPU BOARD OPERATIONS

Overview

This section describes theory of operation for the K450B MPU Board, Part Number 0121-0440-10. The circuits on the MPU Board consist of an 8086 microprocessor, address registers, data transceivers, random access memory (RAM), read only memory (ROM), memory controller and I/O decoder. This board provides control functions for display, display setups, memory transfer, memory functions, memory compares and keyboard.

The MPU Board block diagram is shown in Figure 4-3. The Board Assembly Drawing, Schematic Diagrams and List of Materials are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Microprocessor (schematic sheet 2)
- Address Registers (schematic sheets 3 and 4)
- Memory (schematic sheets 3, 4 and 7)
- Memory Controller (schematic sheet 5)
- I/O Decoding (schematic sheet 6)

Microprocessor

The 8086 microprocessor (schematic sheet 2, location 10J) is used on the MPU Board to operate at 8 MHz clock rate in the minimum mode configuration. The 8086 microprocessor outputs a 20-bit memory address. Data is accessed as 16-bit words, subdivided into a low-order byte and a high-order byte. The low-order 16 address bus lines (AD0 to AD15) are multiplexed with the 16-bit data bus. The Byte High Enable signal (BHE) is used to identify the high-order byte, while A0 identifies the low-order byte.

Initialization is accomplished with activation (HIGH) of the MPU RESET pin (location 8B) for more than four clock cycles. The 8086 microprocessor terminates operations on the high-going edge of the MPU RESET and remains dormant as long as MPU RESET is HIGH. The low-going edge of MPU RESET triggers an internal reset sequence of approximately 10 clock cycles, during which time no other operations should occur.

Non-maskable interrupt request (NMI) is initiated when external logic inputs a low-to-high transition at the NMI pin by power-up signal (PUP) at locations 11H and 11B. A non-maskable interrupt has higher priority than the maskable interrupt. A maskable interrupt is generated when external logic inputs a HIGH level at the INTR pin. The 8086 CPU responds by generating INTA for the interrupt acknowledge cycle.

HOLD and HLDA are standard hold request/acknowledge signals. When external logic inputs HOLD high, the 8086 microprocessor enters a hold state upon completing the current instruction's execution. The 8086 microprocessor acknowledges the hold state by outputting HLDA high. Location 11H is the buffer for the INTR, INTA, and HLDA signals.

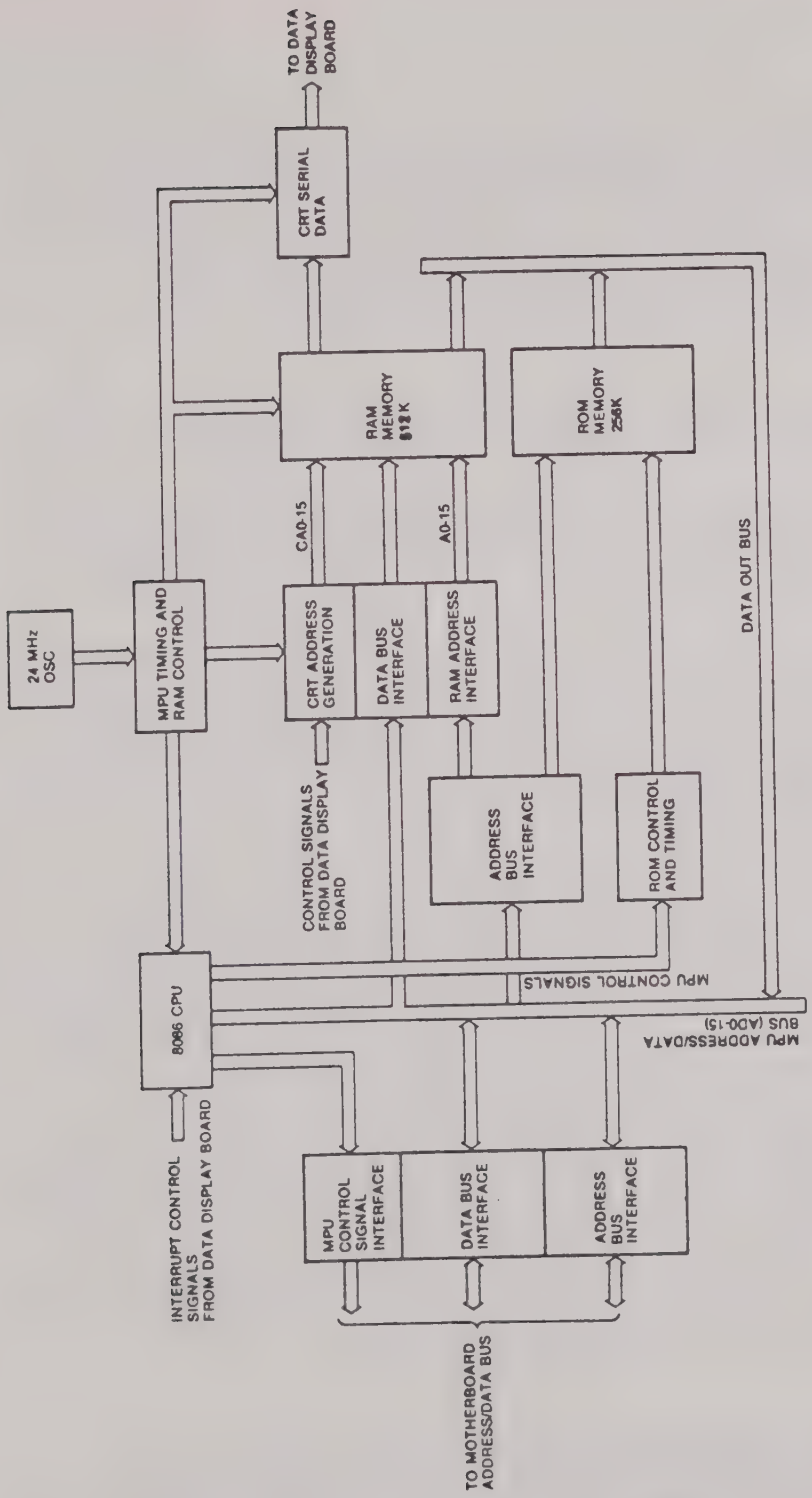


Figure 4-3. MPU Board Block Diagram

Address Registers and Data Transceivers

The 8086 microprocessor uses a multiplexed bus for address and data transfers (schematic sheet 2) The MPU Board demultiplexes the 8086 bus into two buses. One bus controls all transfers from the ROM to the RAM which is contained on locations 1A to 1E, 2A to 2E, 4A to 4H and 6A to 6H. The other bus interfaces with other boards in the K450B. Locations 9H, 10H and 11J are buffers for 20 memory address lines (A0 to A19) and BHE. Locations 9K, 10K and 11K are buffers for 20 address lines and BHE to boards other than the MPU. The transceivers for the data lines are located at 7K and 8K. Locations 7J, 7H, 8J and 8H are wired for PROM's and buffers for temporary test only. The 8086 loads addresses into the address registers by using the Address Latch Enable signal (ALE) and then transmits (WR) the data to, or receives (RD) the data from, the address in the register.

Memory

The 8086 memory space is organized into 16 segments of 64K bytes of external memory space (sheets 2 and 5 of schematic diagrams). Segments C, D, E and F (Hex) are the 256K bytes of ROM which contains the operating software. Segments 0 - 7 (Hex) contain the 512K bytes of dynamic RAM.

The ROM segment (schematic sheet 7), locations 1A to 1E and 2A to 2E, uses sixteen 16K X 8 memories arranged into eight sections of 16K words each. Locations 3L and 3M (schematic sheet 6) are ROM chip select decoders. Data output is read from ROM through a buffer at location 3J for high-byte data and at location 3K for low byte data.

The RAM segment (schematic sheets 3 and 4), locations, 4A to 4H and 6A to 6H, is made up of sixteen 256K X 1 dynamic memories providing 256K words (512K bytes). Data is input into the RAM, through the buffer at location 4J for high-byte data and at location 6J for low-byte data through RAM WRITE DATA EN. Data output is read from RAM through the latch buffer at location 4K for high-byte data and at location 6K for low-byte data through MPU LATCH ENABLE and EN RAM READ. CRT Data is read out into buffer registers at locations 6L and 4L and then shifted out at an 10 MHz clock rate to the Data Display Board by shift registers at locations 6M and 4M.

Memory Controller

The memory timing and the clock for the 8086 microprocessor (sheet 5 of schematic diagrams) are derived from a 24 MHz oscillator (location Y1). The clock generator/driver, (location 12H), is used to divide to an 8 MHz clock to the 8086 clock pin. Locations 11E and 12C divide the 24 MHz clock into timing signals used to generate the Row Address Strobe (RAS) at locations 10C and 8B. Additionally, Column Address Strobe (CAS0 and CAS1) are also generated at locations 8A, 9A and 12D. Write Enable signals for high-byte and low-byte of both RAM segments are generated at locations 7A, 8A, 8B, 10A and 10B. Row Select, Column Select and Latch Enable for both the MPU and CRT are generated at locations 9A and 9B.

The CRT port of the memory requests a word from memory every 1.6 us (625 KHz). The CRT page select addresses are generated at locations 7C, 7D, 8C and 8E (sheet 6 of the schematics) by the 625 KHz clock rate from location 7B.

If the 8086 requests a memory cycle during the CRT cycle, the memory controller uses the READY line on the 8086 microprocessor to generate wait states until the CRT cycle is finished. The memory then completes the requested 8086 memory cycle. The CRT Read cycle of one word every 1.6 usec also provides sequential operation required for the RAM refreshing.

I/O Decoding

The MPU Board addresses other boards in the system as I/O. The PROM (schematic sheet 4) at location 10F is used to decode addresses A11 to A19. When I/O is addressed, M/I0 goes LOW, causing the PROM's outputs to be HIGH. The conditions in which S.A EN is normally HIGH and DEN (Data Enable) becomes active and causes the EN OFFBOARD DATA signal at location 9C to go LOW, placing data on the bus. Read commands for RAM, ROM and S.A are generated by RD, RAM ADRS, ROM ADRS and S.A at locations 9D and 9E. Control signals RD, WR, DEN, DT/R and M/I0 are also buffered out to other boards through buffers at location 9G.

THRESHOLD/GPIB/RS-232 BOARD OPERATIONS

Overview

This section describes the theory of operation for the Threshold/GPIB/RS-232 Board assembly, Part Number 0114-0170-30. The circuits on this board generate threshold voltage levels, convert analog voltages to digital equivalents, control the GPIB Talker/Listener interface, and control the RS-232 Interface.

The Threshold/GPIB/RS-232 Board block diagram is shown in Figure 4-4. The Board Assembly Drawing, Schematic Diagrams and List-of-Materials are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Threshold Circuit (Schematic Sheet 1)
- DAC Circuit (Schematic Sheet 2)
- GPIB Interface Circuit (Schematic Sheet 3)
- RS-232 Interface Circuit (Schematic Sheet 4)
- MPU Interface (Schematic Sheet 5)

Threshold Circuit

The Threshold Circuit (sheet 1 of schematic diagram) generates voltage sources, (VAR A, VAR B, TTL and ECL) that may be selected for each section input.

The VAR A and VAR B thresholds are defined by the four 74LS273 Flip-Flop holding registers, locations 9B and 12B for VAR A, and locations 4B and 6D for VAR B. The holding registers buffer the MPU data bus to the two AD7533LN Digital-to-Analog Converters (DAC) at location 9A for VAR A and location 4A for VAR B. Separate calibration adjustments are provided for VAR A and VAR B Voltage levels. The VAR A Gain is adjusted by R6; Offset is adjusted by R9. The VAR B Gain is adjusted by R1. The Offset is adjusted by R2. Both DACs have a resolution of 10 bits.

The TTL and ECL thresholds are generated by using a voltage divider network and +/- 10V reference voltage level. The calibration adjustment for TTL is R8, ECL is adjusted by R7. The +/- 10V reference adjustment is controlled by R44.

The threshold voltages are supplied as input to eight analog multiplexers (sheet 2 of schematic diagrams). The selection of a particular threshold voltage (VAR A, VAR B, TTL or ECL) used by each probe is accomplished by a set of eight analog multiplexers and eight buffer amplifiers. Six of the multiplexers, at locations 1A, 1D, 1B, 1C, 2A and 2D are tied to high and low data bytes at input sections A, B and C. Two of the multiplexers are tied to R & S latch clocks (location 2B) and J & K sample clocks (location 2C). This allows the software to select one of the four voltages as the threshold. The outputs of the analog multiplexers are buffered by the operational amplifiers (locations 1E and 2E) which provide a gain of two that doubles the voltage of the DAC output.

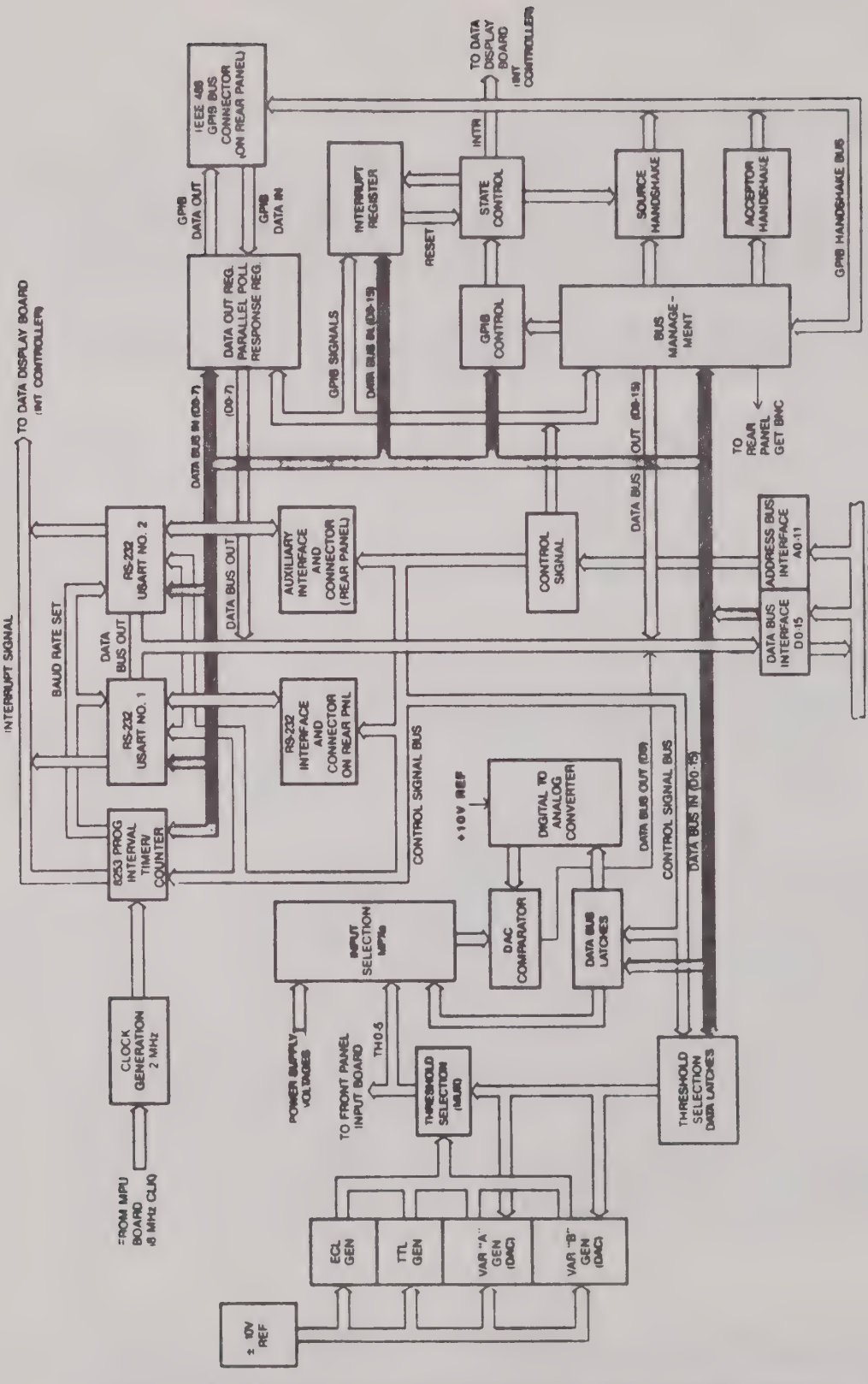


Figure 4-4. K450B Threshold/GPIB/RS-232 Board Block Diagram

DAC Circuit

One of the functions contained on the Threshold/GPIB/RS-232 Board is a software controlled Digital-to-Analog Converter and a comparator that performs Analog-to-Digital Conversions. This is used by the software to check the power supply and reference voltages during power up. Three multiplexers (sheet 2 of schematic diagrams) at locations 5F, 6F and 7F are used to select any one of the power supply voltages used in the K450B. The selected voltage is then scanned by the software using the 12-bit DAC at location 8A. When the DAC value exceeds the voltage being tested, the comparator (location 7A) becomes switched. The MPU compares the resulting value with a table of voltages and their tolerances to determine the pass/fail condition of the test result.

GPIB Interface Circuit

The GPIB Interface Circuit (sheet 3 of schematic diagram) is partitioned so that the handshake required to transmit individual bytes of information (for data or control) is performed by the hardware. All message generation or interpretation is done in the software. The GPIB address and mode for Talk Only, Talk/Listen and Listen Only, are determined by the interactive display for I/O setup. Once the Mode is determined, the GPIB control register is loaded with the specified mode information and the interrupt is enabled. All I/O data transfers occur under control of the interrupt line. With Listen mode selected, the receipt of a data byte or a command at the K450B will generate the interrupt. With Talker mode selected, the interrupt is generated when the byte has been accepted by the listener I/O device.

RS-232 Interface Circuit

The RS-232 Interface Circuit (sheet 4 of schematic diagram) causes information to be entered onto the Threshold/GPIB/RS-232 Board through two 8251A Universal Synchronous/Asynchronous Receiver/Transmitter (USART) at locations 12D and 12E. USART #1 interfaces with the K450B back panel RS-232 port. USART #2 interfaces with the AUX port. The Baud rate is set by the 8253B programmable interval timer/counter at location 8E. The internal timer uses a 2 MHz clock input derived from the CPU oscillator to measure the external master clock period. The bit rate clock output supplied to the USARTS is set at 16 times the actual rate at which data is being transmitted. Plus and minus 15-volt line drivers are used to send the signals to external devices.

MPU Interface

The MPU Interface circuit (sheet 5 of schematic diagram) buffers MPU data and address lines sent to the Threshold/GPIB/RS-232 Board through the mother board interface. The MPU data bus (BD0-BD15) is buffered onto the board by two 74LS245 bus transceivers, locations 14F and 12F which control the two-way direction of data transfers to and from the MPU Address/Data Bus.

The buffered data bytes, D0-D7 and D8-DF are transferred to, and received from board circuits for Threshold Selection Data Latch (schematic sheet 1), Bus Management and GET BNC output connector (schematic sheet 3), Programmable Interval Timer and RS-232 USARTs (schematic sheet 4), and GPIB Parallel Poll Register and Interrupt Register (schematic sheet 3).

The MPU address bus (BA1-BA11) is buffered onto the board by the 74LS244 Buffer/Line Drivers at locations 10F and 11F (schematic sheet 5). The jumper connector for M/I0 input signal supplied to line receiver at 11F must be connected across E13 and E14 to disable the memory mapped I/O and enable the I/O mapped I/O function. The 74LS244 buffers generate three state outputs that are supplied to five 74LS138, 1 of 8 decoders, locations 9D, 10B, 10D, 11B and 11D. These decoders accept three binary inputs and output one active-low control signal (from eight possibilities) for Write Hi Byte, Write Lo Byte, Read High Byte, Read Lo Byte. The control signals are supplied to on-board circuits that control the Threshold Selection Data Latch, Bus Management circuits, and rear panel GET BNC output connector, Programmable Interval Timer and RS-232 USARTs, and GPIB Parallel Poll Register.

CLOCK BOARD OPERATIONS

Overview

This section describes theory of operation for the K450B Clock Board assembly, Part Number 0121-0410-10. The circuits on this board provide all internal clock periods and programmable logic functions. These logic functions decode external clock inputs in accordance with the Master Clock, Sample Clock and Enable Boolean Expressions selected by the instrument operator. Also, circuits for the Level Memory, which store the level at which each sample was recorded, is located on the clock board.

The Clock Board block diagram is shown in Figure 4-5. The Board Assembly Drawing, Schematic Diagrams and List of Material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Internal Clocks and Probe Test (Schematic Sheets 2 and 3)
- External Clocks (Schematic Sheets 4 and 5)
- AND Master Clocks (Schematic Sheets 6, 7 and 8)
- OR Clock Selection (Schematic Sheets 4 and 8)
- Level Memory Circuit (Schematic Sheet 9)
- MPU Interface (Schematic Sheets 10 and 11)

Internal Clocks

All Internal Clocks (sheet 2 of schematic diagram) are derived from the 100 MHz oscillator circuit containing crystal Y1. The potentiometer, R19 allows adjustment of the average value of the 100 MHz signal on the emitter of Q2 so that symmetry of the clock output at location 12C, pin 12 can be set. The variable capacitor, C8 allows adjustment of oscillator frequency.

The two 10137 BCD counters, locations 9E and 10E (schematic sheet 3) are connected as decade dividers to provide the 10 MHz and 1 MHz decades. The 1 MHz output of 10E goes to Q1 which shifts the level, making it compatible with the input requirements of the counter at location 9C.

The two 14518 CMOS Dual BCD Counters at locations 9C and 9D operate between -5V and ground for compatibility with the ECL level. The outputs of all six decade dividers, are supplied to inputs of the eight-to-one, 10164 multiplexer at location 10C. The MPU can select any decade as the output of 10C. For clock frequencies greater than 10 MHz, the select lines to 10C, and the 10109 OR gate at location 10D, is set to all zeros by the MPU. This enables the 100102 OR gates at location 12C to output the 100 MHz (10n sec) clock. The selected decade feeds the input to the 10H016 Programmable Binary Counter at location 11B.

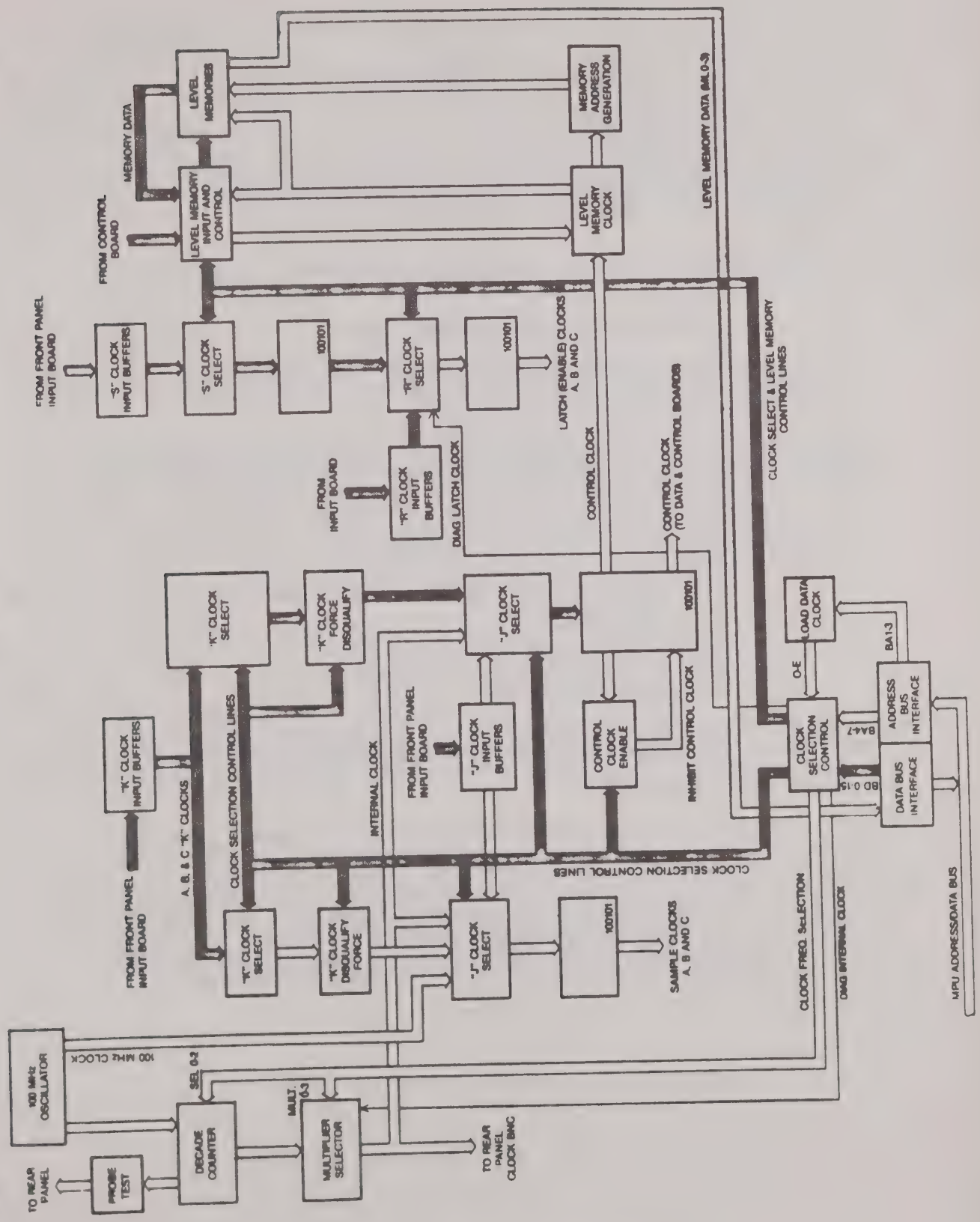


Figure 4-5. K450B Clock Board Block Diagram

The decade dividers with the programmable counter allows the selection of clock periods from 20 ns to 160 Ms in a 1 through 16 sequence. The software, however, limits the user capability to clock periods from 20 ns to 100 Ms in a 1 through 10 sequence. The BCD outputs of the 100 KHz decade counter also drives the select lines of the 4028 CMOS Demultiplexer at location 9B. The outputs of 9B provide a 1 of 8 pulse pattern to the rear panel PROBE TEST connector as test data.

The 1 MHz clock and the least significant bit of BCD counter at location 9C are also supplied to the rear panel PROBE TEST connector as test clocks. When an internal clock mode is selected, all external clocks are de-selected by the MPU (schematic sheet 8). The gate at location 3H, pin 21 is pulled low, enabling Internal clocks to pass through to the OR gate at location 4H, pin 9.

External Clocks

The External Clocks (sheets 4 through 8 of schematic diagram) consist of seven clock circuits as follows:

- Three Latch Enable Clocks (schematic sheets 4 and 5)
- Three Sample Clocks (schematic sheets 6 and 7)
- 1 Control (Master) Clock (schematic sheet 8)

Basically, all seven clock circuits are the same. Only the Control Clock selection, which is the most complex is described in subsequent paragraphs. The Control Clock selection gates have 13 inputs as follows:

- One Internal Clock
- Three AND* Clocks (AJ*, BJ* and CJ*)
- Three AND Clocks (AJ, BJ and CJ)
- Three OR Clocks (AK, BK and CK)
- Three OR* Clocks (AK*, BK* and CK*)

The major difference between Control Clock selection and the Latch Enable selection is the absence of Internal clocks for Latch Enable and the existence of Internal MPU Diagnostic Latch Enable.

AND Master Clocks Selection

The AND (Master) Clocks (sheet 8 of schematic diagram) are selected by the eight 100102 gates at locations 3C, 3H, 4C and 4D. Each of these gates has three inputs. Pin 19 is common to all gates and is driven by the output of the OR Clock selection gate at 4H. One pin of each of the 3C, 3H, 4C and 4D gates is driven by one of the J Clock inputs or their complements. The MPU controls the third input by placing a low on those gates whose J Clock input goes high when the selected clock is true. Only when all selected AND Clocks, or the OR Clock is true, will all of the outputs of 3C, 3H, 4C and 4D be low. This allows the control clock at location 4H, pin 9 to go high. Synchronous start-up of the control clock is provided by the dual flip flops at location 4B. This prevents "sliver" clocks from being passed at the beginning of a record cycle.

OR Clock Selection

The OR Clocks (sheet 8 of schematic diagram) are selected by the five 100102 gates at location 5J and parts of the two gates at 5D and 4H. The MPU places a low on one input of each gate whose other input will be low when one of the selected OR Clocks is true. The OR clocks are the K Clock inputs.

Jumper selection for external clocks (schematic sheet 4, section A8) shows the jumper configuration table. With all jumpers positioned on the left two pins, the board is configured for all twelve clocks. With jumpers positioned on the right two pins, the CK Clock comes from the BS probe and the CJ Clock from the BR probe.

NOTE: The software cannot read these jumpers, but counts the number of Data Boards in the system.

Level Memory Circuit

The Level Memory circuit (sheet 9 of schematic diagram) records which level of trace control is used for each word recorded on the Data Boards. Level data enters the clock board through the 20-pin header, J1.

The two 10176 registers at locations 11E and 11F and single 10173 register at location 11J operate as a pipeline which holds the level data temporarily while the decision is made to either record or not record the data. This decision is made on the Control Board which generates the Armed and Traced signals along with the level data that is sent to the pipeline. When the Traced signal is high, its complement is clocked into register 11F along with the level data. This action allows the OR gate, 12E to produce a write enable pulse on the next control clock transition. If the Traced signal is false, OR gate 12E is disabled and the level data in register 11F is written over at the next sample without being recorded. If the Armed signal goes false, the level memory becomes locked up.

The three 10H016 address counters at locations 11G, 12J and 12H are used for the 10474 memories at locations 12F and 12G. The level memory is multiplexed in two ways. First, through the 10231 latch, pins 14 and 15 (location 11D) which select the memory phase that is written to on each sample. Second, through the 11D 10231 latch at pin 3, which provides uniform 10n sec pulses when recording is in process regardless of the sample rate.

In read mode, the OR gate at location 12D, pin 3 is disabled thereby causing the output of latch 11D, pin 3 to become 1/2 the frequency of the input. When the Armed signal goes false, the pin D input goes true thereby stopping the pulse.

MPU Interface

The MPU Interface circuit (sheets 10 and 11 of schematic diagram) interfaces the Clock Board circuits to the mother board through edge connector P2. The 74LS85 comparator at 12L (sheet 11) decodes four address inputs A4 through A7 from the MPU to provide the My Address signal when the Clock Board is addressed. The My Address signal enables the five 10124 TTL-to-ECL level translators at locations 6J, 7J, 8J, 9K and 10K (schematic sheet 10) which buffer the MPU data bus content onto the Clock Board.

The 10161 de-multiplexer at location 9J decodes address lines A1, A2 and A3 along with the MPU BWR control signal to create load pulses for the 20 10176 holding registers at locations 7A through 7H, 8A through 8H (sheet 10), 9G and 9H, 10J and 10H (sheet 11).

The 10173 multiplexer latch at location 10G multiplexes 8 bits of read data into two 4-bit nibbles which are translated from ECL to TTL levels by the 10125 translator at location 10F. The 74368 tri-state buffer at location 9F is enabled by the BRD signal sent from the MPU and the My Address signal generated by the comparator at location 12L.

The clock Board is configured with eight jumpers located at the lower left corner of the board. These jumpers select clock signals for 32-input or 64-input capability as determined by the number of Data Boards installed in the unit. When the Number 2 Data Board is added to an existing 32-input unit to provide 64 inputs, it is necessary to rearrange the jumper connections to enable the SECTION C clock inputs and the BR, BS clocks into the user specified Latch Clock equation. The jumpers must be relocated from the eight center/lower-row pins to the center/upper-row pins as described in Chapter 6, Options Installation.

NOTE: The K450B software will not recognize the SECTION C clock inputs unless these jumper connections are completed.

DATA BOARD OPERATIONS

Overview

This section describes theory of operation for the K450B Data Board assembly, part number 0121-0415-10 and -20. Up to three Data Boards (Nos. 1, 2 and 3) may be installed in the K450B to provide 80 input channels. The -10 Data Board (No. 1 and 2 processes 32 channels of input data. Therefore, one board is installed to provide 32 channels at Input Sections A and B. Two of these boards are installed to provide 64 channels at Input Sections A, B, C and D.

The -20 Data Board (No. 3) processes 16 channels of data. One of these boards is installed to provide 16 channels at Input Section E.

Circuits on the Data Board receive input data signals supplied from the user's target equipment, select operating modes, generate pipeline processing functions, record traced information in main memory, decode the MPU address/data bus and present status to the MPU.

The Board Assembly Drawing, Schematic Diagrams , and list of materials are provided in Chapter 7. Reference is made to schematic diagrams throughout the descriptions for the following circuit functions.

- Data Input Control (Schematic Sheets 4 and 6)
- Operating Modes (Schematic Sheets 9 & 6)
- Memory Control (Schematic Sheet 3)
- MPU interface (Schematic Sheet 2)

K450B DATA BOARD

BLOCK DIAGRAM (CH A)

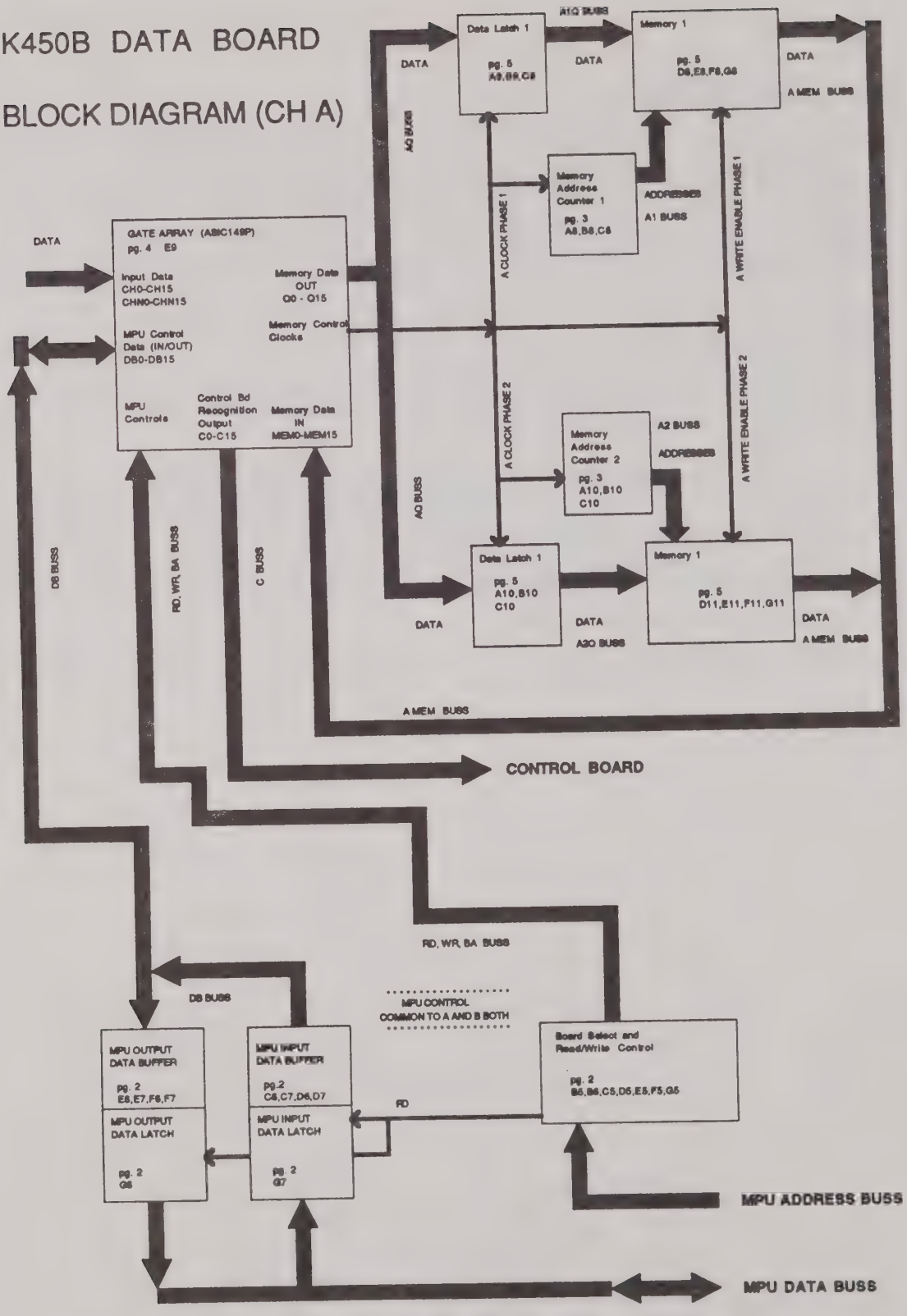


Figure 4-6 K450B Data Board, Block Diagram

Data Input Control

The differential input signal from the probe is received at the Gate Array on the data board. The data board accepts up to 32 channels of data and stores the data in high-speed memory. Two identical Gate Arrays, E9 (Schematic Sheet 4) and E2 (Schematic Sheet 6) receive the data inputs and perform most of the processing and pipelining before data is sent to the memories.

Each gate array handles 16 data channels. Since each of the gate arrays and its associated counters, registers and memories operate identically, only Gate Array E9, and its associated circuitry for input Section A will be discussed.

Control signals from the MPU select which of the four data sources, Memory, Probe, Multiplex, or Diagnostic, will be passed through to the sampling circuitry. A description of each data source type follows:

Memory Data: This data source is a generation of channel memory output which is used only for self-diagnostic purposes and to read out memory to the MPU.

Probe Data: This data source is used in normal input mode (Normal Select).

Multiplex Data: This data source obtained from the low order channels (7-0) is also routed to the high order channels (F-8). In this case, channel F is paired with channel 7, allowing single probing when demultiplex is selected (Demux Select).

Diagnostic Data: This data source is supplied by the MPU for self-diagnostic purposes.

Operating Modes

The gate array contains internal latches that are set by the MPU to control the operating mode of the gate array. The gate array generates the control signals to select the following operating modes:

Normal Mode: This mode allows balanced data from the probes to be processed to the sample register and pipeline register. Output from the sample register is buffered and sent to the Control Board to generate trace conditions for selected patterns.

Glitch Capture Mode: The latch clock is disabled in this mode to allow a feed-back signal from the sample register to indicate the presence of positive and negative glitches. This mode can also be used when the Normal Mode is selected.

Memory Select Mode. This mode allows the MPU to read the contents in high-speed memory. The reading occurs after the memory data passes through the memory latch or after it passes through the pipeline.

Diagnostic Mode: This mode generates 16 signals that are used as inputs to check the circuits of 16 channels. This check determines if the channels are operational. Different data patterns can be placed into latches, sample registers, pipeline, and high-speed memory source locations. The data patterns are then read out and checked by the MPU to detect any variation between the source input pattern and resultant output pattern.

Demux Mode: This mode is used when a latch clock is selected at one channel and a transparent latch is selected for the other channel. This mode is also used for 200 MHz applications where channel 0 uses a 100 MHz latch clock that is 180 degrees out of phase with the sample clock (i.e. delayed by 5ns from the sample clock) while channel 8 uses a transparent latch.

Memory Control

Circuits for memory counters are presented in sheet 3 of the schematic diagram. The 10H016 Programmable Binary Counters (locations A8, B8 and C8) generate the 10-bit address for A1 memories. The identical counters at A11, B11, and C11 generate the 10-bit address for A2 memories. These counters are reset by the A_ADRS_RST signal which comes from the gate array but is controlled by the MPU.

The signals, ACKPH1 and ACKPH2 are clocks for the A1 and A2 memory counters. These signals come from the gate array and are 180 degrees out of phase with each other. The maximum clock rate is 50MHz.

The memory and registers for the A gate array are shown in sheet 5 of the schematic diagram. Data from the gate array is contained on the 16-bit, AQ bus which represents data from the 16 channels. This data is loaded alternately into 10H176 registers for A1 memory (locations A10, B10 and C10). Registers at A1 are loaded by the ACKPH1 clock. Registers at A2 (locations A9, B9 and C9) are loaded by the ACKPH2 clock.

Data from the A1 registers is then stored in the A1 memories (10474 memory locations D11, E11, F11 and G11). Data from the A2 registers is correspondingly stored in the A2 memories (locations D8, E8, F8 and G8).

The write pulses for the memory AWEPH1 and AWEPH2, come from the gate array and are phased alternately as the ACKPH1 and ACKPH2 pulses. The output of the AMEM bus is a Wired-OR of the A1 and A2 memory. These outputs are returned to the gate array where the contents are read out by the MPU.

MPU Interface

The MPU Interface circuits (schematics sheet 2) decode the MPU Address Bus and Data Bus and converts read, write and control signals from TTL to ECL levels. RDNA is the ECL read signal, and WRNA is the write signal both of which are sent to the Section A gate array.

The 10124 Translator (location E5) outputs the signals, BA1E, BA2E and BA3E which serve as address locations within the gate array that are either written to, or read from. The DB Bus is the 16-bit bi-directed ECL data bus that corresponds to the TTL, tri-state, bi-directional BD Bus.

The 74S85 four-bit comparator (location F5), 74S155 dual, two-line decoder (location C5), 10124 TTL-to-ECL translator (location D5), 74LS74 latch (location B5) and 74S37 AND gates (location B6) operate to decode the address B4 (HEX) to B7 (HEX). This decoded signal is combined with the BWR or BRD signal to generate the RDNA or WRNA signals. The 74-LS74 latch (location B5) is used to reshape the BWR signal that is sent to the gate array.

CONTROL BOARD OPERATIONS

Overview

This section describes theory of operation for the K450B Control Board assembly, part number 0121-0420-10. The Control Board contains all decision making logic for controlling the recording process.

This includes word recognition circuits, delay counters, and the logic to combine delay conditions with detected words. These circuit functions cause the K450B to stop recording, jump or advance to another level with different record parameters and selectively enable or disable the recording operation.

The Control Board Block Diagram is shown in Figure 4-7. The Board Assembly Drawing, Schematic Diagrams, and List of Material are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions for the following circuit functions:

- Word Recognition Circuits (Schematic Sheets 2,3 and 4)
- Word Selection Circuits (Schematic Sheets 5 and 6)
- Level Switching Circuit (Schematic Sheet 7)
- Delay Counter (Schematic Sheet 8)
- Recording Control Circuits (Schematic Sheet 9)
- MPU Interface (Schematic Sheet 10)

Word Recognition Circuits

The Word Recognition Circuits are contained on sheets 2, 3 and 4 of schematic diagrams. Word recognition is accomplished separately for each Input Section, A, B, C, D and E. The separate words are combined in the word selection circuits described in subsequent paragraphs. In the circuit descriptions all references are made to the Section C Input (schematic sheets 3 and 4) which is used as an example. The other sections A, B, D, and E operate identically to Section C.

The DATA* signal supplied from the Q* output of the sample registers on the Number 2 Data Board enters the Control Board through the mother board. It is synchronized with the control clock in the 10176 holding registers at locations 4H, 7J, and 7H (sheet 3). The data output from these registers is presented to four of the eight address inputs, and to each of the 10474, 256x4 Static RAMs at locations 4G, 7G and 7F. The other four address lines of the RAMs are driven by the LEVEL X signal, where X is the 4-bit number representing the level of trace control. The four data outputs of the 10474 RAMs correspond to the four combinational functions of the K450B for STOP, JUMP, ADVANCE and TRACE signals generated by the 100101 OR gates at locations 1D and 3D (sheet 4).

The MPU initializes the RAMs to contain zeros only at those address locations and bit positions that correspond to the combinations selected by the user for STOP, JUMP, ADVANCE and TRACE at each level.

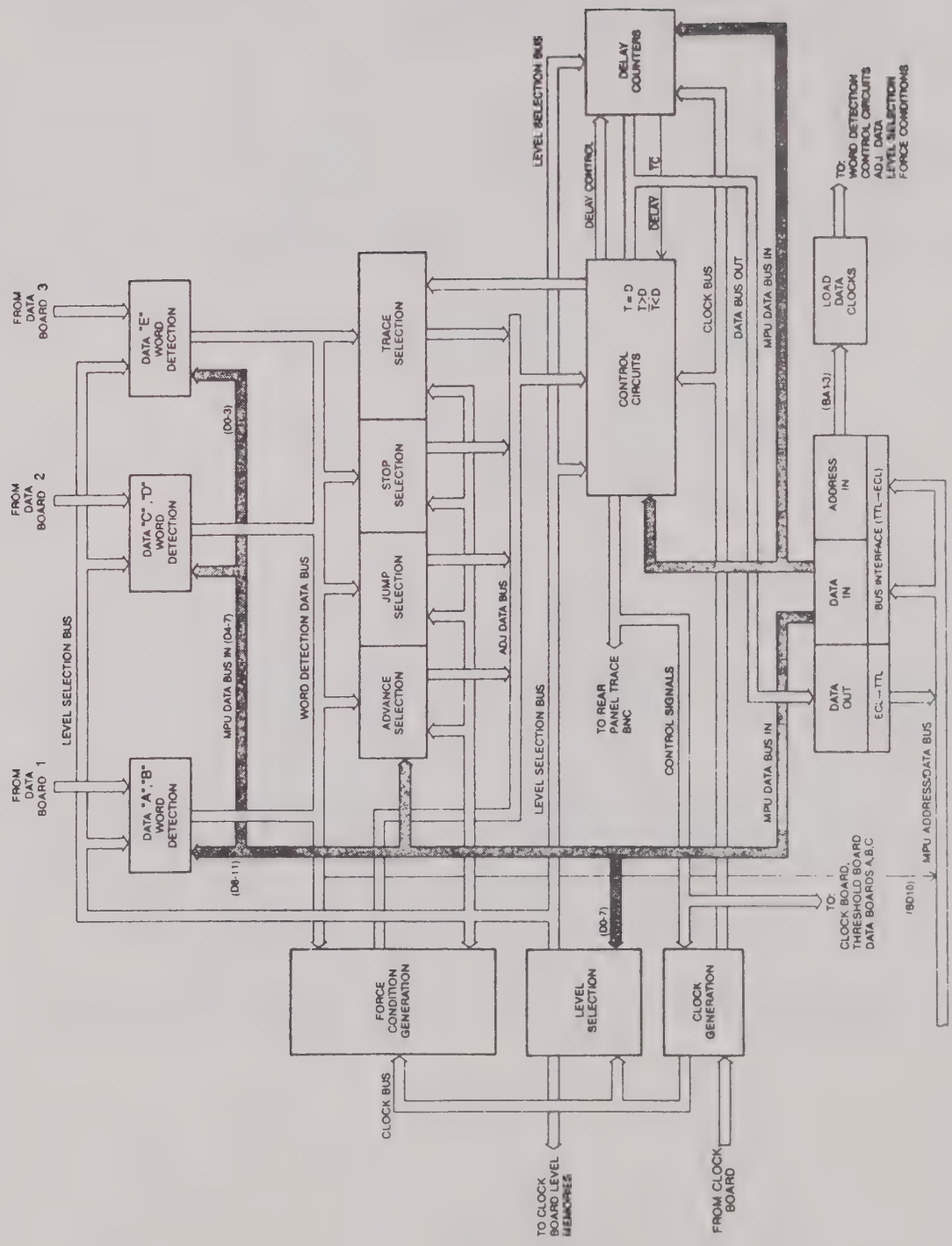


Figure 4-7. K450B Control Board Block Diagram

The RAMs function as programmable logic arrays. They respond to different STOP, JUMP, ADVANCE and TRACE combinations at each of 16 levels for a total of 48 combinations. The 100101 OR gate at 3D combines the outputs from four RAMs into the signals for STOP C, JUMP C, ADVANCE C and TRACE C (where C = Section C Inputs). The 10176 Holding Register at location 3K stores MPU control signals that are used during initialization. The 10164 Multiplexer at location 4C gives the MPU access to section outputs for diagnostic purposes.

Word Selection Circuits

The Word Selection Circuits are found on Sheets 5 and 6 of the schematic diagrams. The signals for STOP A, B, and C; JUMP A,B,and C; ADVANCE A, B, and C, and TRACE A, B, and C are combined with the delay condition signals T<D* T=D* and T>D* in these circuits. In this example, only the ADVANCE select circuit is considered. The STOP, JUMP and TRACE circuits generally operate in the same manner as the ADVANCE circuit.

The signals for ADVANCE A, B, and C, and their complements along with the delay condition signals T<D*, T=D*, and T>D* are presented to the inputs of the 100102 gates at locations 5C and 5D. Each of these gates is also supplied with one of the outputs of the 10145A High Speed, 4x16 RAMs at location 4B, 5B and 6B. The outputs of gates 5C and 5D are NORed together in the 100101 gate at location 5F whose input must be low for the ADVANCE signal to go high. The Advance signal will be low if any of the gates at location 5C or 5D have lows on all three inputs. Pin 19 of gates at locations 5C and 5D is common to all gates. It is low at all times except during Diagnostic Tests or when the Arm Initialization condition is present. The MPU can pull it high for the FORCE ADVANCE condition, as in the following example:

1. Assume the user has selected conditions for:Advance if Data=A and T=D

2. For this selection, the MPU would initialize the 10145A High Speed RAMs to place a low state at pins 1 and 17 of gate 5C. Signals at the appropriate level would be applied to pins 17 and 24 of gate 5D.

3. The controlling input signals to these gates become: ADVANCE B, T<D*, T>D*, ADVANCE C, and ADVANCE A.

4. If any one of these signals is low, indicating the selected equation is false, the output of the gate it controls will be high, causing ADVANCE* to be true and ADVANCE to be false.

The address inputs to the 10145A High Speed RAMs is the 4-bit LEVEL number (e.g., LEVEL 3C, LEVEL 2C, LEVEL 1C and LEVEL 0C). It is therefore possible to select a different Advance equation for each of the 16 levels of trace.

The inputs to the 100101 OR Gate at location 7D parallel the inputs supplied to OR Gate at location 5F which are controlled by the Word Recognition Logic, disregarding the delay conditions. The outputs of 7D are called EVENT and EVENT* which are used to control the delay counter in Events Delay Mode.

The 10176 Registers at locations 6A and 7A are used to hold MPU control signals which can force the signals for STOP*, STOP, JUMP*, JUMP, ADVANCE, ADVANCE*, TRACE, TRACE*, EVENT, and EVENT* to a desired logical state by overriding the normal input conditions. These signals are used during the Diagnostic Checks and the Arm Initialization Sequence. The register at 6A also enables the 10231 Latch at location 5A to FORCE ADVANCE for one clock period. This is used for manual advance and to begin the armed cycle when the unit advances from Level F into Level 0 on the first control clock.

Level Switching Circuit

The Level Switching Circuit is contained on sheet 7 of the schematic diagrams. The 100155 IC at location 5G is a Quad Multiplex Latch. The two sets of inputs to the latch come from the two 10145A RAMs at locations 5H and 5J. The address input to 5H and 5J is the 4-bit number level. The 5H and 5J RAMs are initialized by the MPU so that for any given level address, 5H contains the number of the user selected Jump To Level.

The 100155 has two Enable inputs, both of which must be in a low state for the selected input to be transferred to the output as the next level. One of the Enables is driven with the JUMP OR ADVANCE* control signal, allowing the level to change only when a JUMP or ADVANCE condition is detected. The other Enable is a 3nsec pulse derived from the control (master) clock. The new level then becomes the new address for the Level RAMs 5H and 5J. The propagation delays around the loops are that much greater than the 3nsec Latch Enable pulse that allows glitch-free operation to occur. The JUMP* condition present at pins 16 and 17 of 5G selects which set of inputs becomes latched. The decision to jump or advance gives priority to jumping even when the advance condition is true at the same time.

Delay Counter

The Delay Counter circuit is shown on sheet 9 of the schematic diagrams. The 10H016 Programmable Binary Counter at location 13C and 13E form a simple Programmable Synchronous Counter. The 10145 RAMs at location 14C and 14F are addressed by the Level. Each address is initialized by the MPU with the two's complement plus 1 of the delay number for the corresponding Level.

Recording Control Circuits

The Recording Control circuits are shown on sheet 8 of schematic diagrams. The ICs at location 12A, 12B and 14B store the status of the Control Board that was present prior to the most recent transition of the control clock. Note that all output signal names are expressed in past tense. The input conditions that caused the outputs to become true may not always remain true after being latched. These remembered state signals are decoded by gate circuits located at 11D, 11C, 11B, 11A, 11F and 9B along with the DELAY TOP COUNT (TC) signal (supplied from location 11D on sheet 9 of the schematic). The TC signal controls the delay status bits, T=D, T<D, and T>D to stop recording at the correct time and to control the process of selective trace recording.

The 100155 Mux Latch at location 12B has three inputs, EVENT* ,ADVANCE* and JUMP. Two of these inputs ADVANCE* and JUMP are connected to both the A and B Mux inputs and are clocked to the output regardless of the state of the Mux Selection Control on pins 16 and 17 of 12B.

The two output signals ADVANCED and JUMPED are ORed together at location 11C, to form the DELAY PE* signal. This allows the delay counter to become loaded on the next clock transition and Advanced or Jumped which is used to control the states of the delay condition signals.

The Mux Select control signal for 12B is the EVENT MODE signal which is output of the 10145A RAM at location 13A. This bit is high at those levels in which the user has selected Events Delay Mode. If EVENT MODE is low, the A Mux inputs of 12B are selected causing output pin 9 of 12B to become latched low only when EVENT* is low.

The output signal at pin 9 of 12B is called EVENTED* and is combined with the OLD TD* signal (which is at a low state if T was less than D prior to the last clock) to form the DELAY CE* signal. Operation in Events Delay Mode only allows the Delay Counter to increment once for each sample on which the selected event combination was true.

The 10055 Mux Latch at location 14B also has three inputs, ADVANCE, STOP and TRACE. The STOP and TRACE inputs are connected to both the A and B Mux inputs. The STOP input signal becomes STOPPED after being clocked through 14B and causes the ARMED signal to become false thereby ending the recording process. The TRACE input signal becomes TRACED* after being clocked. The TRACED signal is combined with ARMED and is fed to a BNC connector on the rear of the K450B chassis as the TRACE signal. The TRACED* signal is routed to the Data Boards where it is combined with the ARMED signal to allow the sample that caused the trace condition to be recorded.

The third input to Mux Latch at location 14B is the ADVANCE signal which is connected only to the B Mux input at pin 15. The Mux control input which determines whether ADVANCE will be latched in 14B is the END LEVEL signal which is one of the outputs supplied from the 10145A RAMs at location 13A. The END LEVEL signal will be high only at Level F.

The output signal at pin 9 of 14B is called ADVANCED and ENDED. As the name implies, the signal will be true only if Advance and End Level are both true when 14B is clocked. The Advanced and Ended condition causes the ARMED signal to go false thereby ending the recording process.

The 10176 Mux Latch at location 12A has six inputs: D=1 IF JUMP*, D=1 IF ADVANCE*, CYCLE RESET, T<D*, T=D*, AND T>D*. The CYCLE RESET signal is used only by the MPU during the Arm Initialization cycle or during Self Diagnosis. The other five inputs to 12A coordinate the switching of the delay status bits. The signals for D=1 IF JUMP* and D=1 IF ADVANCE* are supplied from the 10145A RAM at location 13A. These signals provide a look ahead function to provide delays of one which the 10016 Delay Counter (sheet 9) cannot provide. The signals for D=1 IF JUMP* and D=1 IF ADVANCE* will be low only if the next level (either the JUMP-TO or ADVANCE-TO level, or both) has a delay of one selected.

The outputs of 12A for D=1 IF JUMPED* and D=1 IF ADVANCED* are combined with the JUMPED* and ADVANCED* signals respectively at location 11C and 11D to cause the T=D signal to become true immediately upon entering a level with a delay of one selected.

The signals for T<D*, T=D* and T>D* are clocked through 12A to become OLD T<D*, OLD T=D* and OLD T>D*. These three signals also must be present at 11B, 11C, and 11D to ensure proper cycling of the delay condition bits. The 10164 Multiplexers at locations 12C and 12F provide access for the MPU to determine record control status for self-diagnostics.

MPU Interface

The MPU Interface is shown on sheet 10 of the schematic diagram. The 74LS85 Comparator at location 13H decodes the address bus to enable the interface only when the Control Board is addressed. The 10124 Translators at locations 11H, 11K, 9K, 8K and 11J provide TTL to ECL level translation for the 16 line address/data bus. The read data from the Control Board is multiplexed down to only four lines. These lines are translated from ECL to TTL levels by the 74368A Three-State Inverter Buffer at location 12H. The 10161 Demultiplexer at location 13G decodes Address Lines A1, A2 and A3 along with the WR* signal from the MPU to provide LOAD signals for the MPU programmable holding registers, word detection RAMs and control RAMs.

STORAGE CONTROLLER BOARD OPERATIONS

Overview

This chapter describes theory of operation for the Storage Controller Board Assembly, Part Number 0121-0090-10. This board provides data storage for one or two 5 1/4-inch disk drives installed on the logic analyzer chassis. The circuits on this board interface to the MPU Board to transfer, check and decode data that is sent to, or received from the disk drives. On board memory is provided to store data that is transferred to or from the disk drives under DMA control, thereby relieving the MPU Board to perform other tasks during the transfer.

The Storage Controller Board block diagram is shown in Figure 4-8. The Board Assembly Drawing, List of Material and Schematic Diagrams are provided in Chapter 7. Reference is made to the schematic diagrams throughout the descriptions of the following circuit functions:

- o MPU Board Interface (Schematic Sheet 1)
- o Storage Controller Board I/O Registers (Schematic Sheet 1)
- o Floppy Disk Controller and Floppy Interface (Schematic Sheet 2)
- o DMA and Memory Operation, Data Flow (Schematic Sheet 2)
- o Power and Clock Generation Circuits (Schematic Sheets 1 and 2)

MPU Interface

The MPU bus interfaces to the Storage Controller Board through a cable from the Data Display Board to connector J1 on the Storage Controller Board (Schematic Sheet 1). The MPU bus signals consist of eight data lines, eight address lines and control signals which include RD*, WR*, etc. The Storage Controller Board reports to the MPU Board by issuing an Interrupt (INT 7) signal. The MPU Board accesses the 8K x 8 RAM buffer on the Storage Controller Board by activating DMA Channel 2.

Storage Controller Board I/O Registers

Two Input and two Output registers are provided on the Storage Controller Board. These registers control internal on-board circuit functions and report status to the MPU Board. The selection for these registers and VLSI chips is initiated by the I/O Decode PROM (location 2H) and two I/O Decode chips (locations 2J and 2K).

Floppy Disk Controller and Floppy Disk Interface

The Floppy Disk Controller 8272 VLSI chip (Schematic Sheet 2, location 1C) provides the major control functions for data transfer between the MPU Board and disk drives.

Data Transfer Operations: The 8272 operation is accomplished in three phases as follows, and is presented in Figure 4-9:

1. Command Phase
2. Execution Phase
3. Result Phase

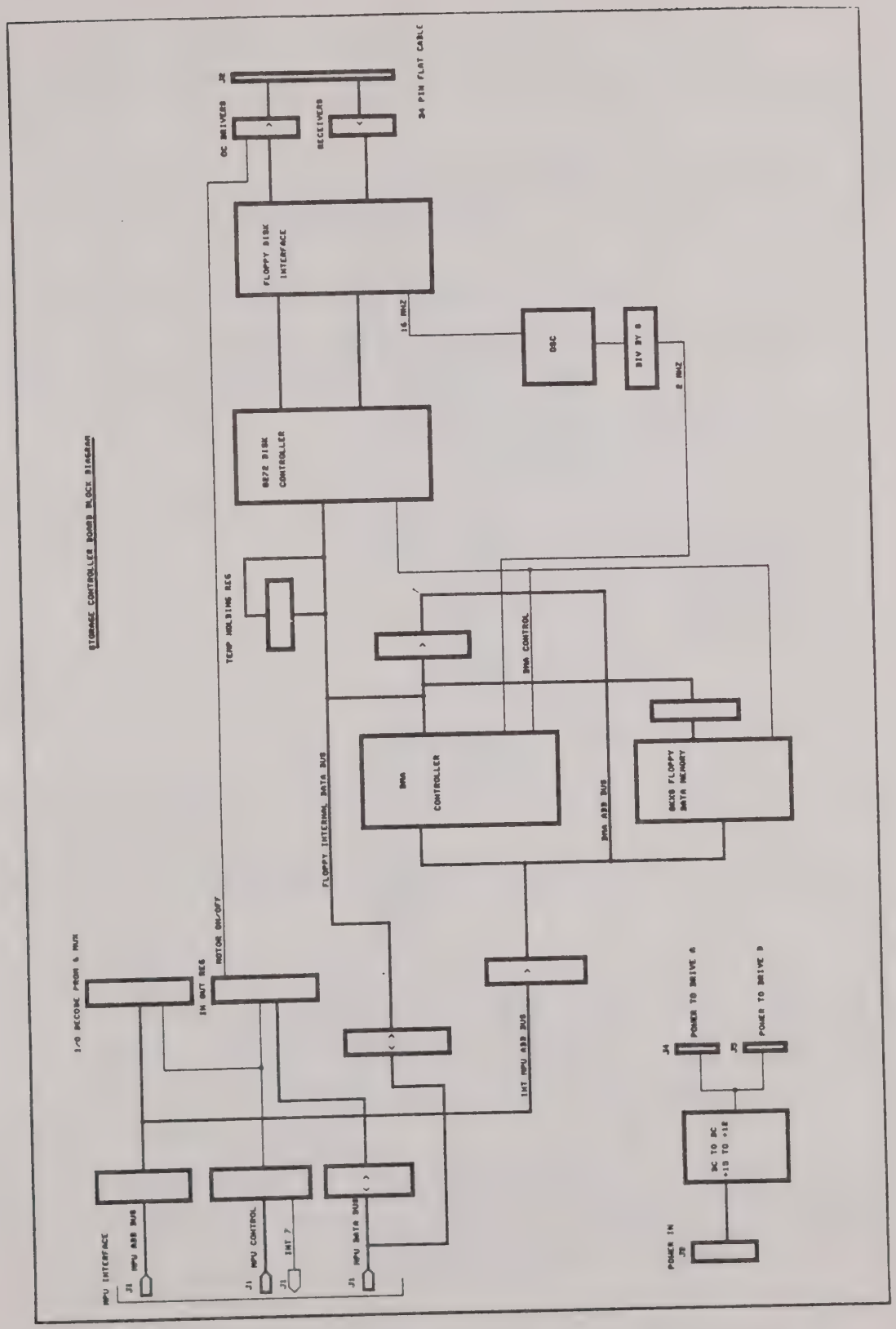


Figure 4-8. K450B Storage Controller Board Block Diagram

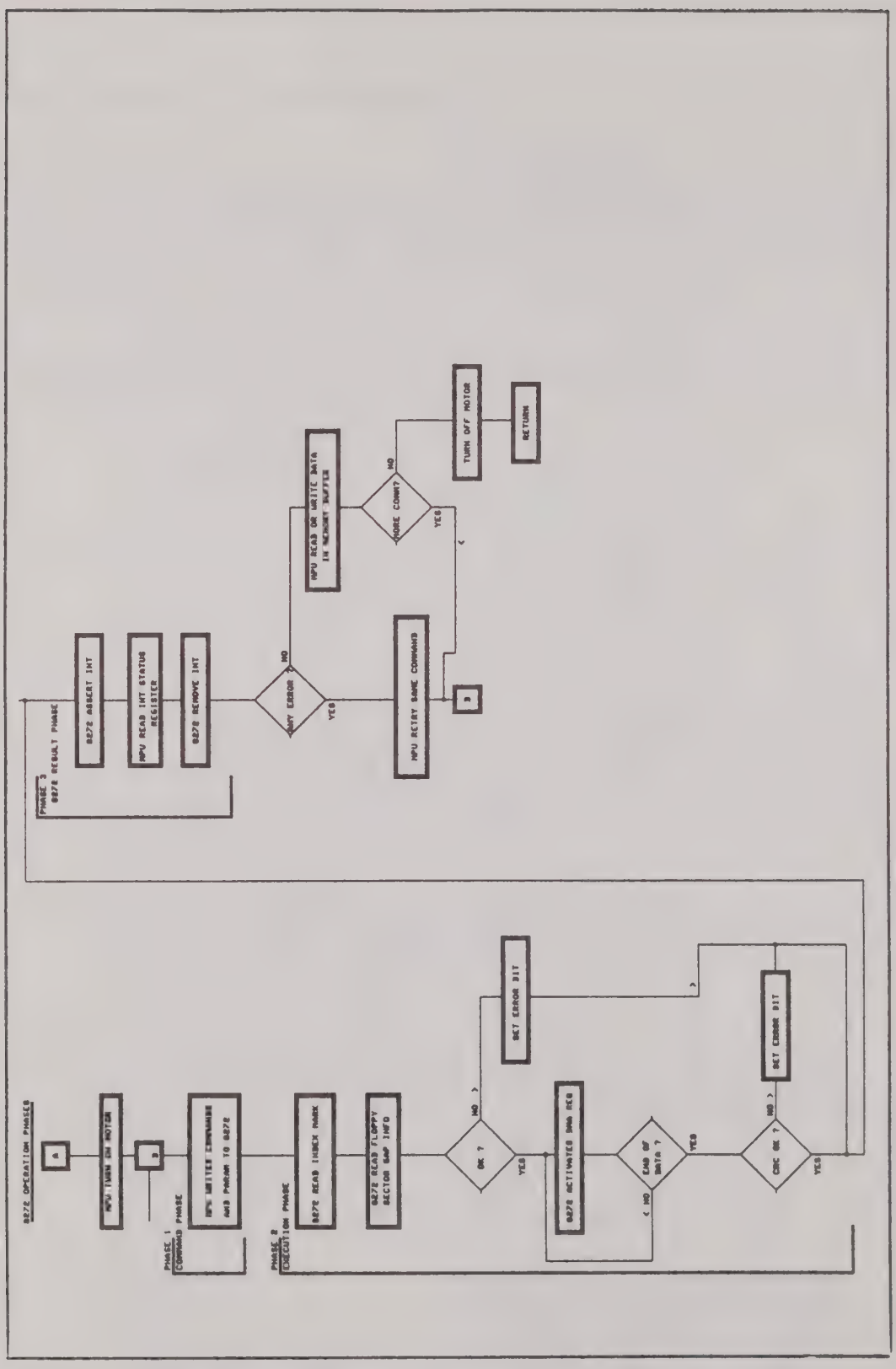


Figure 4-9. Storage Controller Operation Phases

The sequence of events for completing a data transfer operation is as follows:

The MPU Board initiates the Command Phase by issuing a command to the 8272. Each command contains seven parameters which are described in the 8272 Data Sheet. The command specifies the type of operation to be performed.

The 8272 begins the Execution Phase after the Command Phase is completed. The Execution Phase searches for Index from the disk drive and checks for Sector Number and Gap information. When these conditions are satisfied, DMA Request is activated by the 8272 to begin transferring data. Upon completion of data transfer, the 8272 issues the Interrupt (INT 7) signal to the MPU.

The INT 7 signal notifies the MPU to begin the Result Phase. The MPU reads the Interrupt Status Register of the 8272 to determine if the operation terminated successfully (or unsuccessfully).

Drive Control Commands: All of the commands executed by the 8272 do not invoke data transfers, and therefore, do not follow the three operating phases described in previous paragraphs. The following commands are used to control drive functions prior to invoking data transfer:

1. Recalibrate Command --- Commands the drive to position the R/W head carriage at track 0 by sensing the Track 0 signal
2. Seek Command --- Command to activate Step signal to drive
3. Specify Command --- Command is issued once after Power On to specify drive * characteristics as follows:

    a. Head Unload Time (HUT)

    b. Step Rate Time (SRT)

    c. Head Load Time (HLT)

    * Parameter value for drive characteristics is specified by the drive manufacturer

Power On Initialization Sequence: The Power On initialization sequence for Storage Controller Board hardware operation is presented in Figure 4-10.

VLSI Floppy Disk Interface Chip: The 9201 VLSI peripheral chip (Schematic Sheet 2, location 1A) is driven by firmware and is not programmable by the software. The following circuit functions are performed by this chip:

1. Clock data separator and digital phase locked loop circuit
2. Clock dividers and data window generator circuits
3. Write window and write precompensation generator circuits
4. Drive select and head load open collector driver circuits

DMA and Memory Operation Data Flow

The Storage Controller Board uses the 8257-5 DMA Controller chip (Schematic Sheet 2, location 1E). Channels 2 and 3 are used for DMA transfers. Channel 2 is used to transfer data between memory and the MPU. Channel 3 is used to transfer data between memory and the 8272 Floppy Disk Controller (location 1C).

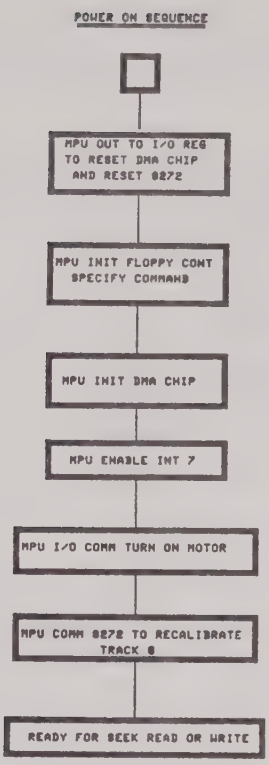


Figure 4-10. Storage Controller Board Power On Sequence

The MPU initializes the 8257-5 to program the address and record length for the amount of data bytes being transferred. The required DMA is enabled, and a command is issued to the 8272 Floppy Disk Controller. The 8272 then issues a DMA request to the 8257-5 DMA Controller (see Figure 4-8). The 8257-5 responds to acknowledge the DMA Request and selects the memory source address and control lines as described in subsequent paragraphs.

The control lines for MEMRD* and IOW* are selected if the DMA transfer occurs from memory to I/O for a disk write operation.

The control lines for IORD* and MEMWR *are selected if the DMA transfer occurs from I/O to memory for a disk read operation.

The DMA transfer occurs via the internal bus network on the Storage Controller Board, 8272 Floppy Disk Controller internal data bus, and the 8257-5 DMA Controller internal address bus (see Figure 4-8).

Transfer of the last data byte is flagged by the 8257-5 DMA Controller Terminal Count (TC) signal. When the TC signal is recognized by the 8272 Floppy Disk Controller, no further DMA cycles are requested. The 8272 then performs a read of the two Cyclic Redundancy Check (CRC) bytes.

Power and Clock Generation Circuits

The power circuit on the Storage Controller Board is a +15 to +12 Vdc Fixed Voltage Regulator that is supplied to the disk drives. The power input connector is J3 and the two power output connectors are J4 and J5. The disk drive signal connector is J2 which is connected to a 34-pin, flat ribbon cable. Refer to the drive manufacturer's manual for descriptions of pin-out signals.

The Storage controller Board contains a 16 MHz crystal oscillator (74LS04, 4B and Y1) that generates a 16 MHz clock signal to the 9201 Floppy Interface chip(schematic sheet 3 location 1A). A divide-by-eight circuit (location 4F) generates a 2 MHz clock signal for the 8257-5 DMA Controller chip.

Chapter 5

DISK DIAGNOSTICS

INTRODUCTION

The K450B Diagnostic Operating System, (DIAG), Part Number 0121-0485-10, is the "User Interface" or "Front End" for the K450B Disk Diagnostics. The main functions that it performs are as follows:

DIAG provides a menu for the operator to enter options and parameters.

DIAG allows the operator to run the Diagnostics with certain options. The individual Diagnostic modules use these options to determine program flow and operation.

These options include which boards in the System are to be tested, the number of times to Repeat each test, Halt Diagnostic Execution Upon Error, Loop Diagnostic Execution upon Error, Test Floppy Disk Drive A or B, Test Floppy Drive Side 0 or Side 1, Display Error Messages or suppress messages, and Allow Operator Interaction of the Diagnostics. These options and parameters will be explained in a later section.

DIAG loads Diagnostic modules from Disk and executes them. The Diagnostic modules consist of six programs on the K450B Disk, and are loaded in one at a time, and executed. Due to the size of the modules, (up to 40k in length), and the limited RAM space available, (64k), it would be impossible for all of the code required to test the K450B, to be resident in memory at once.

So when DIAG is testing a particular board, the appropriate Diagnostic module is then loaded in from the Disk and executed. These Diagnostic modules will be discussed in a later section.

DIAG provides Pass/Fail History information.

DIAG keeps a tabulation of each time a test is executed, and whether it Passed or Failed. This information is accumulative, so if the Diagnostic is run for a long time period, the Pass/Error information is a total representation of all Passes and Errors.

NOTE:

The maximum number of Passes and Errors DIAG can log is 65,535. If the Error count reaches this limit, it will not wrap around to 0, rather DIAG will stop incrementing this count.

STARTING UP THE K450B DIAGNOSTICS

CAUTION

Prior to using the K450B Master Diagnostic Disk, it is recommended that the user format and copy the master disk as described in the K450B User's Manual. Store the master disk and use the duplicate as a backup to avoid possible damage to the original. Ensure the duplicate disk is write protected to prevent inadvertent writing which could destroy data.

When The K450B Logic Analyzer is powered on, it will perform it's power on self test Diagnostics. Assuming these have Passed, the Logic Analyzers's default menu will be displayed.

To boot up the Disk Operating System, insert the mini Floppy Diskette into Disk Drive A with the Write protect tab nearest to the activity light, and close the door on the Drive.

Press the "I/O" key, then press "1". This will "boot up" the Disk Operating System and the screen display should change to show the directory contents of the Diskette. The following files should be in the display:

K450D -XX.EXE	(K450B Diagnostic Operating System)
KDDIAG-XX.EXE	(Keyboard/Display Diagnostic Module)
DBDIAG-XX.EXE	(Data Board Diagnostic Module)
CBDIAG-XX.EXE	(Control Board Diagnostic Module)
CKDIAG-XX.EXE	(Clock Board Diagnostic Module)
THDIAG-XX.EXE	(Threshold/GPIB Board Diagnostic Module)
SCDIAG-XX.EXE	(Storage Controller Diagnostic Module)

Where: XX represents the current version of the Diagnostic Software.

Other files may be listed, but are irrelevant to the Diagnostics.

KDDIAG, DBDIAG, CBDIAG, CKDIAG, THDIAG and SCDIAG are all Diagnostic modules and are not executable as stand alone programs. They are all loaded in and executed by K450D-11.EXE. If a "RECALL" is done on one of these modules, the K450B will lock up. The power will have to be removed and then restored.

To load the K450B Diagnostic, press the NEXT key until the DOS "RECALL" selection appears. Press the right arrow key to enter the filename field. Press the down arrow key until K450D-11.EXE is highlighted. Press the F4 key. This will load DIAG from Disk and execute it. The K450B Diagnostic Main Menu will then be displayed.

MAIN MENU

The "main" menu is displayed upon booting up DIAG. This main menu has three main fields.

The top of the screen has a list of the keys, and a description of the function for each key. Throughout the Diagnostic execution, the top of the screen will have a list of keys. The keys listed and the functions of these keys will vary, depending on the particular state or menu the Diagnostic is in.

The lower-right side of the screen has a list of the "Active" boards in the system. When DIAG began to run, it peeked out to see which boards were installed in the K450B chasis motherboard. The boards that it found were marked "Active", and these are the boards that it will test.

The lower-left side of the screen has a list of the "Inactive" boards, or the boards that are not present in the system. Some boards are optional, and since DIAG was written to test all possible components of a K450B system boards that are not present are displayed as "Inactive", specifying that these boards will not be tested.

NOTE:

The "Active" and "Inactive" status can be forced or overridden. If, for example, a board is actually present in the system, but you do not wish DIAG to test it, you can force it to become Inactive by positioning the cursor with the up or down arrow keys next to the name of the board, and press the left arrow key. This will place this board into the Inactive side. This can be done for any or all boards.

Boards that are flaged as "Inactive" can be forced to become "Active" by positioning the cursor using the up or down arrow key, next to the name of the board and pressing the right arrow key. This would be useful if a board is actually in the system but is faulty, and caused it to appear in the "Inactive" status when DIAG started up. The board can be forced "Active" and tested.

Of course, if a board is not installed in the system, and it is forced to be "Active" when the Diagnostic is run, it will Fail and give you non relevant information.

SYSTEM TESTING (All Active Boards)

When DIAG is started and the Main Menu is displayed, the Active/Inactive/Test››› cursor will be pointing to "All Active Boards". If the NEXT key is pressed, all of the tests for all of the boards in the "Active" list will be automatically tested sequentially.

Before each test is executed it will be loaded in by DIAG and the message "Loading Diagnostic File" will be displayed. The name of the current Diagnostic module will be displayed at the top and the test names and test steps will be updated.

During this automatic testing, DIAG will display the number of Passes and Errors at the bottom of the screen. If there are any Errors, an Error message will be displayed at the center of the screen, and the Error count at the bottom of the screen will be incremented.

The Pass counter at the bottom of the screen will not be incremented until all tests for all Active boards are performed.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current test and return to the Main Menu.

System Testing is normally performed if an overall picture of the unit's integrity is desired. Since all Subtests for all Active boards will be performed, this testing will take quite a while.

SINGLE BOARD TESTING.

If a single board is to be tested, the Test››› cursor should be positioned next to the name of the board and the NEXT key pressed. This method is different than testing "All Active Boards" in several ways.

First the testing is performed only on the chosen board.

Second, the testing is not started automatically. The Subtest Menu list for that particular Board will be displayed, and either all Subtests can be executed, or a single Subtest can be executed.

Third the Pass and Error count is not displayed at the bottom of the screen.

Single Board testing is done when the integrity of a single board or boards is unknown, and a direct test on the board in question is performed. This method provides information at a quicker rate than if all the previous boards in the Active list are tested.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current Subtest and return to the Subtest Menu.

CONDUCTING ALL SUBTESTS OR INDIVIDUAL SUBTESTS

When a single board is selected for testing, the Subtest Menu is displayed. A single Subtest can be performed by positioning the highlighting cursor, using the up or down arrow keys, over the desired test and pressing the NEXT key. The single Subtest will run, and then return to the Subtest Menu. If the parameter selection for NUMBER TO REPEAT TESTS is greater than 1, the particular Subtest will be repeated that number of times.

"ALL SUBTESTS" will execute all of the tests in the Menu sequentially, and return to the Subtest Menu when complete.

If at any time you wish to abort the Diagnostic execution, pressing the STOP key will abort the current Subtest and return to the Subtest Menu.

Pressing the PREVIOUS key will return you to the Main Menu.

DIAGNOSTIC PARAMETERS (EDIT KEY)

There are a number of options or parameters for the execution of the Diagnostic modules. These parameters control the program flow of execution. The parameters can be displayed and/or changed at any time by pressing the EDIT key. This will display the list of parameters, and the current selections. Once the parameter options are selected, pressing the PREVIOUS key will return to the previous Menu Display or program execution.

The parameters are changed by positioning the highlighting cursor next to the desired parameter and pressing the NEXT key. This will select the opposite of the currently displayed option, i.e. YES changes to NO. This method is valid for all parameters except the Times to Repeat Test, which will be explained later.

The parameters are as follows:

Parameter	Options	
1. Halt on Error	No, Yes	(default is No)
2. Loop on Error	No, Yes	(default is No)
3. Display Error Messages	Yes, No	(default is Yes)
4. Times to Repeat Test(s)	1 - 65535	(default is 1)
5. Test Floppy Disk Drive A	No, Yes	(default is No)
6. Test Floppy Disk Drive B	Yes, No	(default is Yes)
7. Test Side 0 of Drive(s)	Yes, No	(default is Yes)
8. Test Side 1 of Drive(s)	Yes, No	(default is Yes)
9. Run Operator Action Tests	No, Yes	(default is No)

Halt on Error

The first parameter, Halt on Error, specifies that if during the execution of the Diagnostic an Error occurs, the Diagnostic will temporarily halt and the Error message will remain on the screen. A "HALTED ON ERROR" message will be blinking to verify that the Diagnostic is halted. Diagnostic execution can be resumed by pressing the NEXT key. If another Error occurs, DIAG will halt again, until the NEXT key is pressed.

Normally when there is an Error, and the Halt on Error parameter is not selected, the Error message is displayed on the screen for about a second. This doesn't allow adequate time to read all of the information displayed, so Halt on Error is useful for "single stepping" through the Errors that occur.

The disadvantage of Halt on Error is that when an Error occurs, all testing is suspended, and the NEXT key must be entered to resume. In the case where you want a unit to run the Diagnostics for a period of time without the need of operator actions, and then later check on the number of Passes and Errors. Halt on Error should be disabled by setting the option to "NO".

Loop on Error

Loop on Error specifies that if during the execution of the Diagnostic an Error occurs, the Diagnostic will loop on the test step that found an Error. This test step will be repeated continuously even if it occasionally Passes.

The Loop on Error option is useful for debugging a board. If for example a board is intermittantly Failing, the continuous looping allows the operator to trigger on a Write pulse, a Read pulse or a clock.

The looping will continue until either the CONTROL key is pressed, or the Loop on Error option is disabled by pressing the EDIT key, and changing the selection to "NO".

NOTE 1:

The CONTROL key is mainly used during the process of Looping on Error. Pressing the CONTROL key "skips" out of the current Test Step and proceeds to the next Test Step. It provides a means to quickly abort a Test Step without changing the Loop on Error Parameter.

NOTE 2:

The Loop on Error option has one characteristic than could be confusing. If for example the option is enabled and an Error occurs, the Error message will be displayed as usual, and the test will be repeated. However, if the Error message is only displayed for about a second, and then the test starts Passing, the Diagnostic may appear to hang since no messages are being displayed and the Test Step number remains constant.

The Diagnostic is not hung up, it is in fact repeating the same Test Step without Error. Pressing the CONTROL key, or disabling the Loop on Error Parameter will allow Diagnostic execution to proceed.

Display Error Messages

This parameter controls whether or not the Error messages will be displayed when Errors occur.

Normally when an Error occurs, and this option is set to YES, a message describing the Error is displayed for about a second, then the message is cleared. For most testing cituations this is desired.

If a test is running that is rather lengthy, such as a RAM addressing test, and there are many Errors, the screen will display many Error messages. Each time a messages is displayed the Diagnostic is paused, and this actually increases the Total Test Time. If the Display Error Messages is set to NO, this will decrease the Total Test Time.

If the unit is to be run unattended, (i.e. it is not necessary to view every Error message), and the maximum number of test cycles desired, this parameter should be set to NO. The total number of Errors can be displayed at a later time by pressing the DATA key.

NOTE:

When the Display Error Messages is set to NO, the Diagnostic module that is currently executing still calls the Error tabulation routine, so that every Error is counted and tabulated.

Number of Times to Repeat Test(s)

This parameter controls the number of times a test is performed. The default is 1. This means when the test or tests are started by pressing the NEXT key, it/they will be executed one time and the Diagnostic will then pause.

If several test repeats or continuous testing is desired, any number from 1 to 65,535 can be selected. Enter this parameter by positioning the cursor, pressing the NEXT key, entering a number with 1 to 5 digits, and again pressing the NEXT key. (If 5 digits are entered, the terminating NEXT key need not be pressed).

For example if the count desired is 158, press NEXT, 1, 5, 8, NEXT. If a number larger than 65,535 is entered, the program will complain and ask you to re-enter the number.

NOTE:

If the repeat count is more than one, the DIAG will cycle through all Subtests of all Active boards and then repeat the cycle until the repeat count has been reached.

At any time during this execution, the DATA key may be pressed to view the Pass/Error history then the PREVIOUS key will resume execution. The EDIT key may also be pressed to change any of the parameters. The PREVIOUS key will then resume execution.

Test Floppy Disk Drive A, Test Floppy Disk Drive B.

This parameter refers to the Floppy Disk Drive tests for Disk Drives A and B. If a Drive is selected a Disk Write/Read test will be performed on that Drive, and a "scratch" Disk must be used since all data on that Disk will be destroyed !

The default selections are Drive A = NO, Drive B = YES. The Diagnostic Disk is residing in Disk Drive A, and a "scratch" Disk should be residing in Disk Drive B. With the default selections, no operator actions are required. Drive B will be tested, and Drive A will not.

If both Disk Drives are to be tested, the parameter options must be changed to Drive A = YES, and Drive B = YES. Each time DIAG is ready to test Disk Drive A, the Diagnostic Disk will have to be removed, and a "scratch" Disk placed in the Drive. When the test is complete, the sratch Disk will have to be removed from Drive A, and the Diagnostic Disk re-inserted.

This procedure requires actions to be performed by the operator, and the RUN OPERATOR ACTIONS parameter must be enabled. This will be explained later

NOTE:

A "scratch" Disk is defined as a new or fairly new Floppy Diskette, that has been "formatted" using the K450B Disk Operating System Format command. The Write Protect slot must not be covered. The Disk used should not contain any important data or programs, since the process of Formatting and the Disk Drive testing distroys all data on the Diskette.

TEST SIDE 0, TEST SIDE 1

This parameter also refers to the Floppy Disk Drives testing. Each Disk Drive has two sides, Side 0 and Side 1. Normally parameters 7 and 8 will be YES, and both sides will be tested during the Floppy Disk testing.

If for example Disk Drive B is having Errors on Side 1, and no Errors on Side 0, setting the TEST SIDE 0 option to NO will allow for more frequent testing of Side 1 of the Disk Drive, and give more Pass/Fail information at a quicker rate.

RUN OPERATOR ACTION TESTS

Some of the tests in the Diagnostic modules require the operator to perform certain actions. One example is the testing of Disk Drive A requires the operator to remove the Diagnostic Disk and insert a "scratch" Disk, allow the test to run, then re-insert the Diagnostic Disk.

Others might be the installation of RS-232 wrap-back connectors, the testing of the Keys on the K450B Keyboard, GPIB Testing, etc.

If a unit is to run the Diagnostics unattended, this parameter should be set to NO, and the specific tests that require operator actions will not be performed.

PASS/ERROR TABULATION (DATA KEY)

At anytime during the Diagnostic Execution the number of Passes and Errors can be displayed by pressing the DATA key. Pressing the PREVIOUS key will return to the previous Menu or executions. A list of the boards in the system will be displayed, as well as the total number of Errors as follows:

```
Number of Errors
Cycle Through All Tests

Keybd/Display          0
Data Board AB          0
Data Board CD          0
Data Board E           0
Control Board          0
Clock Board            0
Threshold Bd.          0
Storage Cont.          0
```

There are two fields that are highlighted by the cursor, they are "Errors" and "Cycle Through All Tests". If the cursor is over Errors, pressing the NEXT key will change the display to the number of Passes, (changing Errors to Passes). Pressing the NEXT key again will change back to the Error display.

This Errors/Passes display shows the total accumulative Errors and Passes for each board in the K450B System. If a board is not in the system, or it was forced Inactive, the Pass and Error count will be 0 for that board. Otherwise the number of times DIAG tested the board will be displayed for the Passes, and the total number, (if any), of Errors will be displayed.

If the down arrow key is entered this will move the cursor into the "Cycle Through All Tests" field, and pressing the NEXT key will display the total Errors/Passes for each Subtest of the Keyboard/Display Board. Pressing the NEXT key will then display the total Errors/Passes for each Subtest of Data Board AB.

Consecutive pressing of the NEXT key will display the Data Board CD, Data Board E, Control Board, Clock Board, Threshold Board, Storage Controller Board, and then finally back to the Board Level Error/Pass Display.

If for example you wish to view to information about Data Board AB, do the following steps:

1. Press the DATA key to display the Board list and total Error count.
2. Press the NEXT key to display the Board list and total Pass count.
3. Press the down arrow key and press the NEXT key twice to display the Data Board AB Subtest Pass count.
4. Press the up arrow and then the NEXT key to display the Data Board AB Subtest Error count.
5. Press the PREVIOUS key to return to the previous Menu.

DIAGNOSTIC RE-INITIALIZATION AND DIAGNOSTIC EXIT TO SYSTEM

When the Diagnostic Modules are executed, the Pass/Fail information is accumulated and pressing the DATA key will display this information.

If a "fresh" start of the Diagnostic is desired, with the Pass/Error information set to 0, this can be achieved by entering the Main Menu by pressing the PREVIOUS key, and then pressing the PREVIOUS key again. This sets up the default Parameters, and resets all Pass/Error information to 0.

NOTE:

BE CAREFUL using the PREVIOUS key while in the Main Menu, as it would be easy to re-initialize the Diagnostic by accident, and loose all the Pass/Error information that has accumulated.

EXITING THE DIAGNOSTIC

When the K450B Logic Analyzer is powered on, it goes through it's power on Diagnostics and comes up in the Default Menu. While in this menu, if you press the "F2" key, the power on diagnostics are run once again.

While the K450B Diagnostic Operating System is under Execution, it is possible to exit back to the Default Menu of the Logic Analyzer. This is done by pressing the "F2" key three consecutive times. This will cause any Diagnostic execution to be aborted, and the K450B will go through the power on diagnostics and come up in the Default Menu.

Pressing the "F2" key three consecutive times has the same effect as powering off the K450B, and restoring power, without the need for removing the Floppy Diskettes.

NOTE:

The "F2" key must be pressed three consecutive times to avoid an accidental exit from the Diagnostic Operating System. Any other keys pressed between the three "F2" keys voids out the exit.

SUMMARY OF K450B DIAGNOSTIC OPERATING SYSTEM KEYS

The K450B Diagnostic will recognize the following keys:

Key	Menu or Execution	Function
NEXT	Main Menu	Execute Diagnostic.
	Subtest Menu	Execute Diagnostic.
	HALTED ON ERROR	Resume Diagnostic execution.
	Parameter Menu	Change selected option.
	Pass/Error Display	Change Error display to Pass display, Cycle through Subtest lists.
PREVIOUS	Main Menu	Re-initialize Diagnostic.
	Subtest Menu	Return to Main Menu.
	Parameter Menu	Return to previous Menu or execution.
	Pass/Error Display	Return to previous Menu or execution.
EDIT	Any Menu or execution	Display the Parameter options.
DATA	Any Menu or execution	Display the Pass/Error information.
STOP	Any execution	Abort current test.
	HALTED ON ERROR	Abort current test.
FIELD (arrows)	Main Menu	Activate/Inactivate a Board, or Select a Board for testing.
	Subtest Menu	Select a Single Test or all Tests.
	Parameter Menu	Select a parameter.
	Pass/Error Display	Change fields for Errors/Passes, or cycle through all Subtest lists.
CONTROL	Looping on Error	Skip out of current Subtest and proceed to the next Subtest.
F2	Any Menu or execution	Three consecutive key-strokes causes an EXIT from the Diagnostics and cold starts the K450B Logic Analyzer

KEYBOARD/DISPLAY BOARD DIAGNOSTIC TEST

DIAGNOSTIC OVERVIEW

This section describes subtests that are executed on the K450B keyboard/display board, how error reporting is done, and the concept behind each subtest program.

There are eight subtests written for the keyboard/display board. Each of these subtests are described individually on the following pages. Loop on error, error count, and pass count update are incorporated into each subtest. Details about interfacing to the diagnostic monitor can be found in the diagnostic monitor description.

All error messages are preceded by a "*" while information messages will use the ">" prefix. Early exit of each subtest is accomplished by pressing the "STOP" key.

Assumtions: This series of tests assumes that the following boards are installed and are operational:

1. MPU
2. Threshold
3. Clock
4. Control

SUBTEST CATEGORIES

1. Keyboard Test
2. Interrupt Controller (8259) Test
3. Clock/Calendar (5832) Test
4. Video RAM Data Test
5. Video RAM Address Test
6. 6164 RAM Data Test
7. 6164 RAM Address Test
8. Beeper Exercise

ERROR COUNT CATEGORIES

1. Subtest 1 Error Count
2. Subtest 2 Error Count
3. Subtest 3 Error Count
4. Subtest 4 Error Count
5. Subtest 5 Error Count
6. Subtest 6 Error Count
7. Subtest 7 Error Count
8. Subtest 8 Error Count

Keyboard/Display Diagnostic Subtest 1

TITLE: KEYBOARD TEST

TARGET LOGIC:
8E,14E,13E,10E
and keyboard interface matrix

PURPOSE:

The keyboard logic is functionally tested by pressing a specified key on the front panel, reading the corresponding I/O port from buffer (10e), and then verifying the key data to the expected data.

TEST DESCRIPTION:

There are 48 keys on the front panel; the corresponding I/O Port 1xh is arranged as follows:

a. x=0 if key is located at column 1 in the front panel
b. x=2 if key is located at column 2 in the front panel
c. x=4 if key is located at column 3 in the front panel
d. x=6 if key is located at column 4 in the front panel
e. x=8 if key is located at column 5 in the front panel
f. x=a if key is located at column 6 in the front panel
h. x=c if key is located at column 7 in the front panel
i. x=e if key is located at column 8 in the front panel.

There are 6 key data read from the buffer (10e),they are arranged as follows

a. the key data read=feh if the key is located at row 1 in the front panel
b. the key data read=fdh if the key is located at row 2 in the front panel
c. the key data read=fbh if the key is located at row 3 in the front panel
d. the key data read=f7h if the key is located at row 4 in the front panel
e. the key data read=efh if the key is located at row 5 in the front panel
f. the key data read=dfh if the key is located at row 6 in the front panel

The following information message is displayed before each key is tested:

>Press key labeled: ????????????

Where ???????????? could be 1 character, for example, "0" through "9", "a" through "f", or up to 13 characters, for example, "TRACE CONTROL" in the domain of 48 defined keys.

TEST STEP INFORMATION:

Test Step	Key Tested
1	NEXT
2	PREVIOUS
3	FORMAT
4	CLOCKS
5	TRACE CONTROL
6	ARM MODE
7	UP ARROW
8	LEFT ARROW
9	MEM A
10	DATA
11	TIMING
12	GRAPH
13	RIGHT ARROW
14	DOWN ARROW
15	MEM B
16	A->B
17	SEARCH
18	COMPARE
19	CONTROL
20	REF
21	C
22	8
23	4
24	0
25	SHIFT
26	HELP
27	D
28	9
29	5
30	1
31	I/O
32	"X"
33	E
34	A
35	6
36	2
37	EDIT
38	INS
39	F
40	B
41	7
42	3
43	ARM
44	STOP
45	F1
46	F2
47	F3
48	F4

ERROR MESSAGE:

If a key data error occurs, the following message is displayed:

```
*Test FAILED--Test Step    ss
 Keyboard Error
 Expected Keycode    = eeh
 Keycode Found       = ddh
 Key Data Code Read = "????????????"
```

where ss should be 1 through 48
ee should be 1 through 48
dd should be be 1 through 48

Keyboard/Display Diagnostic Subtest 2

TITLE: INTERRUPT CONTROLLER TEST

PURPOSE:

The interrupt logic is functionally tested by selecting each interrupt on the 8259 controller and causing each interrupt to occur. As each interrupt is generated, the 8259 receives the interrupt then outputs a vector for the 8086 processor. At these vectors are routines which set diagnostic flags. These flags are examined to determine if the interrupt actually took place. The source of the interrupts are then turned off, and the flags are cleared. After a small amount of time the flags are re-examined to determine if the source of the interrupt has actually been disabled. If a flag is found to be set then an error message is displayed.

TARGET LOGIC: 4E,2E,8E,10E
8D,9D,10D

TEST DESCRIPTION:

The following table indicates the interrupt source and line for the diagnostic test step:

TEST STEP INFORMATION:

Test Step	Interrupt from	on board	Interrupt Line
1	GPIB	Threshold	intr 1
2	RS-232	Threshold	intr 2
3	AUX	Threshold	intr 3
4	Total trace time clock (timer #0)	Clock	intr 4
5	simulated from software		not currently assigned
6	Time of day	Display	intr 6
7	Disk	Storage Controller	intr 7

ERROR MESSAGE:

If an error occurs, the following messages are displayed:

```
*Test FAILED--Test Step   z
Intr 0z Not Generated.
```

where z = 1 - 7

```
*Test FAILED--Test Step   z
Unexpected Interrupt 0z Generated.
```

where z = 1 - 7

Keyboard/Display Diagnostic Subtest 3

TITLE: CLOCK/CALENDAR TEST

PURPOSE:

This subtest verifies operation of the 5832 clock/calendar by saving the current time, then exercising the component by setting the time. The time is then read back and verified. If the test is successful, it indicates proper operation of the 5832.

The time is set so that the next second will cause a rollover. An example of a rollover is if the minutes counter was set to 59. When minutes are advanced then the minutes counter becomes zero and the hours count is incremented by one. This rollover process continues until the years counter rolls over to 00 (from 99).

TARGET LOGIC: 2D,2E,3D,4D,5D,7D

TEST DESCRIPTION:

Operations are exercised on the clock calendar components according to the following table:

TEST STEP INFORMATION:

Test Step	Operation
1	Read current time, save for last step
2	Set clock to: Jan. 1, 1900 @00:00:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @00:01:00
3	Set clock to: Jan. 1, 1900 @00:59:00 Using test feature on 5832 simulate 60 seconds. Read time: Compare to: Jan. 1, 1900 @01:00:00

```
4 ------------ Set clock to: Jan. 1, 1900 @23:59:00

                Using test feature on 5832 simulate
                60 seconds.

                Read time:
                Compare to:  Jan. 2, 1900 @00:00:00

5 ------------ Set clock to: Jan. 31, 1900 @23:59:00

                Using test feature on 5832 simulate
                60 seconds.

                Read time:
                Compare to:  Feb. 1, 1900 @00:00:00

6 ------------ Set clock to: Dec. 31, 1900 @23:59:00

                Using test feature on 5832 simulate
                60 seconds.

                Read time:
                Compare to:  Jan. 1, 1901 @00:00:00

7 ------------ Set clock to: Dec. 31, 1999 @23:59:00

                Using test feature on 5832 simulate
                60 seconds.

                Read time:
                Compare to:  Jan. 1, 1900 @00:00:00
```

NOTE:

Exiting this test via the stop key will restore the time saved in step 1. If power is removed during steps 2 - 7, the time will be lost.

ERROR MESSAGE:

If the time read does not match the time expected the following error message is displayed:

```
*Test FAILED--Test Step          x
Clock/Calendar Error
          year month  day hour  minute  second
Expected: aaa  bbb    ccc ddd   eee     fff
    Read: ggg  hhh    iii jjj   kkk     lll
```

where aaa, ggg = 000 - 999
bbb, hhh = 001 - 012
ccc, iii = 001 - 031
ddd, jjj = 000 - 023
eee, kkk = 000 - 059
fff, lll = 000 - 059

Keyboard/Display Diagnostic Subtest 4

TITLE: VIDEO RAM DATA TEST

PURPOSE:

This subtest verifies that the Keyboard/Display Board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A,7B,7C,8A,8B,8C,9A,9B,9C,10A,10B
dedicated RAM on MPU used for video,

TEST DESCRIPTION:

Although the RAM under test is on the MPU board, the display board uses this memory to create an image sent to the screen. Various data patterns are written to the MPU memory and read back. The data written is compared to the data read. If a miscompare is detected, an error message is displayed. This continues until all the data patterns listed below have been tried.

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

Note: this memory physically starts at 0100h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
        * Test FAILED--Test step   xx
        RAM Data Error
        Value Written = aaH
        Value Read    = bbH
        Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 5

TITLE: VIDEO RAM ADDRESS TEST

PURPOSE:

This subtests verifies that the Keyboard/Display board does not prevent normal operation of the MPU RAM dedicated to video display.

TARGET LOGIC: 7A,7B,7C,8A,8B,8C,9A,9B,9C,10A,10B
RAM located on mpu used for video,

TEST DESCRIPTION:

All of the RAM in this test is preset to zero then the indicated address is written with the value 0FFH. All of RAM is then read to verify that the indicated address is the only data element that was set to 0FFH.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

Note: this memory physically starts at 0100h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
* Test FAILED--Test Step     xx
RAM Data Error
Value Written = FFH
Value Read    = bbh
Address Count = cccch
```

where aa = 00 - ff
bb = 00 - ff
cccc = 0000 - 3fff

Keyboard/Display Diagnostic Subtest 6

TITLE: 6164 RAM DATA

PURPOSE:

This subtest verifies the operation and integrity of the 6164 RAMs on the Keyboard/Display Board by writing to the memory several different data patterns. This memory is then read back and compared to the value written. If a miscompare occurs then an error message is displayed. This process is repeated for all of the 6164 memory until all the patterns listed below have been tried.

TARGET LOGIC: 1B,3B,3C,4C,5B,6B,5E,6E5C,6D,

TEST DESCRIPTION:

The following is a summary of the data written to the RAM during each test step:

TEST STEP INFORMATION:

Test Step	Value Written
1	00H
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

Note: this memory physically starts at 080000h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
* Test FAILED--Test Step   xx
RAM Data Error
Value Written = FFH
Value Read    = bbH
Address Count = ccccH
```

where aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 3FFF

Keyboard/Display Diagnostic Subtest 7

TITLE: 6164 RAM ADDRESS TEST

PURPOSE:

This subtest verifies the operation and integrity of the 6164 RAMs on the keyboard/display board. All of the RAM in this test is preset to zero then the indicated address is written with the value 0FFH. All of RAM is then read to verify that the indicated address is the only data element that was set to 0FFH.

TARGET LOGIC:

1B,3B,3C,4C,5B,6B,5E,6E5C,6D,

TEST DESCRIPTION:

All of the RAM in this test is preset to zero then the indicated address is written with the value 0FFH. All of RAM is then read to verify the written data.

TEST STEP INFORMATION:

Test Step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H
13	0800H
14	1000H
15	2000H

Note: this memory physically starts at 080000h

ERROR MESSAGE:

If an error occurs during this subtest the following message is displayed:

```
* Test FAILED--Test step    xx
RAM Data Error
Value Written = FFH
Value Read    = bbH
Address Count = ccccH

where  aa = 00 - FF
       bb = 00 - FF
     cccc = 0000 - 3FFF
```

Keyboard/Display Diagnostic Subtest 8

TITLE: BEEPER EXERCISE TEST

PURPOSE:

This subtest exercises the beeper circuitry. There are no error messages generated by this routine as there is no way to verfy operation except via audio monitoring.

TARGET LOGIC:

15E,16E,17E,18E

TEST DESCRIPTION:

The beeper is activated by loading p0-p3 on IC with the duration value then the line labeled cp is pulsed.

The beeper is set to various durations as given in the following table:

TEST STEP INFORMATION:

Test Step	Duration
1	0.1 sec
25	1.5 sec

ERROR MESSAGE:

There are no error messages for this subtest. Also note that since no errors are possible, "loop on error" and "halt on error" do not function

DATA BOARD DIAGNOSTIC TEST

DIAGNOSTIC OVERVIEW

This document describes the subtests that are performed by the K450B Data Board Diagnostic. The target hardware is presented, as well as a general description of each subtest, a list of information for each test step, and a description of Error Messages that may be printed.

The K450B Data Board Diagnostic is a board level test of the board's functionality, which runs under the K450B Diagnostic Operating System. It can test from 1 to 3 Data Boards in the system. These correspond to Data Boards AB, CD and E. Each subtest for Data Board AB and CD are run twice to check each section (A/B/C/D) separately.

In order for the Diagnostic to run properly, the board under test must be installed in the Mother Board (not on an extender card), and the internal probe input cables connected to J1 and J2 with external probes installed. All of the channels of all probes must be free from connection to anything (i.e. they must be allowed to float). Also, all of the other boards must be installed in the K450B system.

NOTE:

The internal probe input cables are too short for the board to be on and extender card. If extension cables are used, then an extender card may be used.

Several of the subtests use a sequence of 24 Data patterns to write, read and verify an I/O port or Memory Address. These Data patterns verify that all 16 Data Bits are functional and completely independent of each other.

These 24 Data patterns are:

0000H, 5555H, AAAAH, CCCCH, 3333H, 6666H, 9999H, FFFFH,
0001H, 0002H, 0004H, 0008H, 0010H, 0020H, 0040H, 0080H,
0100H, 0200H, 0400H, 0800H, 1000H, 2000H, 4000H, 8000H.

When writing these Data patterns to an I/O port such as the Sample Register or the Pipeline Registers, the Data value can be randomly accessed. The ECL RAM Memory on the other hand is essentially a 2048 byte FIFO. All 2048 locations are accessed at the same I/O address, (i.e. 086H for writes, and 080H for reads). The RAM's addressing is accomplished by sequential reads or writes from/to the RAM. Address counters on the board are incremented each time a RAM access (i.e. a Sample Clock) occurs.

The RAM actually requires 2051 Sample clocks to get 2048 words of data to the RAM. The three extra clocks are required to get the Data through the Pipeline. After the 2048th clock, the 2048th Data value resides in the Old Pipe Register. One more clock will shift it to the New Pipe Register. An additional clock will shift it to the Old Pipe Register. One last clock will write it to RAM.

NOTE:

When an I/O address is specified for explanation, the addresses for Data Board AB Section A are used. These addresses would only apply if Data Board AB was being tested. Data Board CD addresses are 09xH,0DxH, and Data Board E are 0AxH.

SUBTEST CATAGORIES

There are thirteen Subtests that are performed by the Data Boards Diagnostic. These are catagorized as follows:

1. Force Conditions Test
2. Data Path Test
3. Clocking Disable Test
4. Latch Bits 0-7 Test
5. Latch Bits 8-F Test
6. Glitch Bits 0-7 Test
7. Glitch Bits 8-F Test
8. Multiplex Select Test
9. Pipeline Shift Test
10. RAM Data Integrity
11. RAM Addr Integrity
12. Trace Conditions Test
13. Recirculate RAM Test

ERROR COUNT CATAGORIES

The Error Count Display information is a one for one match with the Subtest list above. The K450B Diagnostic Operating System will display the "Subtest n" instead of the actual test name.

Subtest 1 (Force Conditions Test)
Subtest 2 (Data Path Test)
Subtest 3 (Clocking Disable Test)
Subtest 4 (Latch Bits 0-7 Test)
Subtest 5 (Latch Bits 8-F Test)
Subtest 6 (Glitch Bits 0-7 Test)
Subtest 7 (Glitch Bits 8-F Test)
Subtest 8 (Multiplex Select Test)
Subtest 9 (Pipeline Shift Test)
Subtest 10 (RAM Data Integrity)
Subtest 11 (RAM Addr Integrity)
Subtest 12 (Trace Conditions Test)
Subtest 13 (Recirculate RAM Test)

Data Board Diagnostic Subtest 1

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC:

ALL SECTIONS	SECTIONS A,C,E	SECTIONS B,D
B5 B6	E9	E2
C5 C6 C7		
D5 D6 D7		
E6 E7		
F6 F7		
G6 G7		

TEST DESCRIPTION:

This subtest writes various commands to the Data board(s) and expects certain status values to exists. The commands are written to ports 082H and 084H, and the status is read back from port 088H.

The test does not require any boards other than the MPU to be installed in the system. Specifically, it requires no clocking from the Clock Board.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	65H
3	75H
4	F5H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 4.

hmsg is the Error heading message:
Not Halt, Mem full, ExpWrlow 02 Error
Multiphase Mode Clear Error
Async Mode Clear Error
Freeze Memory Clear Error

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 2

TITLE: DATA PATH TEST

TARGET LOGIC:

ALL SECTIONS					SECTIONS A,C,E	SECTIONS B,D
C6	C7	E7	F7	E6	E9	E2
D6	D7	G6	G7	F6		

TEST DESCRIPTION:

This subtest checks the Data Bus path of the Data Board for functionality and Data Bit uniqueness. Data is transferred by sending output to the Diagnostic Latch at I/O address 086H, issuing three Sample Clocks and receiving input from the Old Pipe Register at I/O address 082H, and comparing Data. Since the Glitch Mode and the Latch Mode are both disabled, Data will slip through to the Old Pipe Registers without the need of a Latch Clock.

The Clock Board is required for this test. The "Sample Clock"is used to clock the data to the Old Pipe Register. This is achieved by doing a "KICKSCLOCK", which writes a "1" to Data bit D0 of Write Register 8 (0B8H) of the Clock Board.

The majority of the subsequent subtests use this Data Path to exercise various features and functions of the Data Board. So if there are any errors in this test, there are bound to be many failures to follow.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	086H, Diagnostic Latch	082H, Old Pipe Register
2	5555H	086H, Diagnostic Latch	082H, Old Pipe Register
3	AAAAH	086H, Diagnostic Latch	082H, Old Pipe Register
4	CCCCH	086H, Diagnostic Latch	082H, Old Pipe Register
5	3333H	086H, Diagnostic Latch	082H, Old Pipe Register
6	6666H	086H, Diagnostic Latch	082H, Old Pipe Register
7	9999H	086H, Diagnostic Latch	082H, Old Pipe Register
8	FFFFH	086H, Diagnostic Latch	082H, Old Pipe Register
9	0001H	086H, Diagnostic Latch	082H, Old Pipe Register
10	0002H	086H, Diagnostic Latch	082H, Old Pipe Register
11	0004H	086H, Diagnostic Latch	082H, Old Pipe Register
12	0008H	086H, Diagnostic Latch	082H, Old Pipe Register
13	0010H	086H, Diagnostic Latch	082H, Old Pipe Register
14	0020H	086H, Diagnostic Latch	082H, Old Pipe Register
15	0040H	086H, Diagnostic Latch	082H, Old Pipe Register
16	0080H	086H, Diagnostic Latch	082H, Old Pipe Register
17	0100H	086H, Diagnostic Latch	082H, Old Pipe Register
18	0200H	086H, Diagnostic Latch	082H, Old Pipe Register
19	0400H	086H, Diagnostic Latch	082H, Old Pipe Register
20	0800H	086H, Diagnostic Latch	082H, Old Pipe Register
21	1000H	086H, Diagnostic Latch	082H, Old Pipe Register
22	2000H	086H, Diagnostic Latch	082H, Old Pipe Register
23	4000H	086H, Diagnostic Latch	082H, Old Pipe Register
24	8000H	086H, Diagnostic Latch	082H, Old Pipe Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Data Path Diag to Sample Reg Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 3

TITLE: CLOCK DISABLE TEST

TARGET LOGIC:

SECTIONS A,C,E		SECTIONS B,D	
A6	E9	E2	A6
A8	A11	A1	A4
B8	B11	B1	B4
C8	C11	C1	C4

All Logic listed in Subtest 2

TEST DESCRIPTION:

This subtest checks the different ways of clocking the Data Board, and the different ways of disabling the clocking.

In Single Phase Mode the Sample Clock, is used for all clocking on the Data Board. If the Multiphase Mode is selected, the Sample Clock, is used for the Sample Register, and the Control Clock, is used for the RAM, Pipelines and Address Counters.

A Condition called "Force Clocks" will cause all Sample Clocks and all Control Clocks to be ignored. Also a condition called "Halted" will disable these clocks.

This test also checks the Address Reset--Memory Full function. The address counters are reset by toggling W4B12. The Memory is "filled" by clocking the address counters 2048 times.

TEST STEP INFORMATION:

Step	Mode of Phase	Force Clocks	Data Expected
1	Single Phase	inactive	5555H
2	Multi Phase	inactive	AAAAH
3	Single Phase	active	0000H
4	Multi Phase	active	0000H

Step	"HALTED/"	MEMORYFULL	Status
5	high	low	0001H
6	low	high	0004H

Step	Mode of Phase	Force Clocks	Halt When Full	Data Expected
7	Single Phase	inactive	active	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 7.

hmsg is the Error heading message:

Force Clocks Enable Data move Error,
Force Clocks Disable Data move Error,
155 En2 Memory Not Full Status Error,
155 En2 Mem-Full/Halt Status Error,
Halt Freeze Old Pipe Register Error.

aaaa is the I/O address of the Data Board:

082H for Data Board AB Section A Old Pipe Register,
088H for Data Board AB Section A Status Register,
0C2H for Data Board AB Section B Old Pipe Register,
0C8H for Data Board AB Section B Status Register,
092H for Data Board CD Section C Old Pipe Register,
098H for Data Board CD Section C Status Register.
0D2H for Data Board CD Section D Old Pipe Register,
0D8H for Data Board CD Section D Status Register.
0A2H for Data Board E Section E Old Pipe Register,
0A8H for Data Board E Section E Status Register.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 4

TITLE: LATCH DATA BITS 0-7 TEST

TARGET LOGIC:

	SECTIONS A,C,E	SECTIONS B,D5F
	E9	E2

TEST DESCRIPTION:

This subtest checks the latch mode of latches of the lower 8 bits, with the upper eight bits in transparent mode. The Latch Clock 0-7 feeds the common Enable input. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The upper bits 8-F are not latched, the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Gate Arrays.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	086H, Diagnostic Latch	082H, Old Pipe Register
2	5555H	086H, Diagnostic Latch	082H, Old Pipe Register
3	AAAAH	086H, Diagnostic Latch	082H, Old Pipe Register
4	CCCCH	086H, Diagnostic Latch	082H, Old Pipe Register
5	3333H	086H, Diagnostic Latch	082H, Old Pipe Register
6	6666H	086H, Diagnostic Latch	082H, Old Pipe Register
7	9999H	086H, Diagnostic Latch	082H, Old Pipe Register
8	FFFFH	086H, Diagnostic Latch	082H, Old Pipe Register
9	0001H	086H, Diagnostic Latch	082H, Old Pipe Register
10	0002H	086H, Diagnostic Latch	082H, Old Pipe Register
11	0004H	086H, Diagnostic Latch	082H, Old Pipe Register
12	0008H	086H, Diagnostic Latch	082H, Old Pipe Register
13	0010H	086H, Diagnostic Latch	082H, Old Pipe Register
14	0020H	086H, Diagnostic Latch	082H, Old Pipe Register
15	0040H	086H, Diagnostic Latch	082H, Old Pipe Register
16	0080H	086H, Diagnostic Latch	082H, Old Pipe Register
17	0100H	086H, Diagnostic Latch	082H, Old Pipe Register
18	0200H	086H, Diagnostic Latch	082H, Old Pipe Register
19	0400H	086H, Diagnostic Latch	082H, Old Pipe Register
20	0800H	086H, Diagnostic Latch	082H, Old Pipe Register
21	1000H	086H, Diagnostic Latch	082H, Old Pipe Register
22	2000H	086H, Diagnostic Latch	082H, Old Pipe Register
23	4000H	086H, Diagnostic Latch	082H, Old Pipe Register
24	8000H	086H, Diagnostic Latch	082H, Old Pipe Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 5

TITLE: LATCH DATA BITS 8-F TEST

TARGET LOGIC:	SECTIONS A,C,E	SECTIONS B,D
	E9	E2

TEST DESCRIPTION:

This subtest is identical to the previous test except that the upper Data bits 8-F are tested instead of the lower bits 0-7.

This test verifies the latch mode of 10130 latches of the upper eight bits, with the lower eight bits in transparent mode. The Latch Clock 8-F feeds the common Enable input to the 10130's. This input is held high, and pulsed low to latch the current data from the "D" to the "Q". The Glitch is disabled so the other Enable input is held low. The lower bits 0-7 are not latched and the Data slips through the "D" to the "Q".

If there are any errors in this test, but the Data Path Test passed, the failure is probably in the Latch Clock or the 10130's.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	086H, Diagnostic Latch	082H, Old Pipe Register
2	5555H	086H, Diagnostic Latch	082H, Old Pipe Register
3	AAAAH	086H, Diagnostic Latch	082H, Old Pipe Register
4	CCCCH	086H, Diagnostic Latch	082H, Old Pipe Register
5	3333H	086H, Diagnostic Latch	082H, Old Pipe Register
6	6666H	086H, Diagnostic Latch	082H, Old Pipe Register
7	9999H	086H, Diagnostic Latch	082H, Old Pipe Register
8	FFFFH	086H, Diagnostic Latch	082H, Old Pipe Register
9	0001H	086H, Diagnostic Latch	082H, Old Pipe Register
10	0002H	086H, Diagnostic Latch	082H, Old Pipe Register
11	0004H	086H, Diagnostic Latch	082H, Old Pipe Register
12	0008H	086H, Diagnostic Latch	082H, Old Pipe Register
13	0010H	086H, Diagnostic Latch	082H, Old Pipe Register
14	0020H	086H, Diagnostic Latch	082H, Old Pipe Register
15	0040H	086H, Diagnostic Latch	082H, Old Pipe Register
16	0080H	086H, Diagnostic Latch	082H, Old Pipe Register
17	0100H	086H, Diagnostic Latch	082H, Old Pipe Register
18	0200H	086H, Diagnostic Latch	082H, Old Pipe Register
19	0400H	086H, Diagnostic Latch	082H, Old Pipe Register
20	0800H	086H, Diagnostic Latch	082H, Old Pipe Register
21	1000H	086H, Diagnostic Latch	082H, Old Pipe Register
22	2000H	086H, Diagnostic Latch	082H, Old Pipe Register
23	4000H	086H, Diagnostic Latch	082H, Old Pipe Register
24	8000H	086H, Diagnostic Latch	082H, Old Pipe Register

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Latch Data bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 24.

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 6

TITLE: GLITCH DATA BITS 0-7 TEST

TARGET LOGIC:	SECTIONS A,C,E	SECTIONS B,D
	E9	E2

All hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest checks the Glitch capture feature of the Data boards by enabling the Glitch capture circuitry which uses the "Set" and "Reset " functions of the latches. The individual Enable pins on the latches are held high so that any "clocking" from the Diagnostic Latch Clock is disabled (i.e. No effect).

Each output instruction to the Diagnostic bits port 086H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum of two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Oldpipe register after issuing three Sample Clocks. Another Sample Clock will present the Second Data to the Old Pipe Register.

In this test, only Data bits 0-7 are in the Glitch Mode. The upper bits 8-F slip through the latches because the enable pins are low.

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	0055H	0000H
4	00AAH	0000H
5	00CCH	0000H
6	0033H	0000H
7	0066H	0000H
8	0099H	0000H
9	00FFH	0000H
10	0001H	0000H
11	0002H	0000H
12	0004H	0000H
13	0008H	0000H
14	0010H	0000H
15	0020H	0000H
16	0040H	0000H
17	0080H	0000H
18	0000H	0000H
19	0000H	0000H
20	0000H	0000H

21	0000H	0000H
22	0000H	0000H
23	0000H	0000H
24	0000H	0000H
25	0000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 0-7 Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive OR of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 7

TITLE: GLITCH DATA BITS 8-F TEST

TARGET LOGIC:	SECTIONS A,C,E	SECTIONS B,D
	E9	E2

TEST DESCRIPTION:

This subtest is similar to the Glitch Data Bits 0-7 except the upper bits are being tested.

This test verifies the Glitch capture feature of the Data boards by enabling the Glitch capture circuitry which uses the "Set" and "Reset" function of the latches. The individual Enable pins on the latches are held high so that any "clocking" from the Diagnostic Latch Clock is disabled (i.e. No effect).

Each output instruction to the Diagnostic bits port 086H, latches the Data in the Glitch latches. A Sample Clock is required to send the Data through to the Sample Register. A maximum of two Data values may be output to the Diagnostic bits port before data overrun occurs.

The way that this circuitry is tested, is two consecutive Output instructions are performed with different Data. The first Data is checked at the Oldpipe register after issuing three Sample Clocks. Another Sample Clock will present the Second Data to the Old Pipe Register.

In this test, only Data bits 8-F are in the Glitch Mode. The lower bits 0-7 slip through the latches because both of the enable pins are low,

TEST STEP INFORMATION:

Step	1st Data	2nd Data
1	0000H	------
2	0000H	0000H
3	5500H	0000H
4	AA00H	0000H
5	CC00H	0000H
6	3300H	0000H
7	6600H	0000H
8	9900H	0000H
9	FF00H	0000H
10	0000H	0000H
11	0000H	0000H
12	0000H	0000H
13	0000H	0000H
14	0000H	0000H
15	0000H	0000H
16	0000H	0000H

17	0000H	0000H
18	0100H	0000H
19	0200H	0000H
20	0400H	0000H
21	0800H	0000H
22	1000H	0000H
23	2000H	0000H
24	4000H	0000H
25	8000H	0000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Glitch Data Bits 8-F Error
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 25.

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 8

TITLE: PROBES/MULTIPLEX TEST

TARGET LOGIC:

SECTIONS A,C,E					SECTIONS B,D			
E9					E2			
A6	A8	A9	A10	A11	A1	A2	A3	A4
	B8	B9	B10	B11	B1	B2	B3	B4
	C8	C9	C10	C11	C1	C2	C3	C4
	D8			D11	D1			D4
	E8			E11	E1			E4
	F8			F11	F1			F4
	G8			G11	G1			G4

J1, J2, Internal Probe Cables, External Probe Cables

All of the hardware in the Data Path Test.

TEST DESCRIPTION:

This subtest checks the five Multiplexing Select Modes of the Data Board. The five modes are:

1. "NORMAL" mode. This samples the logic state at the inputs of J1 and J2. This logic state is set high or low by the external probes.

2. "DEMUX" mode. This is similar to the Normal Mode except the lower eight bits are mirrored into the upper eight bits.

3. "DIAGNOSTIC" select. This reads the Diagnostic bits Register.

4. "MEMORY" select. This reads the data that is currently residing in the ECL Memory, (Manual Recirculate).

5. NOTHING SELECTED. With all four select lines disabled, the Data lines should be pulled up to read 0FFFFH.

This test requires the use of a known good Threshold Board and the installation of the external probes. The Normal Mode and the Demux Mode use the Threshold board to set threshold levels at the hybrid circuit in the probes.

TEST STEP INFORMATION:

Step	Data Expected	Multiplex	Threshold
1	FFFFH	Normal	ECL
2	0000H	Normal	VARIABLE A
3	FFFFH	Normal	VARIABLE B
4	FFFFH	Demux	ECL
5	0000H	Demux	VARIABLE A
6	FFFFH	Demux	VARIABLE B
7	F069H	Diagnostic	----------
8	5AC3H	Memory	----------
9	FFFFH	Floating	----------

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 9.

hmsg is the Error heading message:

Normal ECL Threshold Mux Error,
Normal VARA F Threshold Mux Error,
Normal ECLVARA Threshold Mux Error,
Demux ECL Threshold Mux Error,
Demux VARA F Threshold Mux Error,
Demux ECLVARA Threshold Mux Error,
Diagnostic Select Mux Error,
Memory Select Mux Error,
Multiplexer Disable-Float Error.

aaaa is the I/O address of the Data Board:

082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 9

TITLE: PIPELINES SHIFT TEST

TARGET LOGIC:	SECTIONS A,C,E	SECTIONS B,D
	E9	E2

TEST DESCRIPTION:

This subtest checks the Data Board Pipeline. The Pipeline consists of a three step FILO, (first in last out), with "D" latches at each step that can be read. The steps are called the "Old Pipe Register", the "New Pipe Register", and the "Old Pipe Register" respectively.

With each Pipeline Clock, the Old Pipeline Register Data is lost and receives its new data from the New Pipeline Register. The New Pipeline Register receives its new data from the Old Pipe Register. The Old Pipe Register receives its data from the Glitch Latches.

The Pipeline can receive it's clocking from either the Sample Clock if "Single Phase Mode" is selected, or from the Control Clock if "Multi Phase Mode" is selected. Test Steps 1 - 24 will use the Sample Clock, and Test Steps 25 - 48 will use the Control Clock.

TEST STEP INFORMATION:

Step	Sample Data	New Pipe Data	Old Pipe Data	Mode of Phase
1	0000H	0000H	0000H	Single Phase
2	5555H	0000H	0000H	Single Phase
3	AAAAH	5555H	0000H	Single Phase
4	CCCCH	AAAAH	5555H	Single Phase
5	3333H	CCCCH	AAAAH	Single Phase
6	6666H	3333H	CCCCH	Single Phase
7	9999H	6666H	3333H	Single Phase
8	FFFFH	9999H	6666H	Single Phase
9	0001H	FFFFH	9999H	Single Phase
10	0002H	0001H	FFFFH	Single Phase
11	0004H	0002H	0001H	Single Phase
12	0008H	0004H	0002H	Single Phase
13	0010H	0008H	0004H	Single Phase
14	0020H	0010H	0008H	Single Phase
15	0040H	0020H	0010H	Single Phase
16	0080H	0040H	0020H	Single Phase
17	0100H	0080H	0040H	Single Phase
18	0200H	0100H	0080H	Single Phase
19	0400H	0200H	0100H	Single Phase
20	0800H	0400H	0200H	Single Phase
21	1000H	0800H	0400H	Single Phase
22	2000H	1000H	0800H	Single Phase
23	4000H	2000H	1000H	Single Phase
24	8000H	4000H	2000H	Single Phase

25	0000H	0000H	0000H	Multi Phase
26	5555H	0000H	0000H	Multi Phase
27	AAAAH	5555H	0000H	Multi Phase
28	CCCCH	AAAAH	5555H	Multi Phase
29	3333H	CCCCH	AAAAH	Multi Phase
30	6666H	3333H	CCCCH	Multi Phase
31	9999H	6666H	3333H	Multi Phase
32	FFFFH	9999H	6666H	Multi Phase
33	0001H	FFFFH	9999H	Multi Phase
34	0002H	0001H	FFFFH	Multi Phase
35	0004H	0002H	0001H	Multi Phase
36	0008H	0004H	0002H	Multi Phase
37	0010H	0008H	0004H	Multi Phase
38	0020H	0010H	0008H	Multi Phase
39	0040H	0020H	0010H	Multi Phase
40	0080H	0040H	0020H	Multi Phase
41	0100H	0080H	0040H	Multi Phase
42	0200H	0100H	0080H	Multi Phase
43	0400H	0200H	0100H	Multi Phase
44	0800H	0400H	0200H	Multi Phase
45	1000H	0800H	0400H	Multi Phase
46	2000H	1000H	0800H	Multi Phase
47	4000H	2000H	1000H	Multi Phase
48	8000H	4000H	2000H	Multi Phase

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 48.

hmsg is the Error heading message:
Sample Clock: Old Pipe Register Error
Sample Clock: New Pipe Register Error
Sample Clock: Old Pipe Register Error
Control Clock: Old Pipe Register Error
Control Clock: New Pipe Register Error
Control Clock: Old Pipe Register Error

aaaa is the I/O address of the Data Board:
082H for Data Board AB Section A old pipe Register,
0C2H for Data Board AB Section B old pipe Register,
092H for Data Board CD Section C old pipe Register,
0D2H for Data Board CD Section D old pipe Register,
0A2H for Data Board E Section E old pipe Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 10

TITLE: RAM DATA INTEGRITY TEST

TARGET LOGIC:

SECTIONS A,C,E					SECTIONS B,D				
A6	A8	A9	A10	A11	A1	A2	A3	A4	A6
	B8	B9	B10	B11	B1	B2	B3	B4	
	C8	C9	C10	C11	C1	C2	C3	C4	
	D8			D11	D1			D4	
	E8	E9		E11	E1	E2		E4	
	F8			F11	F1			F4	
	G8			G11	G1			G4	

TEST DESCRIPTION:

This subtest performs a static test of the RAM on the Data boards. This is done using the 24 Data patterns. All 2048 Memory locations are written to with the same data to the same I/O port 086H. Since the address counters should be advancing on each Sample Clock, all locations should be written to the same I/O port.

This test does not check the addressing uniqueness of each location. It does verify that all Data bits are functional and totally independent of each other.

Prior to this test, the Data path up to the Old Pipe Register has been checked. There are two 10H176 "D" latches between the Old Pipe Register and the RAM chip. These latches receive their clock from either ACKPH1 or ACKPH2 depending on the current Phase of the clock. The signals AWEPH1 and AWEPH2 are the write enables to the RAM chips. Therefore, the RAM chips are alternately written to on each Sample Clock.

TEST STEP INFORMATION:

Step	Data	Data Written to	Data Verified at
1	0000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
2	5555H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
3	AAAAH	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
4	CCCCH	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
5	3333H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
6	6666H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
7	9999H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
8	FFFFH	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
9	0001H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
10	0002H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
11	0004H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
12	0008H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
13	0010H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
14	0020H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
15	0040H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH

16	0080H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
17	0100H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
18	0200H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
19	0400H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
20	0800H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
21	1000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
22	2000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
23	4000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
24	8000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Data Integrity Verify Error
Byte Count       = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 24.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 11

TITLE: RAM ADDRESSING INTEGRITY TEST

TARGET LOGIC:

SECTIONS A,C,E					SECTIONS B,D				
A6	A8	A9	A10	A11	A1	A2	A3	A4	A6
	B8	B9	B10	B11	B1	B2	B3	B4	
	C8	C9	C10	C11	C1	C2	C3	C4	
	D8			D11	D1			D4	
	E8	E9		E11	E1	E2		E4	
	F8			F11	F1			F4	
	G8			G11	G1			G4	

TEST DESCRIPTION:

This subtest writes a unique Data value to each of the 2048 Memory locations. Each memory location should contain unique Data from each other location. The Memory is read back and each location is verified to see if each address is uniquely addressable.

The Data that is written is an incrementing pattern. The first test step starts with a value of 0001H for the first location, and the sequencial locations are written to with a 0002H, 0003H, etc.

The second Test step is similar to the first, except the starting Data value is a 0002H. Subsequent test steps shift this Data value left, so that the starting Data values for the 16 test steps are:

TEST STEP INFORMATION:

Step	Start Data	Data Written to	Data Verified at
1	0001H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
2	0002H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
3	0004H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
4	0008H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
5	0010H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
6	0020H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
7	0040H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
8	0080H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
9	0100H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
10	0200H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
11	0400H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
12	0800H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
13	1000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
14	2000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
15	4000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH
16	8000H	086H, Diagnostic Latch	080H, RAM Locations 000 - 1FFH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
RAM Address Unique Error
Byte Count       = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 16.

aaaa is the Address offset for the RAM, in the range of 0 to 1FFH.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 12

TITLE: TRACE CONDITIONS TEST

TARGET LOGIC:	SECTIONS A,C,E	SECTIONS B,D
	E9	E2

TRACED/ Signal from Control Board
ARMED Signal from Control Board

TEST DESCRIPTION:

This subtest uses the Control Board to provide Trace Conditions that exist on the Data Board. These are mainly "ARMED" and "TRACED/". This test is similar to the Force Conditions Test.

TEST STEP INFORMATION:

Step	Status Expected
1	45H
2	C5H
3	72H
4	71H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Trace Conditions Error
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected  = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8  = iiiiH
```

Where:
ssss is the test step number in the range of 1 to 4.

aaaa is the I/O address of the Data Board:
088H for Data Board AB Section A Status Register,
0C8H for Data Board AB Section B Status Register,
098H for Data Board CD Section C Status Register,
0D8H for Data Board CD Section D Status Register,
0A8H for Data Board E Section E Status Register,

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

Data Board Diagnostic Subtest 13

TITLE: RECIRCULATE RAM TEST

TARGET LOGIC:

The main hardware being tested is the feed back loop of the 10173 Multiplexers with Memory Select Enabled and all the RAM circuitry at high speeds.

The Entire Data Path and Most of the Control Logic must be functional for this test to pass.

TEST DESCRIPTION:

The contents of the ECL RAM is recirculated out of the RAM through the Multiplexers, through the Glitch Latches, through the Sample Register, through the New Pipe Register, through the Old Pipe Register, through the RAM latch and back into the ECL RAM. All of the clocking is done by the Clock board and the Control Board.

There is a time-out counter on the recirculation, and after the recirculation is complete, the Data in the ECL RAM should be the same as before.

TEST STEP INFORMATION:

Step	Status Expected	Clock Time Out
1	8000H	10 usec
3	8000H	20 usec
5	8000H	30 usec

Step	Data Expected
2	0000H - 01FFH (incrementing pattern)
4	0000H - 01FFH (incrementing pattern)
6	0000H - 01FFH (incrementing pattern)

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg
I/O Address      = aaaaH
Data Read        = rrrrH
Data Expected    = eeeeH
Error Bit Map    = 0000000000000000B
Board Status X8 = iiiiH
```

Where:

ssss is the test step number in the range of 1 to 6.

hmsg is the Error heading message:
Recirculation Time out-10us clock,
Recirculation Error-10us clock,
Recirculation Time out-20us clock,
Recirculation Error-20us clock,
Recirculation Time out-30us clock,
Recirculation Error-30us clock.

aaaa is the I/O address of the Data Board:
080H for Data Board AB Section A RAM,
0C0H for Data Board AB Section B RAM,
090H for Data Board CD Section C RAM,
0D0H for Data Board CD Section D RAM,
0A0H for Data Board E Section E RAM,
0F0H for Control Board Status.

rrrr is the Data Word read from the Data Board.

eeee is the Data Word Expected from the Data Board.

iiii is the Status information from the current Data Board under test.

NOTE:

The Error Bit Map is a map of the Data Bus, D0 - D15, and is an exclusive Or of the Data Read and the Data Expected. Any bits that are different show up as a "1". Bits that show up as a "0" passed the compare.

CONTROL BOARD DIAGNOSTIC TEST

DIAGNOSTIC OVERVIEW

This section describes the subtests executed on the K450B TRACE CONTROL board and the associated error reporting.

In order for the Diagnostic to run properly, the board under test must be installed in the Mother Board, (not on an extender card). Also, all of the three data boards must be installed in the K450B system.

The TRACE CONTROL board diagnostics is divided into 12 subtests, each of which is described individually on the following pages.

Subtest 1 is a Force Conditions test. Subtest 2 is a Advance RAM Forward and Jump RAM Backward test. Subtests 3 and 4 are Detection RAMs Data and Address Integrity test. Subtests 5 and 6 are Delay Control RAM Data and Address Integrity test. Subtests 7 and 8 are Delay RAMs Data and Address Integrity test. Subtest 9 is Delay Counter test. Subtest 10 is a Relation Logic test. Subtest 11 and 12 are Selection RAMs Data and Address Integrity test.

The external signals through mother board to the data boards are checked in Subtest 1. The external signals through connector J1 to the clock boards are checked in Subtest 2.

Subtests 1,3 and 4 require data boards A,B and C installed in the system.

NOTE:

The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. FORCE CONDITION TEST
2. ADVANCE AND JUMP RAM TEST
3. DETECTION RAMS DATA INTEGRITY TEST
4. DETECTION RAMS ADDRESS INTEGRITY TEST
5. DELAY CONTROL RAM DATA INTEGRITY TEST
6. DELAY CONTROL RAM ADDRESS INTEGRITY TEST
7. DELAY RAMS DATA INTEGRITY TEST
8. DELAY RAMS ADDRESS INTEGRITY TEST
9. DELAY COUNTER TEST
10. RELATION LOGIC TEST
11. SELECTION RAMS DATA INTEGRITY TEST
12. SELECTION RAMS ADDRESS INTEGRITY TEST

ERROR COUNT CATEGORY

1. SUBTEST 1 ERROR COUNT.
2. SUBTEST 2 ERROR COUNT.
3. SUBTEST 3 ERROR COUNT.
4. SUBTEST 4 ERROR COUNT.
5. SUBTEST 5 ERROR COUNT.
6. SUBTEST 6 ERROR COUNT.
7. SUBTEST 7 ERROR COUNT.
8. SUBTEST 8 ERROR COUNT.
9. SUBTEST 9 ERROR COUNT.
10. SUBTEST 10 ERROR COUNT.
11. SUBTEST 11 ERROR COUNT.
12. SUBTEST 12 ERROR COUNT.

Control Board Diagnostic Subtest 1

TITLE: FORCE CONDITION TEST

TARGET LOGIC: See sheet 10 of the schematic and appropriate FORCE LOGIC.

TEST DESCRIPTION:

The force condition is functionally tested by forcing the desired condition true. The condition is then verified by reading back the corresponding status bit.

There are 7 force condition tests (0-6) included; condition 0 is force level 0; condition 1 is force jump and jump not; condition 2 is force trace and trace not; condition 3 is force stop and stop not; condition 4 is force event and advance; condition 5 is force stopped and armed; condition 6 is force manual advance.

Conditon 2 also verifies the 'TRACED' signal can propagate through the mother board to data boards A,B,C. Condition 5 also verifies the 'MEM. ARMED' signal can propagate through the mother board to data boards A,B and C.

TEST STEP INFORMATION:

Test step	Condition tested	Signals in schematics
1	force level 0	'FORCE LEVEL=0'
2	force jump and jump not	'FORCE JUMP','FORCE JUMP/'
3	force trace and trace not	'FORCE TRACE','FORCE TRACE/'
4.	force stop and stop not	'FORCE STOP','FORCE STOP/'
5.	force event and advance	'FORCE EVENT AND ADVANCE'
6.	force stopped and armed	'CYCLE RESET'
7.	force manual advance	'ENABLE MANUAL ADVANCE'

ERROR MESSAGES:
---

1. If an error for condition 0 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force Level 0
Level Expected = eeH
Level Read     = rrH
```

Where zz should be 01

ee should be 00 through 0F

rr should be 00 through 0F

2. If an error for condition 1 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force JUMP & JUMP NOT
Jump Expected = e
Jump Read     = r
```

Where zz should be 02

e should be 0 or 1

r should be 0 or 1

3. If an error for condition 2 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force TRACE & TRACE NOT
Trace Expected          = e
Trace Read              = r
Old Traced A Expected = a
Old Traced A Read       = t
Old Traced B Expected = b
Old Traced B Read       = u
Old Traced C Expected = c
Old Traced C Read       = v
```

Where zz should be 03

e,r,a,t,b,u,c,v should be 0 or 1

4. If an error for condition 3 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOP & STOP NOT
Stop Expected = e
Stop Read     = r
```

Where zz should be 04

e should be 0 or 1

r should be 0 or 1

5. If an error for condition 4 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force EVENT & ADVANCE
Event Expected    = e
Event Read        = r
Advance Expected  = p
Advance Read      = d
```

Where zz should be 05

e,r,p,d should be 0 or 1

6. If an error for condition 5 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force STOPPED & ARMED
Stopped Expected       = e
Stopped/ Read          = r
Armed Expected         = p
Armed/ Read            = d
Mem. Armed A Expected  = a
Mem. Armed A Read      = t
Mem. Armed B Expected  = b
Mem. Armed B Read      = u
Mem. Armed C Expected  = c
Mem. Armed C Read      = v
```

Where zz should be 06

e,r,p,d,a,t,b,u,c,v should be 0 or 1

7. If an error for condition 6 occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP zz
CONDITION : Force MANUAL ADVANCE
Advance Expected         = e
AdvancE Read             = r
Manual Advance Expected  = p
Man. Advance Read        = d
```

Where zz should be 07

e,r,p,d should be 0 or 1

Control Board Diagnostic Subtest 2

TITLE: ADVANCE AND JUMP RAM TEST

TARGET LOGIC: 5H 5J 5G

INTERNEDIATE LOGIC: 5K 12F 11F 4B 6B 7A 7C 9D 11D

TEST DESCRIPTION:

The advance and jump RAMs are functionally tested by advancing the advance RAM to the next level and restoring the jump RAM backward to a previous level. The RAM data is then verified by reading back the level and comparing the result to the expected level.

TEST STEP INFORMATION:

Test Step	RAM Tested	Level Tested	Expected Level
1 through 16	advance	00H through 0FH	Level tested + 1
17 through 32	jump	00H through 0FH	Level tested - 1

ERROR MESSAGE:

1. If an error of advance RAM occurs,the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Adv. RAM Advancing Test
Adv. RAM Level at       = llH
Adv. RAM Data Expected  = eeH
Adv. RAM Data Read      = rrH
Error Bit Map           = xxxxxxxxB
Ext. Level Expected     = ppH
Ext. Level Read         = qqH
Error Bit Map           = yyyyyyyyB
```

Where zz should be 01 through 16

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

pp should be 00 through 0F

qq should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

yyyyyyyy should be 00000000 through 00001111

2. If an error of jump RAM occurs,the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Jump RAM Advancing Test
Jump RAM Level at = llH
Jump RAM Data Expected = eeH
Jump RAM Data Read = rrH
```

Where zz should be 17 through 32

ll should be 00 through 0F

ee should be 00 through 0F

rr should be 00 through 0F

Control Board Diagnostic Subtest 3

TITLE: DETECTION RAM DATA INTEGRITY TEST

TARGET LOGIC:

1F 1G
3F 3G
4F 4G
7F 7G
8F 8G
9F 9G

INTERMEDIATE LOGIC: 8D,9D
3D,4D,7D
1D,3D
6B,5B,4B,7B,8B,1B,2B,3B,8A,9A
5D,5C,7C,4D,5F,3C,1C,8C,9C,9B
12C,12G,12H,3K

TEST DESCRIPTION:

The detection RAMs data integrity is functionally tested by writing a 4 bits nibble into each RAM. The RAM data is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) nibble and comparing the result to the expected nibble.

The nibble patterns tested are:

1010B,0101B,1100B,0011B,0001B,0010B,0100B,1000B.

The detection RAMs tested are:

8G,8F,9G,9F,4G,4F,7G,7F,1G,1F,3G,3F.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Nibble Patterns
01 through 08	8F(00)	1010,0101,1100,0011,0001,0010,0100,1000
09 through 16	8G(01)	1010,0101,1100,0011,0001,0010,0100,1000
17 through 24	9F(02)	1010,0101,1100,0011,0001,0010,0100,1000
25 through 32	9G(03)	1010,0101,1100,0011,0001,0010,0100,1000
33 through 40	4F(04)	1010,0101,1100,0011,0001,0010,0100,1000
41 through 48	4G(05)	1010,0101,1100,0011,0001,0010,0100,1000
49 through 56	7F(06)	1010,0101,1100,0011,0001,0010,0100,1000
57 through 64	7G(07)	1010,0101,1100,0011,0001,0010,0100,1000
65 through 72	1F(08)	1010,0101,1100,0011,0001,0010,0100,1000
73 through 80	1G(09)	1010,0101,1100,0011,0001,0010,0100,1000
81 through 88	3F(10)	1010,0101,1100,0011,0001,0010,0100,1000
89 through 96	3G(11)	1010,0101,1100,0011,0001,0010,0100,1000

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Data Integrity Test
RAM chip location      = cc
Detect Address         = ddddH
AJST/ Nibble Expected  = nnH
AJST/ Nibble Read      = rrH
Error Bit Map          = xxxxxxxxB
```

Where cc should be 00 through 11

dddd should be 0000 through 03FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF

xxxxxxxx should be 00000000 through 00001111

NOTE : AJST is the abbreviation of ADVANCE, JUMP, STOP, TRACE

Control Board Diagnostic Subtest 4

TITLE: DETECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 1J,1H,3J,3H,4J,4H,7J,7H,8J,8H,9J,9H,
8G,8F,9G,9F,
4G,4F,7G,7F,
1G,1F,3G,3F,

TEST DESCRIPTION:

The detection RAMs address integrity is functionally tested by clearing all locations of each RAM,then writing a 4 bits nibble(1010B) into the asserted address,the RAM address is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) nibble from all locations,and compare to the nibble 0AH.

The detection RAMs tested are:

8G,8F,9G,9F,4G,4F,7G,7F,1G,1F,3G,3F.

There are 10 address bits for each detection RAM,low nibble from levels,rest of the bits from sample registers of data boards.

TEST STEP INFORMATION:

Test Step	RAM Chip Location	Asserted Address Bit
1 through 10	8F(00)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
11 through 20	8G(01)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
21 through 30	9F(02)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
31 through 40	9G(03)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
41 through 50	4F(04)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
51 through 60	4G(05)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
61 through 70	7F(06)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
71 through 80	7G(07)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
81 through 90	1F(08)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
91 through 100	1G(09)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
101 through 110	3F(10)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H
111 through 120	3G(11)	01H,02H,04H,08H,10H,20H,40H,80H,100H,200H

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Detection RAMs Address Integrity Test
RAM Chip Location     = cc
High Nibble Related to Data Board B
Address Expected      = ddddH
Address Found         = ffffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read     = rrH
```

Where cc should be 00 through 11

b should be A,B,C

dddd should be 0000 through FF

ffff should be 0000 through 03FF

nn should be 0A,05,0C,03,01,02,04,08

rr should be 00 through FF

Note : AJST is the abbreviation of ADVANCE,JUMP,STOP,TRACE

Control Board Diagnostic Subtest 5

TITLE: DELAY CONTROL RAM DATA INTEGRITY TEST

TARGET LOGIC: 13A,12C,12G,12H

TEST DESCRIPTION:

The delay control RAM data integrity is functionally tested by writing a four bits nibble into the delay control RAM. The RAM data is then verified by reading the (EVENT MODE,END LEVEL,(D=1 IF JUMP)/,(D=1 IF ADVANCE)/) nibble from bit 14 0f port 0FEH, 0FCH, 0FAH, 0F8H and comparing the result to the nibble written.

There are 8 nibble patterns:

1010B,0101B,1100B,0011B,0001B,0010B,0100B,1000B.

TEST STEP INFORMATION:

Teset Step	Nibble Pattern	Levels
1	1010B	0 through 0FH
2	0101B	0 through 0FH
3	1100B	0 through 0FH
4	0011B	0 through 0FH
5	0001B	0 through 0FH
6	0010B	0 through 0FH
7	0100B	0 through 0FH
8	1000B	0 through 0FH

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step  zz
Delay control RAM Data Integrity Test
RAM Address      = aaH
Nibble Expected = eeH
Nibble Read      = rrH
Error Bit Map    = xxxxxxxxB
```

Where aa should be 00 through 0F

ee should be 0A,05,0C,03,01,02,04,08

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

Control Board Diagnostic Subtest 6

TITLE: DELAY CONTROL RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 13A,12C,12G,12H

TEST DESCRIPTION:

The delay control RAM address integrity is functionally tested by writing a 4 bits nibble(1010B) into the asserted address. The address is then verified by reading nibble data from all 16 locations and comparing the result to the
nibble expected(1010B).

TEST STEP INFORMATION:

Test Step	Nibble Pattern	Asserted Address
1	1010B	0001B
2	1010B	0010B
3	1010B	0100B
4	1010B	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay control RAM Address Integrity test
Address Expected = eeH
Address Found    = ffH
Nibble Expected  = nnH
Nibble Read      = rrH
```

Where zz should be 1 through 4

ee should be 01,02,04,08

ff should be 00 through FF

nn should be 0A.

rr should be 00 through 0F

Control Board Diagnostic Subtest 7

TITLE: DELAY RAMS DATA INTEGRITY TEST

TARGET LOGIC: 14C,14D,14E,14F,13C,13D,13E,13F
11C,11B,12D,12E,12G,12H

TEST DESCRIPTION:

The delay RAMs data integrity is functionally tested by writing a word pattern into the delay RAMs. The word data of RAMs is then loaded into the delay counter. The data integrity is then verified by reading the word data and comparing the result to the word expected.

There are 8 delay word patterns tested:

AAAAH, 5555H, CCCCH, 3333H, 1111H, 2222H, 4444H, 8888H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested
1	AAAAH
2	5555H
3	CCCCH
4	3333H
5	1111H
6	2222H
7	4444H
8	8888H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Data Integrity Test
RAM Address    = aaH
Word Expected  = eeeeH
Word Read      = rrrrH
Error Bit Map  = xxxxxxxxxxxxxxxxB
```

Where: zz should be 1 through 8.

aa should be 00 through 0F

eeee should be AAAA,5555,CCCC,3333,1111,2222,4444,8888

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

Control Board Diagnostic Subtest 8

TITLE: DELAY RAMS ADDRESS INTEGRITY TEST

TARGET LOGIC: 14C,14D,14E,14F

INTERMEDIATE LOGIC 13C,13D,13E,13F
11C,11B,12D,12E,12G,12H

TEST DESCRIPTION:

The delay RAMs address integrity is functionally tested by writing a word (0AAAAH) into the asserted level address. The delay RAMs is then loaded into the delay counter,the address integrity is then verified by reading the delay count from all level addresses and comparing the result to the word 0AAAAH.

There are 4 address bits tested : 0001B, 0010B, 0100B, 1000B.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Asserted Level Address
1	AAAAH	0001B
2	AAAAH	0010B
3	AAAAH	0100B
4	AAAAH	1000B

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay RAM Address Integrity Test
Address Expected = aaH
Address Found    = ffH
Word Expected    = eeeeH
Word Read        = rrrrH
```

Where zz should be 1 through 4.

aa should be 01,02,04,08

ff should be 00 through 0F

eeee should be AAAA.

rrrr should be 0000 through FFFF

Control Board Diagnostic Subtest 9

TITLE: DELAY COUNTER TEST

TARGET LOGIC: 13C,13D,13E,13F

INTERMEDIATE LOGIC 14C,14D,14E,14F
11C,11B,12D,12E,12G,12H

TEST DESCRIPTION:

The delay counter is functionally tested by writing the delay word into delay RAMs and then loading it into the delay counter. The counting operation is then verified by kicking clocks, reading the delay count and comparing the result to the word expected.

The counting operation is verified by the following two method:

1. Kick clocks until delay count is equal to 0.
2. Kick a clock to increment only one count.

The delay count word patterns being tested are:

8000H, 4000H, 2000H, 1000H, 0800H, 0400H, 0200H, 0100H, 0080H, 0040H, 0020H, 0010H, 0008H, 0004H, 0002H, 0001H.

TEST STEP INFORMATION:

Test Step	Word Pattern Tested	Clocks to Kick	Expected Count
1	8000H	8000H	0
2	8000H	1	8001H
3	4000H	C000H	0
4	4000H	1	4001H
5	2000H	E000H	0
6	2000H	1	2001H
7	1000H	F000H	0
8	1000H	1	1001H
9	0800H	F800H	0
10	0800H	1	0801H
11	0400H	FC00H	0
12	0400H	1	0401H
13	0200H	FE00H	0
14	0200H	1	0201H
15	0100H	FF00H	0
16	0100H	1	0101H
17	0080H	FF80H	0
18	0080H	1	0081H
19	0040H	FFC0H	0
20	0040H	1	0041H

21	0020H	FFE0H	0
22	0020H	1	0021H
23	0010H	FFF0H	0
24	0010H	1	0011H
25	0008H	FFF8H	0
26	0008H	1	0009H
27	0004H	FFFCH	0
28	0004H	1	0005H
29	0002H	FFFEH	0
30	0002H	1	0003H
31	0001H	FFFFH	0
32	0001H	1	0002H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Delay Counting Operation Test
Count Pattern  = ccccH
Count Expected = eeeeH
Count Read     = rrrrH
Error Bit Map  = xxxxxxxxxxxxxxxxB
```

Where zz should be 1 throygh 32.

cccc should be 8000,4000,2000,1000,0800,0400,
0200,0100,0080,0040,0020,0010,
0008,0004,0002,0001.

eeee should be 8000,4000,2000,1000,0800,0400,0200,0100,
0080,0040,0020,0010,0008,0004,0002,0001,0.

rrrr should be 0000 through FFFF

xxxxxxxxxxxxxxxx should be 0000000000000000 through 1111111111111111

Control Board Diagnostic Subtest 10

TITLE: RELATION LOGIC TEST

TARGET LOGIC: 12B,14B,12A,13A,11A,11F,11C,11B,11D,9B,9C,12F

TEST DESCRIPTION:

The relation logic is functionally tested by making one of the logic paths true. The relation is then verified by reading the desired relation bit and comparing the result to the expected logic state.

The Boolean function of each logic path is :

```
Path 1 : P1 = (old T < D)*(advanced + jumped)*(evented)*(TC)
Path 2 : P2 = (jumped)*(D=1 If Jumped)
Path 3 : P3 = (advanced)*(D=1 If advanced)*(jumped /)
Path 4 : P4 = (old T = D)*(evented /)*((advanced + jumped) /)
Path 5 : P5 = (old T = D)*(evented)*((advanced + jumped) /)
Path 6 : P6 = (old T > D)*((advanced + jumped) /)
(T < D) = NOT (P1 + P2 + P3 + P4 + P5)
(T = D) = P1 + P2 + P3 + P4
(T > D) = P5 + P6
Path 0 logic means T < D true.
```

TEST STEP INFORMATION:

Test Step	Logic Path	Relation True
1	0,1	T < D then T = D
2	2	T = D
3	3	T = D
4	4,5,6	T = D then T > D

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Relation Logic Path p Failed
"T < D" Expected = a
"T < D" Read     = b
"T = D" Expected = c
"T = D" Read     = d
"T > D" Expected = e
"T > D" Read     = f
```

Where zz should be 1 throygh 4.

a,b,c,d,e,f should be 0 or 1.

Control Board Diagnostic Subtest 11

TITLE: SELECTION RAM DATA INTEGRITY TEST

TARGET LOGIC: 6B,5B,4B,7B,8B,1B,2B,3B,8A,9A,

INTERMEDIATE LOGIC: 5C,5D,7C,4D,8D,5F,7D,1C,3C,8C, 9C,3D,9B,6A

TEST DESCRIPTION:

The selection RAMs data integrity is functionally tested by separating all RAMs into 4 subgroups(ADVANCE,JUMP,STOP,TRACE),writing the specified data into the RAMS of each subgroup. The data integrity is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) bits and comparing the result to the nibble expected.

There are 4 subgroups being tested:

Subgroup A :
- bit 0 -- selection bit for ADVANCE A
- bit 1 -- selection bit for ADVANCE B
- bit 2 -- selection bit for ADVANCE C
- bit 3 -- selection bit for (ADVANCE C.B.A)/
- bit 4 -- selection bit for ADVANCE if T > D
- bit 5 -- selection bit for ADVANCE if T = D
- bit 6 -- selection bit for ADVANCE if T < D
- bit 7 -- selection bit for ADVANCE if 'x'

Subgroup J :
- bit 0 -- selection bit for JUMP A
- bit 1 -- selection bit for JUMP B
- bit 2 -- selection bit for JUMP C
- bit 3 -- selection bit for (JUMP C.B.A)/
- bit 4 -- selection bit for JUMP if T > D
- bit 5 -- selection bit for JUMP if T = D
- bit 6 -- selection bit for JUMP if T < D

Subgroup S :
- bit 0 -- selection bit for STOP A
- bit 1 -- selection bit for STOP B
- bit 2 -- selection bit for STOP C
- bit 3 -- selection bit for (STOP C.B.A)/
- bit 4 -- selection bit for STOP if T > D
- bit 5 -- selection bit for STOP if T = D
- bit 6 -- selection bit for STOP if T < D
- bit 7 -- selection bit for STOP if 'x'

Subgroup T :
- bit 0 -- selection bit for TRACE A
- bit 1 -- selection bit for TRACE B
- bit 2 -- selection bit for TRACE C
- bit 3 -- selection bit for (TRACE C.B.A)/
- bit 4 -- selection bit for TRACE if T > D
- bit 5 -- selection bit for TRACE if T = D
- bit 6 -- selection bit for TRACE if T < D
- bit 7 -- selection bit for TRACE if 'x'

Each bit has logic 0 and logic 1 to be tested.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Related Chip
1	Advance	0	ADVANCE A	0	4B-D3
2	Advance	0	ADVANCE A	1	4B-D3
3	Advance	1	ADVANCE B	0	5B-D2
4	Advance	1	ADVANCE B	1	5B-D2
5	Advance	2	ADVANCE C	0	5B-D3
6	Advance	2	ADVANCE C	1	5B-D3
7	Advance	3	(ADVANCE C.B.A)/	0	5B-D1
8	Advance	3	(ADVANCE C.B.A)/	1	5B-D1
9	Advance	4	ADVANCE if T > D	0	6B-D2
10	Advance	4	ADVANCE if T > D	1	6B-D2
11	Advance	5	ADVANCE if T = D	0	6B-D0
12	Advance	5	ADVANCE if T = D	1	6B-D0
13	Advance	6	ADVANCE if T < D	0	6B-D3
14	Advance	6	ADVANCE if T < D	1	6B-D3
15	Advance	7	ADVANCE if 'x'	0	6B-D1
16	Advance	7	ADVANCE if 'x'	1	6B-D1
17	Jump	0	Jump A	0	8B-D2
18	Jump	0	Jump A	1	8B-D2
19	Jump	1	Jump B	0	8B-D3
20	Jump	1	Jump B	1	8B-D3
21	Jump	2	Jump C	0	4B-D0
22	Jump	2	Jump C	1	4B-D0
23	Jump	3	(Jump C.B.A)/	0	4B-D2
24	Jump	3	(Jump C.B.A)/	1	4B-D2
25	Jump	4	Jump if T > D	0	7B-D3
26	Jump	4	Jump if T > D	1	7B-D3
27	Jump	5	Jump if T = D	0	7B-D1
28	Jump	5	Jump if T = D	1	7B-D1
29	Jump	6	Jump if T < D	0	7B-D2
30	Jump	6	Jump if T < D	1	7B-D2
31	Jump	7	None	x	None
32	Jump	7	None	x	None
33	Stop	0	Stop A	0	3B-D2
34	Stop	0	Stop A	1	3B-D2
35	Stop	1	Stop B	0	2B-D0
36	Stop	1	Stop B	1	2B-D0
37	Stop	2	Stop C	0	2B-D2
38	Stop	2	Stop C	1	2B-D2
39	Stop	3	(Stop C.B.A)/	0	1B-D1
40	Stop	3	(Stop C.B.A)/	1	1B-D1
41	Stop	4	Stop if T > D	0	1B-D0
42	Stop	4	Stop if T > D	1	1B-D0
43	Stop	5	Stop if T = D	0	1B-D3
44	Stop	5	Stop if T = D	1	1B-D3
45	Stop	6	Stop if T < D	0	1B-D2
46	Stop	6	Stop if T < D	1	1B-D2
47	Stop	7	Stop if 'x'	0	2B-D3
48	Stop	7	Stop if 'x'	1	2B-D3
49	Trace	0	Trace A	0	9A-D0
50	Trace	0	Trace A	1	9A-D0
51	Trace	1	Trace B	0	8A-D2

52	Trace	1	Trace B	1	8A-D2
53	Trace	2	Trace C	0	8A-D0
54	Trace	2	Trace C	1	8A-D0
55	Trace	3	(Trace C.B.A)/	0	8A-D1
56	Trace	3	(Trace C.B.A)/	1	8A-D1
57	Trace	4	Trace ifT › D	0	9A-D2
58	Trace	4	Trace ifT > D	1	9A-D2
59	Trace	5	Trace ifT = D	0	9A-D3
60	Trace	5	Trace ifT = D	1	9A-D3
61	Trace	6	Trace ifT < D	0	3B-D0
62	Trace	6	Trace ifT < D	1	3B-D0
63	Trace	7	Trace if'x'	0	3B-D1
64	Trace	7	Trace if'x'	1	3B-D1

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Data Integrity
Subgroup g Bit b Testing
RAM Address              = aaH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read     = rrH
Error Bit Map          = xxxxxxxxB
```

Where zz should be 1 throygh 64

g should be A,J,S,T.

b should be 0 or 1.

aa should be 00 through 0F.

nn should be 08,04,02,01,0

rr should be 00 through 0F

xxxxxxxx should be 00000000 through 00001111

Control Board Diagnostic Subtest 12

TITLE: SELECTION RAM ADDRESS INTEGRITY TEST

TARGET LOGIC: 6B,5B,4B,7B,8B,1B,2B,3B,8A,9A,

INTERMEDIATE LOGIC :
5C,5D,7C,4D,8D,5F,7D,1C,3C,8C,
9C,3D,9B

TEST DESCRIPTION:

The selection RAMs address integrity is functionally tested by separating all RAMs into 4 subgroups(ADVANCE,JUMP,STOP,TRACE),clearing all locations of selection RAMs going to the asserted level address, and writing bit 0 into the RAMS of each subgroup. The address integrity is then verified by reading the (ADVANCE,JUMP,STOP,TRACE) bits from all locations.

There are 4 subgroups being tested:

Subgroup A : bit 0 -- selection bit for ADVANCE A
Subgroup J : bit 0 -- selection bit for JUMP A
Subgroup S : bit 0 -- selection bit for STOP A
Subgroup T : bit 0 -- selection bit for TRACE A

Each bit only test logic 0.

TEST STEP INFORMATION:

Test Step	Subgroup	Bit	Mnemonic	Logic State	Level Address
1	Advance	0	ADVANCE A	0	01H
2	Advance	0	ADVANCE A	0	02H
3	Advance	0	ADVANCE A	0	04H
4	Advance	0	ADVANCE A	0	08H
5	Jump	0	JUMP A	0	01H
6	Jump	0	JUMP A	0	02H
7	Jump	0	JUMP A	0	04H
8	Jump	0	JUMP A	0	08H
9	Stop	0	STOP A	0	01H
10	Stop	0	STOP A	0	02H
11	Stop	0	STOP A	0	04H
12	Stop	0	STOP A	0	08H
13	TRACE	0	TRACE A	0	01H
14	TRACE	0	TRACE A	0	02H
15	TRACE	0	TRACE A	0	04H
16	TRACE	0	TRACE A	0	08H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
*TEST FAILED -- TEST STEP  zz
Selection RAMs Address Integrity
Subgroup g Testing
Address Expected       = eeH
Address Found          = ffH
AJST/ Nibble Expected = nnH
AJST/ Nibble Read      = rrH
```

Where zz should be 1 throygh 16

g should be A,J,S,T.

ee should be 01,02,04,08

ff should be 00 through 0F

nn should be 08,04,02,01

rr should be 00 through 0F

CLOCK BOARD DIAGNOSTIC TEST

DIAGNOSTIC OVERVIEW

This section describes the subtests that are performed by the K450B Clock Board Diagnostic. The target hardware is presented, as well as a general description of each Subtest, a list of information for each Test Step, and Error messages that may be printed.

The K450B Clock Board Diagnostic is a board level Diagnostic which runs under the K450B Diagnostic Operating System. The Diagnostic verifies all functions of the Clock Board except for "J2", which presents clocks to the front panel. The hardware that is not tested is a 4028 Multiplexer/driver at 9B, two drivers at 10B, and the cable going to the front panel.

The Diagnostic Tests that are performed can be divided into five basic sections.

The first is the Force Conditions Test. This test is a series of simple I/O operations that are performed on the Clock Board.

The second is the Sample and Control Clock testing. These clocks move data on the Data Boards. Specifically, the Sample Clock controls the Data Boards' Sample Registers, and the Control Clock controls the Data Board Pipeline.

The third is the Latch Clock testing. The Latch Clocks also control data flow on the Data Boards, but in a special "latch mode" where data is latched before it reaches the Data Boards' Sample Registers.

The fourth is the Frequency testing. All seven decades from the 100Mhz Clock, down to the 100 Hz Clock are tested. The Clock Board Multiplier is tested to see if it can actually perform a divide by function, thereby slowing the clock rate.

The fifth and final is the testing of the Level RAM. The RAM is tested for Data integrity, Addressing integrity, and control logic functionality.

The Diagnostic uses Data Boards AB and CD extensively to check out the clocking features. The Diagnostic also requires the use of the Control Board and the Threshold Board. All of these boards must be operational for any realistic pinpointing of possible failures. Six of the external probes at Sections A,B,and C must be installed, with floating inputs(i.e. no connection).

Sections D and E of the data boards are not used in this test because the D section uses the same clocks as the A section and the E section uses the same clocks as the B section.

If Data Board CD is not installed (i.e. the unit being tested is a 32-channel logic analyzer), the C section clocks of the Clock Board will not be tested and the following message will be displayed:

>Testing sections A & B, cannot test section C.

This message informs the operator that the A and B sections are being tested, but there is insufficient hardware in the system to diagnose section C. All six probes must still be installed to properly test sections A and B.

The type of tests that are performed on the Clock Board are static type tests. They verify the functionality and individuality of multiplexers and gates, but do not perform "real time" testing on the board. Therefore, if racing conditions exist, or if there are problems with propagation delays, the Diagnostic will probably not detect them.

Also, the frequency test that is performed on the Clock Decades is a "ballpark" test, and does not verify that the 100 Mhz source clock is exactly 100.00 Mhz. This must be adjusted/verified with a scope or frequency counter.

The Clock Board provides very little status information to monitor the Modes or selections. Of the 133 Command Output Bits, the Clock board only provides 4 Status Input Bits.

If multiple failures exist on a Board Under Test, the problem might originate in the I/O port decoding and Data latching. This portion of the board is initially assumed to be functional. If it is not, very few if any of the tests will pass.

DESCRIPTION OF DATA BOARD REGISTERS USED TO TEST CLOCK BOARD

The Sample Clocks, Latch Clocks and Control Clocks are tested using the K450B Data Boards. The Data Boards are also used for the Frequency tests.

A simple Outline of the Registers on the Data Boards is as follows:

1. Data Boards Diagnostic Latch Register.

   Data Board AB Section A - Write Port 080H.(cannot read back this port)

   Data Board AB Section B - Write Port 0C0H. (cannot read back this port)

   Data Board CD Section C - Write Port 090H. (cannot read back this port)

This Latch is the "Front End" to the Data Board's Data Path. Data is placed in this register by simply performing an OUTWORD instruction.

2. Data Boards Sample Registers /New pipe Registers.

   Section A - cannot read / write directly to this port
   Section B - cannot read / write directly to this port
   Section C - cannot read / write directly to this port

Data is transfered from the Data Board's Diagnostic Latch Registers to the Data Board's Sample Register when a Sample Clock is issued.

Sample Register A requires Sample Clock A, Sample Register B requires Sample Clock B, and Sample Register C requires Sample Clock C.

This transfer will take place assuming the Data Board is not in "Latch" mode.

Data is transferred from the Data Boards Sample Registers to the Data Boards New Pipe Registers when a Control Clock is issued.

3. Data Boards Oldpipe Registers.

   Section A - Read Port 082H. (cannot write directly to this port)
   Section B - Read Port 0C2H. (cannot write directly to this port)
   Section C - Read Port 092H. (cannot write directly to this port)

Data is transferred from the Data Boards New Pipe Registers to the Data Boards Old Pipe Registers when a Control Clock is issued. Data Boards AB, CD and E all use a single Control Clock for transfer.

4. "Latch" Mode on the Data Boards.

When the Data Boards are in Latch Mode, an extra Data latch is present between the Diagnostic Latch Registers and the Sample Registers. A Latch Clock is required to transfer Data.

In Latch Mode, the following sequence is required to place Data into the Data Board's Sample Registers.

Output the desired Data to the Diagnostic Latch Registers. This will present the Data to the input of the "Latch" mode Registers. Issuing a Latch Clock will present this Data to the input of the Sample Registers. Issuing a Sample Clock will latch this Data in the Sample Registers.

Section A requires Latch Clock A, Section B requires Latch Clock B, and Section C requires Latch Clock C.

SUBTEST CATEGORIES

There are fourteen subtests that are performed by the Clock Board Diagnostic. These are as follows:

1. Force Conditions Test
2. Sample and Control Clocks, Diagnostic Internal Clock Test
3. Sample and Control Clocks, Or-only Enables Test
4. Sample Clocks, 10ns Clock Test
5. Sample and Control Clocks, AJ, BJ and CJ Clocks Test
6. Sample and Control Clocks, AK, BK and CK Clocks Test
7. Latch Clocks, Diagnostic Internal Clock Test
8. Latch Clocks, Diagnostic Or-only Enables Test
9. Latch Clocks, AR, BR and CR Clocks Test
10. Latch Clocks, AS, BS and CS Clocks Test
11. Decade Frequency and Multiplier Divide by Test
12. Level RAMs Data Integrity Test
13. Level RAMs Address Integrity Test
14. Level RAMs Control Test

ERROR COUNT CATEGORIES

The Error Count Display information is a one for one match with the Subtest list above. The K450B Diagnostic Operating System will display the message "Subtest n" instead of the actual test name.

Subtest 1	(Force Conditions)
Subtest 2	(Sample and Control Clocks, Diagnostic Internal)
Subtest 3	(Sample and Control Clocks, Or-only Enables)
Subtest 4	(Sample Clocks, 10ns Clock Test
Subtest 5	(Sample and Control Clocks, AJ, BJ and CJ)
Subtest 6	(Sample and Control Clocks, AK, BK and CK)
Subtest 7	(Latch Clocks, Diagnostic Internal)
Subtest 8	(Latch Clocks, Diagnostic Or-only Enables)
Subtest 9	(Latch Clocks, AR, BR and CR)
Subtest 10	(Latch Clocks, AS, BS and CS)
Subtest 11	(Decade Frequency and Multiplier)
Subtest 12	(Level RAMs Data Integrity)
Subtest 13	(Level RAMs Address Integrity)
Subtest 14	(Level RAMs Control)

Clock Board Diagnostic Subtest 1

TITLE: FORCE CONDITIONS TEST

TARGET LOGIC: 7J 6J 8J 10K 11K 12J 6K 9K 9J 11H 10H 10G 10F 9F 11K 5J

TEST DESCRIPTION:

This subtest issues commands to the Clock Board and expects to see certain status conditions existing. Commands are issued by writing to port 0BEH, and the Status is read back from port 0B2H.

Since the Clock Board only provides 4 status bits, for all of the 113 command bits, only a fraction of the I/O read/write/control logic is actually tested. If there are errors in this test the I/O decode logic an/or data latches are may be fault, and the succeeding tests will probably have multiple errors.

TEST STEP INFORMATION:

Step	Expected Status
1	A000H
2	2000H
3	0000H
4	6000H, 7000H
5	7000H

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Force Conditions/Status Error
No Clocking used
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range of 1 to 5.

aaaa is the address of the Clock Board Status Register, 00B2H.

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Status Register.

NOTE:

With the limited amount of status bits on the Clock Board, there's just no real way to pin point the cause of an error. Whether the fault lies with an address decoder, a Data Bit Driver or Latch, the fault can only really be determined using a Logic Analyzer or Scope, and setting the Loop On Error Option.

Clock Board Diagnostic Subtest 2

TITLE: SAMPLE AND CONTROL CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC:

7A 8A 10H 7B 8B 9G
7D 8D 10J 7E 8E 9H
7F 8F 7G 8G 7H 8H
11H 10D 12C 11C
10C
11B
3E 3F 3G 3H 4F 4G 4C 4D

TEST DESCRIPTION:

The Diagnostic Internal Sample Clocks A, B and C, and the Diagnostic Internal Control Clock will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing three Diagnostic Internal Sample Clocks, and checking the Oldpipe Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing two Diagnostic Internal Control Clocks, and checking the Old Pipe Registers to see if a Data transfer took place.

NOTE:

The Diagnostic Internal Clock is "kicked" by outputing a "1" to bit D0 of Write Registers 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive "kicks" can be achieved by consecutive outputs to this port. It is not necessary to ever set this bit low.

TEST STEP INFORMATION:

Step	Data	Clock Tested	Data Verified at
1	0000H	Sample A,B,C	Oldpipe Registers A,B,C
2	5555H	Sample A,B,C	Oldpipe Registers A,B,C
3	AAAAH	Sample A,B,C	Oldpipe Registers A,B,C
4	CCCCH	Sample A,B,C	Oldpipe Registers A,B,C
5	3333H	Sample A,B,C	Oldpipe Registers A,B,C
6	6666H	Sample A,B,C	Oldpipe Registers A,B,C
7	9999H	Sample A,B,C	Oldpipe Registers A,B,C
8	FFFFH	Sample A,B,C	Oldpipe Registers A,B,C
9	0000H	Control	Oldpipe Registers A,B,C
10	5555H	Control	Oldpipe Registers A,B,C
11	AAAAH	Control	Oldpipe Registers A,B,C
12	CCCCH	Control	Oldpipe Registers A,B,C

13	3333H	Control	Oldpipe Registers A,B,C
14	6666H	Control	Oldpipe Registers A,B,C
15	9999H	Control	Oldpipe Registers A,B,C
16	FFFFH	Control	Oldpipe Registers A,B,C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
17	AAAAH	0000H	0000H	Sample A	Oldpipe Registers A,B,C
18	0000H	BBBBH	0000H	Sample B	Oldpipe Registers A,B,C
19	0000H	0000H	CCCCH	Sample C	Oldpipe Registers A,B,C
20	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
21	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
22	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
23	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
24	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
25	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C

NOTE:

Test Steps 20 - 22 verify that the Control Clock does not change the contents of the Oldpipe Registers.

Test Steps 23 - 25 verify that the Control Clock can clock Data into the Oldpipe Registers with all Sample Clocks disabled.

Disable Test:

Disable Sample clock A,B,C and Control clock. Hammer the Clock Board with kick clock (sample & control) then check the data boards to make sure the data didn't move.

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
26	AAAAH	-----	-----	Sample A	Oldpipe Register A
27	-----	BBBBH	-----	Sample B	Oldpipe Register B
28	-----	-----	CCCCH	Sample C	Oldpipe Register C
29	0000H	-----	-----	Control	Oldpipe Register A
30	-----	0000H	-----	Control	Oldpipe Register B
31	-----	-----	0000H	Control	Oldpipe Register C

Force disqualify test:

Enable all clocks and make Force disqualify active. Hammer the clock board with kick clock then check all data boards to see whether data has moved or not.

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
32	AAAAH	-----	-----	Sample A	Oldpipe Register A
33	-----	BBBBH	-----	Sample B	Oldpipe Register B
34	-----	-----	CCCCH	Sample C	Oldpipe Register C
35	0000H	-----	-----	Control	Oldpipe Register A
36	-----	0000H	-----	Control	Oldpipe Register B
37	-----	-----	0000H	Control	Oldpipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Internal Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 37.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.
0000H for Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 3

TITLE: SAMPLE AND CONTROL CLOCKS, OR-ONLY ENABLES TEST

TARGET LOGIC: 3C 3F 3G 4C 4D 4E 4F 4G 5D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B and C, and Control Clock's OR-Only Enable bits are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable test.

The Sample Clocks are tested by placing Data at the Front End of the Data Board and issuing three Sample Clock by toggling the OR-Only Enable bit. The Oldpipe Registers are then checked to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing two Control Clock by toggling the OR-Only Enable bit, and checking the Oldpipe Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Oldpipe Register A
2	BBBBH	Sample B	Oldpipe Register B
3	CCCCH	Sample C	Oldpipe Register C
4	AAAAH	Control	Oldpipe Register A
5	BBBBH	Control	Oldpipe Register B
6	CCCCH	Control	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Sample A	Oldpipe Registers A,B,C
8	0000H	BBBBH	0000H	Sample B	Oldpipe Registers A,B,C
9	0000H	0000H	CCCCH	Sample C	Oldpipe Registers A,B,C
10	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C
11	AAAAH	BBBBH	CCCCH	Control	Oldpipe Registers A,B,C

Force disqualify test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
12	AAAAH	-----	-----	Sample A	Oldpipe Register A
13	-----	BBBBH	-----	Sample B	Oldpipe Register B
14	-----	-----	CCCCH	Sample C	Oldpipe Register C
15	0000H	-----	-----	Control	Oldpipe Register A
16	-----	0000H	-----	Control	Oldpipe Register B
17	-----	-----	0000H	Control	Oldpipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected  = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 17.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB Section A, (082H)
BBBBH for Data Board AB Section B, (0C2H).
CCCCH for Data Board CD Section C, (092H).
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 4

TITLE: SAMPLE CLOCKS, 10ns CLOCK TEST

TARGET LOGIC: 3C 3F 3G 4C 4D 4E 4F 4G 5D

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Sample Clocks A, B and C, and 10ns Clock Enable bit are tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, toggling the 10ns Enable bit once, and then checking the Oldpipe Registers to see if a Data transfer took place.

NOTE:

The 10ns Enable bit is toggled active then inactive with two consecutive output instructions by the 8086 CPU. Since the 100Mhz Clock is so fast compared to the execution speed of the 8086, many Sample Clocks will occur during the short period that the 10ns Enable is active. This will not cause a problem, since the Oldpipe Register cannot overflow. (In this test sample clock is used for the new pipe and Oldpipe as well as the Sample register.)

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A	Oldpipe Register A
2	BBBBH	Sample B	Oldpipe Register B
3	CCCCH	Sample C	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Sample A	Oldpipe Registers A,B,C
5	0000H	BBBBH	0000H	Sample B	Oldpipe Registers A,B,C
6	0000H	0000H	CCCCH	Sample C	Oldpipe Registers A,B,C

Force disqualify test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	-----	-----	Sample A	Oldpipe Register A
8	-----	BBBBH	-----	Sample B	Oldpipe Register B
9	-----	-----	CCCCH	Sample C	Oldpipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
10 ns Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Sample A,
Sample B,
Sample C.

tttt is the test type: Functional,
Uniqueness,
Force Disqualify.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB.
BBBBH for Data Board AB.
CCCCH for Data Board CD.
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 5

TITLE: SAMPLE AND CONTROL CLOCKS, AJ, BJ AND CJ CLOCKS TEST

TARGET LOGIC: 3C 3D 3F 3G 3E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AJ, AJ/, BJ, BJ/, CJ and CJ/ clock enables for the Sample Clocks A, B and C and the Control Clock will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing three Sample Clocks by toggling one of the AJ, BJ, CJ Enables, and checking the Oldpipe Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing two Control Clocks by toggling one of the AJ,BJ,CJ Enables, and checking the Oldpipe Registers to see if a Data transfer took place.

NOTE:

The Logic states of AJ, AJ/, BJ, BJ/, CJ and CJ/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold will be used to provide the High and Low logic states.

This test will require the use of the Threshold Board and the probes.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AJ/,BJ/,CJ/	Oldpipe Register A
2	BBBBH	Sample B - AJ/,BJ/,CJ/	Oldpipe Register B
3	CCCCH	Sample C - AJ/,BJ/,CJ/	Oldpipe Register C
4	AAAAH	Control - AJ/,BJ/,CJ/	Oldpipe Register A
5	BBBBH	Control - AJ/,BJ/,CJ/	Oldpipe Register B
6	CCCCH	Control - AJ/,BJ/,CJ/	Oldpipe Register C
7	AAAAH	Sample A - AJ,BJ,CJ	Oldpipe Register A
8	BBBBH	Sample B - AJ,BJ,CJ	Oldpipe Register B
9	CCCCH	Sample C - AJ,BJ,CJ	Oldpipe Register C
10	AAAAH	Control - AJ,BJ,CJ	Oldpipe Register A
11	BBBBH	Control - AJ,BJ,CJ	Oldpipe Register B
12	CCCCH	Control - AJ,BJ,CJ	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AJ/	Oldpipe Registers A,B,C
14	AAAAH	0000H	0000H	Sample A - BJ/	Oldpipe Registers A,B,C
15	AAAAH	0000H	0000H	Sample A - CJ/	Oldpipe Registers A,B,C
16	0000H	BBBBH	0000H	Sample B - AJ/	Oldpipe Registers A,B,C
17	0000H	BBBBH	0000H	Sample B - BJ/	Oldpipe Registers A,B,C
18	0000H	BBBBH	0000H	Sample B - CJ/	Oldpipe Registers A,B,C
19	0000H	0000H	CCCCH	Sample C - AJ/	Oldpipe Registers A,B,C
20	0000H	0000H	CCCCH	Sample C - BJ/	Oldpipe Registers A,B,C
21	0000H	0000H	CCCCH	Sample C - CJ/	Oldpipe Registers A,B,C
22	AAAAH	BBBBH	CCCCH	Control - AJ/	Oldpipe Registers A,B,C
23	AAAAH	BBBBH	CCCCH	Control - BJ/	Oldpipe Registers A,B,C
24	AAAAH	BBBBH	CCCCH	Control - CJ/	Oldpipe Registers A,B,C
25	AAAAH	0000H	0000H	Sample A - AJ	Oldpipe Registers A,B,C
26	AAAAH	0000H	0000H	Sample A - BJ	Oldpipe Registers A,B,C
27	AAAAH	0000H	0000H	Sample A - CJ	Oldpipe Registers A,B,C
28	0000H	BBBBH	0000H	Sample B - AJ	Oldpipe Registers A,B,C
29	0000H	BBBBH	0000H	Sample B - BJ	Oldpipe Registers A,B,C
30	0000H	BBBBH	0000H	Sample B - CJ	Oldpipe Registers A,B,C
31	0000H	0000H	CCCCH	Sample C - AJ	Oldpipe Registers A,B,C
32	0000H	0000H	CCCCH	Sample C - BJ	Oldpipe Registers A,B,C
33	0000H	0000H	CCCCH	Sample C - CJ	Oldpipe Registers A,B,C
34	AAAAH	BBBBH	CCCCH	Control - AJ	Oldpipe Registers A,B,C
35	AAAAH	BBBBH	CCCCH	Control - BJ	Oldpipe Registers A,B,C
36	AAAAH	BBBBH	CCCCH	Control - CJ	Oldpipe Registers A,B,C

Threshold disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Oldpipe Registers A,B,C
38	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Oldpipe Registers A,B,C
39	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Oldpipe Registers A,B,C
40	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Oldpipe Registers A,B,C
41	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Oldpipe Registers A,B,C
42	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Oldpipe Registers A,B,C
43	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Oldpipe Registers A,B,C
44	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Oldpipe Registers A,B,C
45	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Oldpipe Registers A,B,C
46	0000H	0000H	0000H	Control - AJ/	Oldpipe Registers A,B,C
47	0000H	0000H	0000H	Control - BJ/	Oldpipe Registers A,B,C
48	0000H	0000H	0000H	Control - CJ/	Oldpipe Registers A,B,C
49	AAAAH	BBBBH	CCCCH	Sample A - AJ	Oldpipe Registers A,B,C
50	AAAAH	BBBBH	CCCCH	Sample A - BJ	Oldpipe Registers A,B,C
51	AAAAH	BBBBH	CCCCH	Sample A - CJ	Oldpipe Registers A,B,C
52	AAAAH	BBBBH	CCCCH	Sample B - AJ	Oldpipe Registers A,B,C
53	AAAAH	BBBBH	CCCCH	Sample B - BJ	Oldpipe Registers A,B,C
54	AAAAH	BBBBH	CCCCH	Sample B - CJ	Oldpipe Registers A,B,C
55	AAAAH	BBBBH	CCCCH	Sample C - AJ	Oldpipe Registers A,B,C
56	AAAAH	BBBBH	CCCCH	Sample C - BJ	Oldpipe Registers A,B,C
57	AAAAH	BBBBH	CCCCH	Sample C - CJ	Oldpipe Registers A,B,C
58	0000H	0000H	0000H	Control - AJ	Oldpipe Registers A,B,C
59	0000H	0000H	0000H	Control - BJ	Oldpipe Registers A,B,C
60	0000H	0000H	0000H	Control - CJ	Oldpipe Registers A,B,C

Force disqualify test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AJ/	Oldpipe Registers A,B,C
62	AAAAH	BBBBH	CCCCH	Sample A - BJ/	Oldpipe Registers A,B,C
63	AAAAH	BBBBH	CCCCH	Sample A - CJ/	Oldpipe Registers A,B,C
64	AAAAH	BBBBH	CCCCH	Sample B - AJ/	Oldpipe Registers A,B,C
65	AAAAH	BBBBH	CCCCH	Sample B - BJ/	Oldpipe Registers A,B,C
66	AAAAH	BBBBH	CCCCH	Sample B - CJ/	Oldpipe Registers A,B,C
67	AAAAH	BBBBH	CCCCH	Sample C - AJ/	Oldpipe Registers A,B,C
68	AAAAH	BBBBH	CCCCH	Sample C - BJ/	Oldpipe Registers A,B,C
69	AAAAH	BBBBH	CCCCH	Sample C - CJ/	Oldpipe Registers A,B,C
70	0000H	0000H	0000H	Control - AJ/	Oldpipe Registers A,B,C
71	0000H	0000H	0000H	Control - BJ/	Oldpipe Registers A,B,C
72	0000H	0000H	0000H	Control - CJ/	Oldpipe Registers A,B,C
73	AAAAH	BBBBH	CCCCH	Sample A - AJ	Oldpipe Registers A,B,C
74	AAAAH	BBBBH	CCCCH	Sample A - BJ	Oldpipe Registers A,B,C
75	AAAAH	BBBBH	CCCCH	Sample A - CJ	Oldpipe Registers A,B,C
76	AAAAH	BBBBH	CCCCH	Sample B - AJ	Oldpipe Registers A,B,C
77	AAAAH	BBBBH	CCCCH	Sample B - BJ	Oldpipe Registers A,B,C
78	AAAAH	BBBBH	CCCCH	Sample B - CJ	Oldpipe Registers A,B,C
79	AAAAH	BBBBH	CCCCH	Sample C - AJ	Oldpipe Registers A,B,C
80	AAAAH	BBBBH	CCCCH	Sample C - BJ	Oldpipe Registers A,B,C
81	AAAAH	BBBBH	CCCCH	Sample C - CJ	Oldpipe Registers A,B,C
82	0000H	0000H	0000H	Control - AJ	Oldpipe Registers A,B,C
83	0000H	0000H	0000H	Control - BJ	Oldpipe Registers A,B,C
84	0000H	0000H	0000H	Control - CJ	Oldpipe Registers A,B,C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify.

qqqq is the tested Clock Enable: AJ/ BJ/ CJ/,
AJ BJ CJ,
AJ/,
BJ/,
CJ/,
AJ,
BJ,
CJ.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB, (082H).
BBBBH for Data Board AB, (0C2H).
CCCCH for Data Board CD, (092H).
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 6

TITLE: SAMPLE AND CONTROL CLOCKS, AK, BK AND CK CLOCKS TEST

TARGET LOGIC: 5D 5E 5F 5G 5H

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AK, AK/, BK, BK/, CK and CK/ clock enables for the Sample Clocks A, B and C and the Control Clock will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Force Disqualify Disable.

The Sample Clocks are tested by placing Data at the Front End of the Data Board, issuing three Sample Clocks by toggling one of the AK, BK, CK Enables, and checking the Oldpipe Registers to see if a Data transfer took place.

The Control Clocks are similarly tested by clocking data into the Sample Registers, issuing two Control Clocks by toggling one of the AK, BK, CK Enables, and checking the Oldpipe Registers to see if a Data transfer occurred.

NOTE:

The Logic states of AK, AK/, BK, BK/, CK and CK/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold will be used to provide the High and Low logic states.

This test will require the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Sample A - AK/,BK/,CK/	Oldpipe Register A
2	BBBBH	Sample B - AK/,BK/,CK/	Oldpipe Register B
3	CCCCH	Sample C - AK/,BK/,CK/	Oldpipe Register C
4	AAAAH	Control - AK/,BK/,CK/	Oldpipe Register A
5	BBBBH	Control - AK/,BK/,CK/	Oldpipe Register B
6	CCCCH	Control - AK/,BK/,CK/	Oldpipe Register C
7	AAAAH	Sample A - AK,BK,CK	Oldpipe Register A
8	BBBBH	Sample B - AK,BK,CK	Oldpipe Register B
9	CCCCH	Sample C - AK,BK,CK	Oldpipe Register C
10	AAAAH	Control - AK,BK,CK	Oldpipe Register A
11	BBBBH	Control - AK,BK,CK	Oldpipe Register B
12	CCCCH	Control - AK,BK,CK	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
13	AAAAH	0000H	0000H	Sample A - AK/	Oldpipe Registers A,B,C
14	AAAAH	0000H	0000H	Sample A - BK/	Oldpipe Registers A,B,C
15	AAAAH	0000H	0000H	Sample A - CK/	Oldpipe Registers A,B,C
16	0000H	BBBBH	0000H	Sample B - AK/	Oldpipe Registers A,B,C
17	0000H	BBBBH	0000H	Sample B - BK/	Oldpipe Registers A,B,C
18	0000H	BBBBH	0000H	Sample B - CK/	Oldpipe Registers A,B,C
19	0000H	0000H	CCCCH	Sample C - AK/	Oldpipe Registers A,B,C
20	0000H	0000H	CCCCH	Sample C - BK/	Oldpipe Registers A,B,C
21	0000H	0000H	CCCCH	Sample C - CK/	Oldpipe Registers A,B,C
22	AAAAH	BBBBH	CCCCH	Control - AK/	Oldpipe Registers A,B,C
23	AAAAH	BBBBH	CCCCH	Control - BK/	Oldpipe Registers A,B,C
24	AAAAH	BBBBH	CCCCH	Control - CK/	Oldpipe Registers A,B,C
25	AAAAH	0000H	0000H	Sample A - AK	Oldpipe Registers A,B,C
26	AAAAH	0000H	0000H	Sample A - BK	Oldpipe Registers A,B,C
27	AAAAH	0000H	0000H	Sample A - CK	Oldpipe Registers A,B,C
28	0000H	BBBBH	0000H	Sample B - AK	Oldpipe Registers A,B,C
29	0000H	BBBBH	0000H	Sample B - BK	Oldpipe Registers A,B,C
30	0000H	BBBBH	0000H	Sample B - CK	Oldpipe Registers A,B,C
31	0000H	0000H	CCCCH	Sample C - AK	Oldpipe Registers A,B,C
32	0000H	0000H	CCCCH	Sample C - BK	Oldpipe Registers A,B,C
33	0000H	0000H	CCCCH	Sample C - CK	Oldpipe Registers A,B,C
34	AAAAH	BBBBH	CCCCH	Control - AK	Oldpipe Registers A,B,C
35	AAAAH	BBBBH	CCCCH	Control - BK	Oldpipe Registers A,B,C
36	AAAAH	BBBBH	CCCCH	Control - CK	Oldpipe Registers A,B,C

Threshold disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
37	AAAAH	BBBBH	CCCCH	Sample A - AK/	Oldpipe Registers A,B,C
38	AAAAH	BBBBH	CCCCH	Sample A - BK/	Oldpipe Registers A,B,C
39	AAAAH	BBBBH	CCCCH	Sample A - CK/	Oldpipe Registers A,B,C
40	AAAAH	BBBBH	CCCCH	Sample B - AK/	Oldpipe Registers A,B,C
41	AAAAH	BBBBH	CCCCH	Sample B - BK/	Oldpipe Registers A,B,C
42	AAAAH	BBBBH	CCCCH	Sample B - CK/	Oldpipe Registers A,B,C
43	AAAAH	BBBBH	CCCCH	Sample C - AK/	Oldpipe Registers A,B,C
44	AAAAH	BBBBH	CCCCH	Sample C - BK/	Oldpipe Registers A,B,C
45	AAAAH	BBBBH	CCCCH	Sample C - CK/	Oldpipe Registers A,B,C
46	0000H	0000H	0000H	Control - AK/	Oldpipe Registers A,B,C
47	0000H	0000H	0000H	Control - BK/	Oldpipe Registers A,B,C
48	0000H	0000H	0000H	Control - CK/	Oldpipe Registers A,B,C
49	AAAAH	BBBBH	CCCCH	Sample A - AK	Oldpipe Registers A,B,C
50	AAAAH	BBBBH	CCCCH	Sample A - BK	Oldpipe Registers A,B,C
51	AAAAH	BBBBH	CCCCH	Sample A - CK	Oldpipe Registers A,B,C
52	AAAAH	BBBBH	CCCCH	Sample B - AK	Oldpipe Registers A,B,C
53	AAAAH	BBBBH	CCCCH	Sample B - BK	Oldpipe Registers A,B,C
54	AAAAH	BBBBH	CCCCH	Sample B - CK	Oldpipe Registers A,B,C
55	AAAAH	BBBBH	CCCCH	Sample C - AK	Oldpipe Registers A,B,C
56	AAAAH	BBBBH	CCCCH	Sample C - BK	Oldpipe Registers A,B,C
57	AAAAH	BBBBH	CCCCH	Sample C - CK	Oldpipe Registers A,B,C
58	0000H	0000H	0000H	Control - AK	Oldpipe Registers A,B,C
59	0000H	0000H	0000H	Control - BK	Oldpipe Registers A,B,C
60	0000H	0000H	0000H	Control - CK	Oldpipe Registers A,B,C

Force disqualify test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
61	AAAAH	BBBBH	CCCCH	Sample A - AK/	Oldpipe Registers A,B,C
62	AAAAH	BBBBH	CCCCH	Sample A - BK/	Oldpipe Registers A,B,C
63	AAAAH	BBBBH	CCCCH	Sample A - CK/	Oldpipe Registers A,B,C
64	AAAAH	BBBBH	CCCCH	Sample B - AK/	Oldpipe Registers A,B,C
65	AAAAH	BBBBH	CCCCH	Sample B - BK/	Oldpipe Registers A,B,C
66	AAAAH	BBBBH	CCCCH	Sample B - CK/	Oldpipe Registers A,B,C
67	AAAAH	BBBBH	CCCCH	Sample C - AK/	Oldpipe Registers A,B,C
68	AAAAH	BBBBH	CCCCH	Sample C - BK/	Oldpipe Registers A,B,C
69	AAAAH	BBBBH	CCCCH	Sample C - CK/	Oldpipe Registers A,B,C
70	0000H	0000H	0000H	Control - AK/	Oldpipe Registers A,B,C
71	0000H	0000H	0000H	Control - BK/	Oldpipe Registers A,B,C
72	0000H	0000H	0000H	Control - CK/	Oldpipe Registers A,B,C
73	AAAAH	BBBBH	CCCCH	Sample A - AK	Oldpipe Registers A,B,C
74	AAAAH	BBBBH	CCCCH	Sample A - BK	Oldpipe Registers A,B,C
75	AAAAH	BBBBH	CCCCH	Sample A - CK	Oldpipe Registers A,B,C
76	AAAAH	BBBBH	CCCCH	Sample B - AK	Oldpipe Registers A,B,C
77	AAAAH	BBBBH	CCCCH	Sample B - BK	Oldpipe Registers A,B,C
78	AAAAH	BBBBH	CCCCH	Sample B - CK	Oldpipe Registers A,B,C
79	AAAAH	BBBBH	CCCCH	Sample C - AK	Oldpipe Registers A,B,C
80	AAAAH	BBBBH	CCCCH	Sample C - BK	Oldpipe Registers A,B,C
81	AAAAH	BBBBH	CCCCH	Sample C - CK	Oldpipe Registers A,B,C
82	0000H	0000H	0000H	Control - AK	Oldpipe Registers A,B,C
83	0000H	0000H	0000H	Control - BK	Oldpipe Registers A,B,C
84	0000H	0000H	0000H	Control - CK	Oldpipe Registers A,B,C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 84.

cccc is the tested Clock: Sample A,
Sample B,
Sample C,
Control.

tttt is the test type: Functional,
Uniqueness,
Disable,
Force Disqualify.

qqqq is the tested Clock Enable: AK/ BK/ CK/,
AK BK CK,
AK/,
BK/,
CK/,
AK,
BK,
CK.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the oldpipe Register which should be:
AAAAH for Data Board AB, (082H).
BBBBH for Data Board AB, (0C2H).
CCCCH for Data Board CD, (092H).
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 7

TITLE: LATCH CLOCKS, DIAGNOSTIC INTERNAL CLOCK TEST

TARGET LOGIC: 2B 2E 1D 2C 2D
1H 2G 2F 2H 1E 1J

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Diagnostic Internal Latch Clocks A, B and C will be tested for functionality as well as the ability to disable these Clocks using the Normal Disable, and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board,issuing a Diagnostic Latch Clock, issuing three Diagnostic Sample Clocks,and checking the Oldpipe Registers to see if a Data transfer took place.

NOTE:

The Diagnostic Latch Clock is "kicked" by outputing a "1" to bit D1 of Write Register 0B8H of the Clock Board. This produces a clock pulse the width of the 8086's Write pulse. Consecutive "kicks" can be achieved by consecutive outputs to this port. It is not necessary to ever set this bit low.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	0000H	Latch A,B,C	Oldpipe Registers A,B,C
2	5555H	Latch A,B,C	Oldpipe Registers A,B,C
3	AAAAH	Latch A,B,C	Oldpipe Registers A,B,C
4	CCCCH	Latch A,B,C	Oldpipe Registers A,B,C
5	3333H	Latch A,B,C	Oldpipe Registers A,B,C
6	6666H	Latch A,B,C	Oldpipe Registers A,B,C
7	9999H	Latch A,B,C	Oldpipe Registers A,B,C
8	FFFFH	Latch A,B,C	Oldpipe Registers A,B,C

Threshold disable test:

Step	Data	Clock Tested	Data Verified at
9	AAAAH	Latch A	Oldpipe Register A
10	BBBBH	Latch B	Oldpipe Register B
11	CCCCH	Latch C	Oldpipe Register C

Latch disqualify disable test:

Step	Data	Clock Tested	Data Verified at
12	AAAAH	Latch A	Oldpipe Register A
13	BBBBH	Latch B	Oldpipe Register B
14	CCCCH	Latch C	Oldpipe Register C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
Diagnostic Latch Clock
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 14.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Threshold Disable,
Disqualify Disable.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
Data for Functional Testing:
0000H,
5555H,
AAAAH,
CCCCH,
3333H,
6666H,
9999H,
FFFFH.
Data for Threshold Disable and Disqualify Disable Testing:
AAAAH for Data Board AB Section A.
BBBBH for Data Board AB Section B.
CCCCH for Data Board CD Section C.

Clock Board Diagnostic Subtest 8

TITLE: LATCH CLOCKS, DIAGNOSTIC OR-ONLY ENABLES TEST

TARGET LOGIC: 1E 2F

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Latch Clocks A, B and C OR-Only Enables will be tested for functionality, uniqueness, and the ability to disable these Clocks using the the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Diagnostic Latch Clock, issuing three Diagnostic Sample Clocks and checking the Oldpipe Registers to see if a Data transfer took place.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A	Oldpipe Register A
2	BBBBH	Latch B	Oldpipe Register B
3	CCCCH	Latch C	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
4	AAAAH	0000H	0000H	Latch A	Oldpipe Registers A,B,C
5	0000H	BBBBH	0000H	Latch B	Oldpipe Registers A,B,C
6	0000H	0000H	CCCCH	Latch C	Oldpipe Registers A,B,C

Latch disqualify disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	BBBBH	CCCCH	Latch A	Oldpipe Registers A,B,C
8	AAAAH	BBBBH	CCCCH	Latch B	Oldpipe Registers A,B,C
9	AAAAH	BBBBH	CCCCH	Latch C	Oldpipe Registers A,B,C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
OR Only Enables
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 9.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Latch Disqualify Disable.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB Section A.
BBBBH for Data Board AB Section B.
CCCCH for Data Board CD Section C.

0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 9

TITLE: LATCH CLOCKS, AR, BR AND CR CLOCKS TEST

TARGET LOGIC: 1D 1F 1G 1H 1J 2F 2G 2H

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AR, AR/, BR, BR/, CR and CR/ Clock Enables for Latch Clocks A, B and C will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable, and the Latch Disqualify Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, issuing a Latch Clock by toggling one of the AR, BR, CR Enables, and issuing three Diagnostic Internal Sample Clocks. The Oldpipe Registers are then checked to see if a Data transfer took place.

NOTE:

The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARIABLE A Threshold will be used to provide the High and Low logic states.

This test will require the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AR/,BR/,CR/	Oldpipe Register A
2	BBBBH	Latch B - AR/,BR/,CR/	Oldpipe Register B
3	CCCCH	Latch C - AR/,BR/,CR/	Oldpipe Register C
4	AAAAH	Latch A - AR,BR,CR	Oldpipe Register A
5	BBBBH	Latch B - AR,BR,CR	Oldpipe Register B
6	CCCCH	Latch C - AR,BR,CR	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AR/	Oldpipe Registers A,B,C
8	AAAAH	0000H	0000H	Latch A - BR/	Oldpipe Registers A,B,C
9	AAAAH	0000H	0000H	Latch A - CR/	Oldpipe Registers A,B,C
10	0000H	BBBBH	0000H	Latch B - AR/	Oldpipe Registers A,B,C

11	0000H	BBBBH	0000H	Latch B - BR/	Oldpipe Registers A,B,C
12	0000H	BBBBH	0000H	Latch B - CR/	Oldpipe Registers A,B,C
13	0000H	0000H	CCCCH	Latch C - AR/	Oldpipe Registers A,B,C
14	0000H	0000H	CCCCH	Latch C - BR/	Oldpipe Registers A,B,C
15	0000H	0000H	CCCCH	Latch C - CR/	Oldpipe Registers A,B,C
16	AAAAH	0000H	0000H	Latch A - AR	Oldpipe Registers A,B,C
17	AAAAH	0000H	0000H	Latch A - BR	Oldpipe Registers A,B,C
18	AAAAH	0000H	0000H	Latch A - CR	Oldpipe Registers A,B,C
19	0000H	BBBBH	0000H	Latch B - AR	Oldpipe Registers A,B,C
20	0000H	BBBBH	0000H	Latch B - BR	Oldpipe Registers A,B,C
21	0000H	BBBBH	0000H	Latch B - CR	Oldpipe Registers A,B,C
22	0000H	0000H	CCCCH	Latch C - AR	Oldpipe Registers A,B,C
23	0000H	0000H	CCCCH	Latch C - BR	Oldpipe Registers A,B,C
24	0000H	0000H	CCCCH	Latch C - CR	Oldpipe Registers A,B,C

Threshold disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AR/	Oldpipe Registers A,B,C
26	AAAAH	BBBBH	CCCCH	Latch A - BR/	Oldpipe Registers A,B,C
27	AAAAH	BBBBH	CCCCH	Latch A - CR/	Oldpipe Registers A,B,C
28	AAAAH	BBBBH	CCCCH	Latch B - AR/	Oldpipe Registers A,B,C
29	AAAAH	BBBBH	CCCCH	Latch B - BR/	Oldpipe Registers A,B,C
30	AAAAH	BBBBH	CCCCH	Latch B - CR/	Oldpipe Registers A,B,C
31	AAAAH	BBBBH	CCCCH	Latch C - AR/	Oldpipe Registers A,B,C
32	AAAAH	BBBBH	CCCCH	Latch C - BR/	Oldpipe Registers A,B,C
33	AAAAH	BBBBH	CCCCH	Latch C - CR/	Oldpipe Registers A,B,C
34	AAAAH	BBBBH	CCCCH	Latch A - AR	Oldpipe Registers A,B,C
35	AAAAH	BBBBH	CCCCH	Latch A - BR	Oldpipe Registers A,B,C
36	AAAAH	BBBBH	CCCCH	Latch A - CR	Oldpipe Registers A,B,C
37	AAAAH	BBBBH	CCCCH	Latch B - AR	Oldpipe Registers A,B,C
38	AAAAH	BBBBH	CCCCH	Latch B - BR	Oldpipe Registers A,B,C
39	AAAAH	BBBBH	CCCCH	Latch B - CR	Oldpipe Registers A,B,C
40	AAAAH	BBBBH	CCCCH	Latch C - AR	Oldpipe Registers A,B,C
41	AAAAH	BBBBH	CCCCH	Latch C - BR	Oldpipe Registers A,B,C
42	AAAAH	BBBBH	CCCCH	Latch C - CR	Oldpipe Registers A,B,C

Latch disqualify disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
43	AAAAH	BBBBH	CCCCH	Latch A - AR/	Oldpipe Registers A,B,C
44	AAAAH	BBBBH	CCCCH	Latch A - BR/	Oldpipe Registers A,B,C
45	AAAAH	BBBBH	CCCCH	Latch A - CR/	Oldpipe Registers A,B,C
46	AAAAH	BBBBH	CCCCH	Latch B - AR/	Oldpipe Registers A,B,C
47	AAAAH	BBBBH	CCCCH	Latch B - BR/	Oldpipe Registers A,B,C
48	AAAAH	BBBBH	CCCCH	Latch B - CR/	Oldpipe Registers A,B,C
49	AAAAH	BBBBH	CCCCH	Latch C - AR/	Oldpipe Registers A,B,C
50	AAAAH	BBBBH	CCCCH	Latch C - BR/	Oldpipe Registers A,B,C
51	AAAAH	BBBBH	CCCCH	Latch C - CR/	Oldpipe Registers A,B,C
52	AAAAH	BBBBH	CCCCH	Latch A - AR	Oldpipe Registers A,B,C
53	AAAAH	BBBBH	CCCCH	Latch A - BR	Oldpipe Registers A,B,C
54	AAAAH	BBBBH	CCCCH	Latch A - CR	Oldpipe Registers A,B,C
55	AAAAH	BBBBH	CCCCH	Latch B - AR	Oldpipe Registers A,B,C

56	AAAAH	BBBBH	CCCCH	Latch B - BR	Oldpipe Registers A,B,C
57	AAAAH	BBBBH	CCCCH	Latch B - CR	Oldpipe Registers A,B,C
58	AAAAH	BBBBH	CCCCH	Latch C - AR	Oldpipe Registers A,B,C
59	AAAAH	BBBBH	CCCCH	Latch C - BR	Oldpipe Registers A,B,C
60	AAAAH	BBBBH	CCCCH	Latch C - CR	Oldpipe Registers A,B,C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 60.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Threshold Disable,
Latch Disqualify Disable.

qqqq is the tested Clock Enable: AR/ BR/ CR/,
AR BR CR,
AR/,
BR/,
CR/,
AR,
BR,
CR.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB Section A.
BBBBH for Data Board AB Section B.
CCCCH for Data Board CD Section C.
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 10

TITLE: LATCH CLOCKS, AS, BS AND CS CLOCKS TEST

TARGET LOGIC: 10 1E 2B 2C 2D 2E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The AS, AS/, BS, BS/, CS and CS/ Clock Enables for Latch Clocks A, B and C will be tested for functionality and uniqueness, as well as the ability to disable these Clocks using the Threshold Disable.

The Latch Clocks are tested by placing Data at the Front End of the Data Board, asserting the appropriate AS,BS,CS Enables, issuing a Diagnostic Latch Clock, and issuing three Diagnostic Internal Sample Clocks. The Oldpipe Registers are then checked to see if a Data transfer took place.

NOTE 1:

This test is different from previous tests due to the transparent mode of the 10130 Latches on the Data Boards. When the Latch Clock is held in a low state, the 10130 Latches on the Data Board are transparent, i.e., the "Q" output follows the "D" input. When the Latch Clock goes high, this latches the Data into the 10130's and the "D" input then becomes a don't care.

In this test, instead of toggling the enable to the AS, BS or CS, it will be held active and a Diagnostic Int Clock issued. This will cause the Data Board to be in Latch Mode, instead of being transparent.

NOTE 2:

The Logic states of AR, AR/, BR, BR/, CR and CR/ are determined by the current threshold at the probes. An ECL Threshold, and a VARAIABLE A Threshold will be used to provide the High and Low logic states.

This test will require the use of the Threshold Board, and the probes.

TEST STEP INFORMATION:

Functionality test:

Step	Data	Clock Tested	Data Verified at
1	AAAAH	Latch A - AS/,BS/,CS/	Oldpipe Register A
2	BBBBH	Latch B - AS/,BS/,CS/	Oldpipe Register B
3	CCCCH	Latch C - AS/,BS/,CS/	Oldpipe Register C
4	AAAAH	Latch A - AS,BS,CS	Oldpipe Register A

5	BBBBH	Latch B - AS,BS,CS	Oldpipe Register B
6	CCCCH	Latch C - AS,BS,CS	Oldpipe Register C

Uniqueness test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
7	AAAAH	0000H	0000H	Latch A - AS/	Oldpipe Registers A,B,C
8	AAAAH	0000H	0000H	Latch A - BS/	Oldpipe Registers A,B,C
9	AAAAH	0000H	0000H	Latch A - CS/	Oldpipe Registers A,B,C
10	0000H	BBBBH	0000H	Latch B - AS/	Oldpipe Registers A,B,C
11	0000H	BBBBH	0000H	Latch B - BS/	Oldpipe Registers A,B,C
12	0000H	BBBBH	0000H	Latch B - CS/	Oldpipe Registers A,B,C
13	0000H	0000H	CCCCH	Latch C - AS/	Oldpipe Registers A,B,C
14	0000H	0000H	CCCCH	Latch C - BS/	Oldpipe Registers A,B,C
15	0000H	0000H	CCCCH	Latch C - CS/	Oldpipe Registers A,B,C
16	AAAAH	0000H	0000H	Latch A - AS	Oldpipe Registers A,B,C
17	AAAAH	0000H	0000H	Latch A - BS	Oldpipe Registers A,B,C
18	AAAAH	0000H	0000H	Latch A - CS	Oldpipe Registers A,B,C
19	0000H	BBBBH	0000H	Latch B - AS	Oldpipe Registers A,B,C
20	0000H	BBBBH	0000H	Latch B - BS	Oldpipe Registers A,B,C
21	0000H	BBBBH	0000H	Latch B - CS	Oldpipe Registers A,B,C
22	0000H	0000H	CCCCH	Latch C - AS	Oldpipe Registers A,B,C
23	0000H	0000H	CCCCH	Latch C - BS	Oldpipe Registers A,B,C
24	0000H	0000H	CCCCH	Latch C - CS	Oldpipe Registers A,B,C

Threshold disable test:

Step	A Data	B Data	C Data	Clock Tested	Data Verified at
25	AAAAH	BBBBH	CCCCH	Latch A - AS/	Oldpipe Registers A,B,C
26	AAAAH	BBBBH	CCCCH	Latch A - BS/	Oldpipe Registers A,B,C
27	AAAAH	BBBBH	CCCCH	Latch A - CS/	Oldpipe Registers A,B,C
28	AAAAH	BBBBH	CCCCH	Latch B - AS/	Oldpipe Registers A,B,C
29	AAAAH	BBBBH	CCCCH	Latch B - BS/	Oldpipe Registers A,B,C
30	AAAAH	BBBBH	CCCCH	Latch B - CS/	Oldpipe Registers A,B,C
31	AAAAH	BBBBH	CCCCH	Latch C - AS/	Oldpipe Registers A,B,C
32	AAAAH	BBBBH	CCCCH	Latch C - BS/	Oldpipe Registers A,B,C
33	AAAAH	BBBBH	CCCCH	Latch C - CS/	Oldpipe Registers A,B,C
34	AAAAH	BBBBH	CCCCH	Latch A - AS	Oldpipe Registers A,B,C
35	AAAAH	BBBBH	CCCCH	Latch A - BS	Oldpipe Registers A,B,C
36	AAAAH	BBBBH	CCCCH	Latch A - CS	Oldpipe Registers A,B,C
37	AAAAH	BBBBH	CCCCH	Latch B - AS	Oldpipe Registers A,B,C
38	AAAAH	BBBBH	CCCCH	Latch B - BS	Oldpipe Registers A,B,C
39	AAAAH	BBBBH	CCCCH	Latch B - CS	Oldpipe Registers A,B,C
40	AAAAH	BBBBH	CCCCH	Latch C - AS	Oldpipe Registers A,B,C
41	AAAAH	BBBBH	CCCCH	Latch C - BS	Oldpipe Registers A,B,C
42	AAAAH	BBBBH	CCCCH	Latch C - CS	Oldpipe Registers A,B,C

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
cccc Clock tttt Error
qqqq Clock Enable
I/O Address      = aaaaH
Status Read      = rrrrH
Status Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 42.

cccc is the tested Clock: Latch A,
Latch B,
Latch C.

tttt is the test type: Functional,
Uniqueness,
Threshold Disable.

qqqq is the tested Clock Enable: AS/ BS/ CS/,
AS BS CS,
AS/,
BS/,
CS/,
AS,
BS,
CS.

aaaa is the address of a Data Board Oldpipe Register:
082H for Data Board AB Section A
0C2H for Data Board AB Section B
092H for Data Board CD Section C

rrrr is the Data Word read from the Status Register.

eeee is the Data Word expected from the Oldpipe Register which should be:
AAAAH for Data Board AB Section A.
BBBBH for Data Board AB Section B.
CCCCH for Data Board CD Section C.
0000H for all Data Boards during Uniqueness Testing.

Clock Board Diagnostic Subtest 11

TITLE: DECADE FREQUENCY AND MULTIPLIER DIVIDE BY TEST

TARGET LOGIC: 10D 12C 11C
10C
11B
9E 10E 9C 9D

Setup Latches in Subtest 2

100Mhz Oscilator Descrete componets (Grid 8B-6B)

TEST DESCRIPTION:

This test will check the Clock Decade multiplexer (Decade) and the divide by counter (Multiplier).

The 100Mhz, 10Mhz, 1Mhz, 100Khz, 10Khz, 1Khz and 100hz Clocks will be tested with various Multipliers. The Clock frequencies will be verified within a ballpark range, but this will only verify that the multiplexer is selecting different Decades. A frequency counter is required to adjust/verify the Time Period of the 100Mhz Clock.

When the faster Clock frequencies are being tested, the testing time is very quick, and the following message will be displayed:

>Counting Clock Pulses...

During the 1Khz test, (this one takes a while), the following message will be displayed:

>Counting Clock Pulses... 4 seconds

During the 100hz test, (this one takes a long time), the following message will be displayed:

>Counting Clock Pulses...20 seconds

During the testing of the Multiplier Divide by counter, the following message will be displayed:

>Checking the Multiplier Divide by...

TEST STEP INFORMATION:

Decade frequency test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
1	0	8	256	128	384
2	1	8	256	128	384
3	2	8	256	128	384
4	3	8	256	128	384
5	4	8	256	128	384
6	5	8	256	128	384
7	6	8	256	128	384

Multiplier devide by test:

Step	Decade	Mult	Clks Expected	Clks Minimum	Clks Maximum
8	3	0	~83	0	512
9	3	1	~89	Step 8 Clock Count	512
10	3	2	~95	Step 9 Clock Count	512
11	3	3	~97	Step 10 Clock Count	512
12	3	4	~111	Step 11 Clock Count	512
13	3	5	~122	Step 12 Clock Count	512
14	3	6	~134	Step 13 Clock Count	512
15	3	7	~148	Step 14 Clock Count	512
16	3	8	~167	Step 15 Clock Count	512
17	3	9	~191	Step 16 Clock Count	512
18	3	10	~224	Step 17 Clock Count	512
19	3	11	~270	Step 18 Clock Count	512
20	3	12	~336	Step 19 Clock Count	512
21	3	13	~450	Step 20 Clock Count	512
22 *	3	14	256	0	512
23 *	3	15	256	0	512

NOTE 1:

The values above preceeded by ~ are aproximate values. They were selected by running the test a single time on a single K450B. This value will vary from System to System due to minor differences in the CPU's Clock frequency, and other hardware propagation times. The precise values are not important as long as Clock count increments while the Multiplier incrementes.

NOTE 2:

Test Steps 22 and 23 are a little different from the rest. When the Multiplier goes from 13 to 14, and from 14 to 15, the Clock count no longer follows the slow-linear increase that it followed with the Multiplier range of 0 to 12. The Clock count aproximately doubles, so a ballparking method of 256 clocks inside the 0 to 512 range is used.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg Error
Decade x:  ffff Clock
Multiplier      = mmmmD
Clocks counted  = ccccD
Min Clock count = llllD
Max Clock count = hhhhD
```

Where:

ssss is the Test Step in the range: 1 to 23.

hmsg is "Clock Frequency Counting",
"Multiplier Clock Divide by".

x is the selected Decade: 0, 1, 2, 3, 4, 5, 6.

ffff is the Clock frequency:
100Mhz,
10Mhz,
1Mhz,
100Khz,
10Khz,
1Khz,
100hz.

mmmm is the current Multiplier value, range is 0 to 15.

cccc is the Number of clocks counted, range is 0 to 512.

llll is the Minimum number of clocks that could be counted for frequency.

hhhh is the Maximum number of clocks that could be counted for frequency.

Clock Board Diagnostic Subtest 12

TITLE: LEVEL RAMS DATA INTEGRITY TEST

TARGET LOGIC: 11E 11F
11J
12F 12G
12D 10D 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs on the Clock Board are organized as two 1024 x 4. They are written to by the Control Board, and read into the highest nibble of the word from port B0H of the Clock Board.

The Level RAM's Data Integrity will be checked by writing all 16 possible values to the RAM, and reading it back to verify that each Data Bit is functional and unique.

TEST STEP INFORMATION:

Data integrity test:

Step	Data	Address Locations
1	0000H	000 - 1023
2	0001H	000 - 1023
3	0002H	000 - 1023
4	0003H	000 - 1023
5	0004H	000 - 1023
6	0005H	000 - 1023
7	0006H	000 - 1023
8	0007H	000 - 1023
9	0008H	000 - 1023
10	0009H	000 - 1023
11	000AH	000 - 1023
12	000BH	000 - 1023
13	000CH	000 - 1023
14	000DH	000 - 1023
15	000EH	000 - 1023
16	000FH	000 - 1023

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Data Integrity Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 16.

cccc is RAM byte count, (address) in the range of 0 to 2048.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Clock Board Diagnostic Subtest 13

TITLE: LEVEL RAMS ADDRESS INTEGRITY TEST

TARGET LOGIC: 11D
11G 12H
11E 11F
11J
12F 12G 12J
12D 10D 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

The Level RAMs address is provided by dual counters which provide 10 address lines which can address 1024 locations. An additions flip flop toggles back and forth between the two 10474 RAM Chips on each Write/Read, to allow the access of 2048 RAM locations.

The Level RAMs will be tested for addressing uniqueness. This will verify that each of 2048 locations can be written to independantly of all others.

TEST STEP INFORMATION:

Step 1. An incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 16 locations. This verifies address lines A0, A1, A2 and A3.

Step 2. A Block Incrementing Data pattern from 00H to 0FH is written to RAM, which repeats after each 1024 locations. This verifies address lines A4, A5, A6 ,A7, A8, and A9.

Step 3. A Block Data pattern of 05H and 0AH is written to RAM, which covers all 2048 locations. This verifies that both of the 10474 RAM chips are written to.

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
Level RAM Address Uniqueness Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:
ssss is the Test Step in the range: 1 to 3.

cccc is RAM byte count, (address) in the range of 0 to 2047.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Clock Board Diagnostic Subtest 14

TITLE: LEVEL RAM CONTROL TEST

TARGET LOGIC: 11D
11G 12H 12J
11E 11F
11J
12F 12G
12D 10D 12E

Setup Latches in Subtest 2

TEST DESCRIPTION:

This Subtest verifies the functionality of the Control Logic associated with the Level RAM.

The First Test Step checks the odd/even toggling of the level ram. Each Consecutive write operation to the RAM should toggle back and forth between the "Even 10474" RAM chip, and the "ODD 10474" RAM chip. A "D" latch is acting as a flip flop, and providing a write enable signal to only one RAM chip. A 0AH will be written to all Even addresses and a 05H is written to all Odd Addresses.

The Second Test Step checks the Level RAM Write Enable/Disable function. The Level RAM is Write enabled when the signals 'ARMED' and 'TRACED' from the Control Board are both active.

This test performs 7 writes with the following conditions:

LEVEL	ARMED	TRACED	RESULT
0	1	1	0
1	1	1	1
2	1	0	not recorded
3	1	0	not recorded
4	1	1	4
5	1	1	5
5	0	1	not recorded

The Third Test Step checks the Recirculation feature of the Level RAM. The Data is read out of the 10474 RAM chips, looped back, and written back in. This is checked by writing an incrementing pattern into the RAM, and then reading it back, verifying the Data Integrity.

The Data is read back a second time and verified. On the second read, the Data will be shifted by one Address location from the Recirculation.

The Fourth Test Step checks the Level RAM reset persistence by first filling the RAM with a value of 00H, then holding the reset line to the RAM address counters active, and hammering address location 0 by performing 1024 consecutive write operations. This should modify the Data Value at location 0, but the other 1023 locations should be unchanged. All 1024 locations are read back and verified.

TEST STEP INFORMATION:

Step	Data Even Locations	Data Odd Locations
1	000AH	0005H

Step	Data	Address	
2	0000H	000	
	0001H	001	
	0004H	002	
	0005H	003	
Step	Data	Address	
4	0005H	000	(0005H in Location 000 Only)
	0000H	001	
	0000H	002	
	.	.	
	.	.	
	0000H	1022	
	0000H	1023	

ERROR MESSAGES:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step   ssss
hmsg Error
Diagnostic Internal Clock
Byte Count     = ccccD
Data Read      = rrrrH
Data Expected = eeeeH
```

Where:

ssss is the Test Step in the range: 1 to 4.

hmsg is Level RAM odd/even Toggle,
Level RAM Write enable/disable,
Level RAM Recirculation,
Level RAM Hammer/Addr Reset.

cccc is RAM byte count, (address) in the range of 0 to 1023.

rrrr is the Data Word read from the Level RAMS.

eeee is the Data Word expected from the Level RAMS which should be:

Odd/Even Test:
0005H,
000AH.

Write Disable/Enable Test:
0000H,
0001H,
0004H,
0005H.

Recirculation Test:
0000H,
0001H,
0002H,
0003H,
0004H,
0005H,
0006H,
0007H,
0008H,
0009H,
000AH,
000BH,
000CH,
000DH,
000EH,
000FH.

Hammer/Address Reset Test:
0005H,
0000H.

DIAGNOSTIC OVERVIEW

This section describes the subtests executed on the K450B Threshold/GPIB/RS232 Board and the associated error reporting.

The Threshold/GPIB/RS232 board diagnostics is divided into nine subtests, each of which is described individually on the following pages.

Subtest 1 is a DAC 7541 linearity test. Subtest 2 is a DAC 7533 linearity test. Subtest 3 is a Multiplexer/threshold test. Subtest 4 is a serial I/O #1 test. Subtest 5 is a serial I/O #2 test. Subtest 6 is a 8253 counter 0 mode 1 test.

Subtests 7 through subtest 9 are GPIB internal logic tests. The GPIB cable and operator intervene flag should not be set. Subtest 7 is the GPIB control status test. Subtest 8 is GPIB MPU interrupt logic test. Subtest 9 is GPIB data out register and parallel poll response register test.

Only a part of the GPIB logic is checked by the GPIB internal test. The subtests 7 through 9 will check internal logic only. External handshake logic is not tested.

NOTE: The 'TARGET LOGIC' listed in each subtest description does not necessarily include all of the logic which could affect the operation of the subtest.

SUBTEST CATEGORY

1. DAC 7541 LINEARITY TEST
2. DAC 7533 LINEARITY TEST
3. MUX/THRESHOLD LOGIC TEST
4. SERIAL I/O #1 TEST
5. SERIAL I/O #2 TEST
6. TIMER 8253 COUNTER 0 TEST
7. GPIB INTERNAL CONTROL LINE TEST
8. GPIB INTERNAL MPU INTERRUPT LOGIC TEST
9. GPIB INTERNAL DATA REGISTER TEST

ERROR COUNT CATEGORY

1. SUBTEST 1 ERROR COUNT.
2. SUBTEST 2 ERROR COUNT.
3. SUBTEST 3 ERROR COUNT.
4. SUBTEST 4 ERROR COUNT.
5. SUBTEST 5 ERROR COUNT.
6. SUBTEST 6 ERROR COUNT.
7. SUBTEST 7 ERROR COUNT.
8. SUBTEST 8 ERROR COUNT.
9. SUBTEST 9 ERROR COUNT.
10. SUBTEST 10 ERROR COUNT.

Threshold Diagnostic Subtest 1

TITLE: DAC 7541 LINEARITY TEST

TARGET LOGIC: 5E,6E,8B,7F,8F,8A,12F
7A,7E,Q2
and power supply +5.0V,-5.2V,-2.0V,AGND,-10.0V,+10.0V,
VBB(+3.0V),+15V(divided as +7.5V),-15V(divided as -7.5V),

TEST DESCRIPTION:

The DAC 7541 linearity is functionally tested by using the +10.0V, -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.5V, -7.5V, +0.00V, +1.30V and -1.40V as reference voltage, multiplexed through 7F as noninverting input. Data is written into 8A as inverting input until Q2 toggles its state. The ADC status is then verified by reading port 04H bit 0.

When the reference voltage is +10.0V, the DAC 7541 is initially programmed to -10.0V. Q2 is turned on, and the ADC status bit is equal to 0, incrementing the DAC 7541 output voltage until ADC status bit toggles its state.

When the reference voltages are -10.0V, AGND, -2.0V, -5.2V, +5.0V, +3.0V, +7.50V, -7.50V, DVM input, +1.30V, -1.40V the DAC 7541 is initially programmed to +10.0V. Q2 is turned off, and the ADC status bit is equal to 1, decrementing the DAC 7541 output voltage until the ADC status bit toggles its state.

TEST STEP INFORMATION:

Step	Reference voltage	Initial 7541 data voltage	Initial ADC status
1	+10.0V	0FFFH(-10.0V)	0
2	-10.0V	0000H(+10.0V)	1
3	AGND	0000H(+10.0V)	1
4	-2.0V	0000H(+10.0V)	1
5	-5.2V	0000H(+10.0V)	1
6	+5.0V	0000H(+10.0V)	1
7	VBB(+3.0V)	0000H(+10.0V)	1
8	+15V/2	0000H(+10.0V)	1
9	-15V/2	0000H(+10.0V)	1
10	DVM	0000H(+10.0V)	1
11	-ECL	0000H(+10.0V)	1
12	+TTL	0000H(+10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7541 Linearity Test
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = sll.lll
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 12

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 9.940, 10.235, 0.300, 2.350, 5.625, 4.820
2.700, 7.380, 7.980, 0.300, 1.000, 1.700

ll.lll should be 10.240, 9.935, 0.300, 1.750, 5.025, 5.420
3.300, 7.980, 7.380, 0.300, 1.600, 1.100

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 2

TITLE: DAC 7533 LINEARITY TEST

TARGET LOGIC: 6D,4B,12B,9B,9A,4A,5A,10A, 6F,7A,8A,Q2,8F,5E,6E,8B

TEST DESCRIPTION:

The DAC 7533 linearity is functionally tested by using the DAC 7541 as reference voltage. VAR A and VAR B are multiplexed through 6F as the noninverting input of 7A, and continues incrementing or decrementing VAR A or VAR B voltage by writing to port 08H or 0AH until the ADC output bit toggles its state.

When the DAC 7541 reference voltage is +10.0V, DAC 7533 is initially programmed to -10.0V. Q2 is turned off and the ADC status bit is equal to 1. When the DAC 7541 reference voltages are -9.980V, -5.0V, 0.00V and +5.0V, DAC 7533 is initialized to +10.0V and Q2 is turned on. The ADC status bit is equal to 0.

When VAR A and VAR B are being tested, each DAC 7533 has five voltage levels as follows: -9.980V, -5.0V, 0.00V, +5.00V and +10.00V.

TEST STEP INFORMATION:

Step	Reference voltage	Initial 7533 data voltage	Initial ADC status
1	-9.980V(7541)	0000H(VAR A +10.0V)	0
2	-5.0V(7541)	0000H(VAR A +10.0V)	0
3	-0.000V(7541)	0000H(VAR A +10.0V)	0
4	+5.0V(7541)	0000H(VAR A +10.0V)	0
5	+10.00V(7541)	0FFFH(VAR A -10.0V)	1
6	-9.980V(7541)	0000H(VAR B +10.0V)	0
7	-5.0V(7541)	0000H(VAR B +10.0V)	0
8	-0.000V(7541)	0000H(VAR B +10.0V)	0
9	+5.0V(7541)	0000H(VAR B +10.0V)	0
10	+10.00V(7541)	0FFFH(VAR B -10.0V)	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
DAC 7533 Linearity Test
Voltage Expected     = see.eee
Voltage Lower Limit  = suu.uuu
Voltage Upper Limit  = sll.lll
Actual Voltage Read  = saa.aaa
ADC Status Expected  = x
ADC Status Expected  = y
```

Where zz should be in the range of 1 through 10

s should be + or -

ee.eee should be in the range of 00.000 through 10.000

uu.uuu should be 10.220, 5.620, 0.500, 4.620, 9.740

ll.lll should be 9.740, 4.620, 0.500, 5.620, 10.240

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 3

TITLE: THRESHOLD/MUX. LOGIC TEST

TARGET LOGIC: 4D,5B,1A,1D,1B,1C,2A,2D 5F,7A,7E,5E,6E,8B,8A,8F and Q2.

TEST DESCRIPTION:

The threshold/mux's logic is functionally tested by using the TH0 through TH5 as reference voltages. These voltages are multiplexed through 5F as the noninverting input of 7A. The DAC 7541 is initially programmed to +10.0V and decrements the DAC 7541 output voltage until the ADC output status bit toggles its state.

Reference voltages for -ECL, -TTL, -VAR A and -VAR B are present for each threshold channel. The -ECL is +1.300V, -TTL is -1.400V, -VAR A is +5.0V and -VAR B is -5.0V.

Testing occurs for threshold channels TH0 through TH5. The original ADC status bit should be 1 when the DAC 7541 is initialized to +10.0V.

TEST STEP INFORMATION:

Step	Logic	TH channel	Initialized 7541 voltage	Initial ADC status
1	-ECL	0	+10.0V	1
2	-ECL	1	+10.0V	1
3	-ECL	2	+10.0V	1
4	-ECL	3	+10.0V	1
5	-ECL	4	+10.0V	1
6	-ECL	5	+10.0V	1
7	-VAR A	0	+10.0V	1
8	-VAR A	1	+10.0V	1
9	-VAR A	2	+10.0V	1
10	-VAR A	3	+10.0V	1
11	-VAR A	4	+10.0V	1
12	-VAR A	5	+10.0V	1
13	-TTL	0	+10.0V	1
14	-TTL	1	+10.0V	1
15	-TTL	2	+10.0V	1
16	-TTL	3	+10.0V	1
17	-TTL	4	+10.0V	1
18	-TTL	5	+10.0V	1
19	-VAR B	0	+10.0V	1
20	-VAR B	1	+10.0V	1
21	-VAR B	2	+10.0V	1
22	-VAR B	3	+10.0V	1
24	-VAR B	4	+10.0V	1
24	-VAR B	5	+10.0V	1

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Threshold/Mux. Logic Test
?????? Threshold Testing
TH Channel n Testing
Voltage Expected     = see.eee
Voltage Lower Limit = suu.uuu
Voltage Upper Limit = sll.lll
Actual Voltage Read = saa.aaa
ADC Status Expected = x
ADC Status Expected = y
```

Where zz should be in the range of 1 through 24

?????? should be -ECL, -VAR A, -TTL, -VAR B

n should be in the range of 0 through 5

s should be + or -

ee.eee should be 1.300, 5.000, 1.400, 5.000

uu.uuu should be 0.980, 4.800, 1.720, 5.440

ll.lll should be 1.620, 5.400, 1.080, 4.800

aa.aaa should be in the range of 00.000 through 10.000

x,y should be 0 or 1

Threshold Diagnostic Subtest 4

TITLE: SERIAL I/O PORT #1 TEST

TARGET LOGIC: 12D, 14A, 13A, 8E

TEST DESCRIPTION:

Serial I/O port #1 is functionally tested by using USART #1 as a transmitter and receiver to transmit an 8-bit data pattern and receive the transmitted bytes through the wrap back RS232 connector within a specified time window(95% through 105%).

The RS232 wrap back connector is configurated as follows:

CTS (clear to send) short to RTS (request to send),
DSR (data set ready) short to DTR (data terminal ready),
RxD (received data) short to TxD (transmitted data).
that is to say,
pin 2 short to pin 3,
pin 4 short to pin 5,
pin 6 short to pin 20.

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:
---

1. If an error of transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Transmitter Buffer Not Empty
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where: zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error of no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
No Character Received
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where: zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error of character received early occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Early
Testing Baud Rate        = bbbb
Minimum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where: zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 3554, 2596, 1282, 640, 312, 236, 158, 80, 40

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error of character received late occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Character Received Late
Testing Baud Rate        = bbbb
Maximum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where: zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 4606, 3402, 1718, 834, 408, 310, 198, 106, 56

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error of bad character occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 1 Test
Bad character Received
Testing Baud Rate        = bbbb
Received Data            = rrH
Transmitted Data         = ttH
```

where: zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

TEST 109 - CTS

1. Using last selected baud rate from Test 108(9600), write a 13H to the 8251 port 42 to enable TX and RX and DTR but not RTS which is tied to CTS.

2. Write to port 40 (data port).

3. Read port 42; continue until timeout if no character received.

4. If character received(bit 1 = 1), an error occurred.

ERROR MESSAGE:

```
*  Test FAILED ---Test Step 109
Serial I/O Port 1 Test
CTS force inactive
```

TEST 110

1. Output 10H to port 42 of 8251. (TX, RX, RTS, DTR off)

2. Read port 42. Error occurs if bit 7 = 1.

ERROR MESSAGE:

```
*  Test FAILED ---Test Step 110
Serial I/O Port 1 Test
DSR force inactive
```

Threshold Diagnostic Subtest 5

TITLE: SERIAL I/O PORT #2 TEST

TARGET LOGIC: 12E,15B,13B,8E,8D

TEST DESCRIPTION:

Serial I/O port #2 is functionally tested by using USART #2 as a transmitter and receiver to transmit an 8-bit data pattern and receive the transmitted bytes through the wrap back RS232 connector within a specified time window(95% through 105%).

The RS232 wrap back connector is configurated as follows:

CTS(clear to send) short to RTS(request to send),
DSR(data set ready) short to DTR(data terminal ready),
RxD(received data) short to TxD(transmitted data).
that is to say,
pin 2 short to pin 3,
pin 4 short to pin 5,
pin 6 short to pin 20.

The following patterns are transmitted:

0AAH, 055H, 0CCH, 033H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

The following baud rates are tested:

110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

TEST STEP INFORMATION:

Test Step	Baud Rate	Data Pattern
1 through 12	110	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
13 through 24	150	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
25 through 36	300	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
37 through 48	600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
49 through 60	1200	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
61 through 72	1800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
73 through 84	2400	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
85 through 96	4800	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H
97 through 108	9600	0AAH,55H,0CCH,33H,01H,02H,04H,08H,10H,20H,40H,80H

ERROR MESSAGE:
---

1. If an error of transmitter buffer not empty occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Transmitter Buffer Not Empty
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

2. If an error of no character received occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
No Character Received
Testing Baud Rate     = bbbb
Status Byte Read      = rrH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

3. If an error of character received early occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Early
Testing Baud Rate        = bbbb
Minimum Expected Count   = eeeee
Actual Software Count    = ccccc
Received Data            = rrH
Transmitted Data         = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 3554, 2596, 1282, 640, 312, 236, 158, 80, 40

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

4. If an error of character received late occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Character Received Late
Testing Baud Rate       = bbbb
Maximum Expected Count  = eeeee
Actual Software Count   = ccccc
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

eeeee should be 4606, 3402, 1718, 834, 408, 310, 198, 106, 56

ccccc should be in the range of 00000 through 65535

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

5. If an error of bad character occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Serial I/O Port 2 Test
Bad character Received
Testing Baud Rate       = bbbb
Received Data           = rrH
Transmitted Data        = ttH
```

where zz should be in the range of 1 through 108

bbbb should be 110, 150, 300, 600, 1200, 1800, 2400, 4800, 9600

rr should be in the range of 00 through FF

tt should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

TEST 109 - CTS

1. Using last selected baud rate from Test 108(9600), write a 13H to the 8251 port 62 to enable TX and RX and DTR but not RTS which is tied to CTS.

2. Write to port 60 (data port).

3. Read port 62; continue until timeout if no character received.

4. If character received(bit 1 = 1), an error occurred.

ERROR MESSAGE:

```
*  Test FAILED ---Test Step 109
Serial I/O Port 2 Test
CTS force inactive
```

TEST 110

1. Output 10H to port 62 of 8251. (TX, RX, RTS, DTR off)

2. Read port 62. Error occurs if bit 7 = 1.

ERROR MESSAGE:

```
*  Test FAILED ---Test Step 110
Serial I/O Port 2 Test
DSR force inactive
```

Threshold Diagnostic Subtest 6

TITLE: TIMER 8253 COUNTER 0 TEST

TARGET LOGIC: 13F,8D,8E and GATE/ logic from control board

TEST DESCRIPTION:

The timer 8253 counter 0 is functionally tested by programming counter 0 to mode 1(programmable one shot mode) and triggering GATE0 from control board GATE/ logic. The counter 0 is then verified by reading the latched count after GATE0 has been triggered.

The terminal count patterns tested are :

8000H,4000H,2000H,1000H,0800H,0400H,0200H,0100H,
0080H,0040H,0020H,0010H,0008H,0004H,0002H,0001H.

There are two methods for testing counter 0 in mode 1:

a. After loading terminal count,trigger GATE0 from low to high.

b. After loading terminal count,trigger GATE0 from low to high two times, the second trigger should cause a counter reset to the terminal count value.

TEST STEP INFORMATION:

Test step	Terminal count programmed	Rising edge trigger pulses
1	8000H	1
2	4000H	1
3	2000H	1
4	1000H	1
5	0800H	1
6	0400H	1
7	0200H	1
8	0100H	1
9	0080H	1
10	0040H	1
11	0020H	1
12	0010H	1
13	0008H	1
14	0004H	1
15	0002H	1
16	0001H	1
17	8000H	2
18	4000H	2
19	2000H	2
20	1000H	2
21	0800H	2

22	0400H	2
23	0200H	2
24	0100H	2
25	0080H	2
26	0040H	2
27	0020H	2
28	0010H	2
29	0008H	2
30	0004H	2
31	0002H	2
32	0001H	2

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED--Test Step zz
Timer 8253 Counter 0 Test
Programmable One Shot Mode
Testing Terminal count = ccccH
Expected High Count    = eeeeH
Expected Low Count     = 1111H
Actually Read Count    = rrrrH
```

where: zz should be in the range of 1 through 32

cccc should be 8000, 4000, 2000, 1000, 0800, 0400, 0200, 0100,
0080, 0040, 0020, 0010, 0008, 0004, 0002, 0001.

eeee should be 7EC8, 3EC8, 1EC8, 0EC8, 06C8, 02C8, 00C8, FFC8,
FF48, FF08, FEE8, FED8, FED0, FECC, FECA, FEC9.
or 7FDD, 3FDD, 1FDD, 0FDD, 07DD, 03DD, 01DD, 00DD,
005D, 001D, FFFD, FFED, FFE5, FFE1, FFDF, FFDE.

1111 should be 7EB8, 3EB8, 1EB8, 0EB8, 06B8, 02B8, 00B8, FFB8,
FF38, FEF8, FED8, FEC8, FEC0, FEBC, FEBA, FEB9.
or 7FCD, 3FCD, 1FCD, 0FCD, 07CD, 03CD, 01CD, 00CD,
004D, 000D, FFED, FFDD, FFD5, FFD1, FFCF, FFCE.

rrrr should be in the range of 0000 through FFFF

Threshold Diagnostic Subtest 7

TITLE: GPIB INTERNAL CONTROL LINES TEST

TARGET LOGIC: 15F,17F,16F,16D

TEST DESCRIPTION:

The GPIB internal control lines are functionally tested by writing the local control bit true. The control bit is then verified by reading back the control status bit.

There are 5 control lines being tested:

'catn', 'cifc', 'cren', 'srq', 'end'

If the 'cacs' line is not true, then lines for 'catn', 'cifc', 'cren' and 'srq' are also not true.

TEST STEP INFORMATION:

Test step	Control bit
1	'catn'
2	'cifc'
3	'cren'
4	'srq'
5	'end'

ERROR MESSAGE:

If an error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Control Lines
Status Port Address 01H
Bit 7 through Bit 3 is :
atn  srq  ifc  ren  eoi
"????" and "cacs" Logic Test
"????" Status Expected = ssssssssB
"????" Status Read     = rrrrrrrrB
Falling Time Constant  = ttttt
"????" Status Expected = eeeeeeeeB
"????" Status Read     = vvvvvvvvB
Rising Time Constant   = ccccc
```

where zz should be in the range of 1 to 5

???? should be catn, cifc, cren, srq, end.

ssssssss should be 10000000, 00100000, 00010000, 01000000, 00001000.

rrrrrrrr should be 00000000 through 11111111.

ttttt should be in the range of 00000 through 65535.

eeeeeeee should be 00000000.

vvvvvvvv should be 00000000 through 11111111.

ccccc should be in the range of 00000 through 65535.

NOTE : Falling and rising time constant are for diagnostic reference only.

Threshold Diagnostic Subtest 8

TITLE: GPIB INTERNAL MPU INTERRUPT TEST

TARGET LOGIC: 15F,17F,16F,15D,17D,21D,17B, 18B,19B,20A,20B,21A,19A,20A,16B,21F

TEST DESCRIPTION:

The GPIB internal MPU interrupt is functionally tested by writing local control control bit true and local command bits true. The interrupt status bit is then verified by reading the interrupt status.

There are four MPU interrupt logic conditions being tested: 'tint', 'srint', 'nrint' and 'cint'. (The 'lint' is associated with the GPIB external handshake function which is not tested.)

The 'INTR1/'test is associated with 'tint', 'srint', 'nrint' and 'cint'interrupt logic conditions.

TEST STEP INFORMATION:

Test step	MPU interrupt logic
1	'tint' and 'INTR1/'
2	'srint' and 'INTR1/'
3	'nrint' and 'INTR1/'
4	'cint' and 'INTR1/'

ERROR MESSAGE:

1. If an INTR1/ error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
GPIB INTR1/ Not Generated
```

where zz should be in the range of 1 through 4

????? should be tint, srint, nrint, cint.

2. If an interrupt status error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
```

```
GPIB Internal Interrupt Line
gint/ lint tint cint nrint srint get/ nins/
"?????" Interrupt Line Test
Status 1 Expected   = aaaaaaaaB
Status 1 Read       = bbbbbbbbB
Status 2 Expected   = cccccccB
Status 2 Read       = ddddddddB
Status 3 Expected   = eeeeeeeeB
Status 3 Read       = ffffffffB
Status 4 Expected   = gggggggB
Status 4 Read       = hhhhhhhhB
```

where zz should be 1 through 4

?????? should be tint, srint, nrint, cint

aaaaaaaa should be 10000010.

cccccccc should be 11111111, 10000010.

eeeeeeee should be 00100010, 00000110, 00001010, 00010010.

gggggggg should be 10000010.

bbbbbbbb should be in the range of 00000000 through 11111111

dddddddd should be in the range of 00000000 through 11111111

ffffffff should be in the range of 00000000 through 11111111

hhhhhhhh should be in the range of 00000000 through 11111111

Threshold Diagnostic Subtest 9

TITLE: GPIB INTERNAL DATA REGISTER TEST

TARGET LOGIC: 18E,19E,18D,19D,20E,21E,20F

TEST DESCRIPTION:

The GPIB internal data register is functionally tested by writing a data byte pattern through data register or parallel poll response register. The data byte is then verified by reading the data from the input register.

There are 12 data patterns tb be tested :

0AAH, 55H, 0CCH, 33H, 01H, 02H, 04H, 08H, 10H, 20H, 40H, 80H.

There are two output registers to be tested :

1. Data output register (18E)
2. parallel poll response register (19E).

TEST STEP INFORMATION:

Test step	Register under test	Data pattern
1	data output register	0AAH
2	data output register	55H
3	data output register	0CCH
4	data output register	33H
5	data output register	01H
6	data output register	02H
7	data output register	04H
8	data output register	08H
9	data output register	10H
10	data output register	20H
11	data output register	40H
12	data output register	80H
13	parallel poll response	0AAH
14	parallel poll response	55H
15	parallel poll response	0CCH
16	parallel poll response	33H
17	parallel poll response	01H
18	parallel poll response	02H
19	parallel poll response	04H
20	parallel poll response	08H
21	parallel poll response	10H
22	parallel poll response	20H
23	parallel poll response	40H
24	parallel poll response	80H

ERROR MESSAGE:
---

1. If a data output register error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Data Out Register Testing
Data Register Expected = eeH
Data Register Read     = rrH
```

where: zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

2. If a parallel poll response register error occurs, the following message is displayed:

```
* Test FAILED -- Test Step zz
GPIB Data Register Test
Parallel Poll Response
Data Register Expected = eeH
Data Register Read     = rrH
```

where: zz should be in the range of 1 through 24

ee should be AA, 55, CC, 33, 01, 02, 04, 08, 10, 20, 40, 80

rr should be 00 through FF

STORAGE CONTROLLER BOARD DIAGNOSTIC TEST

DIAGNOSTIC OVERVIEW

This section describes the subtests executed on the K450B Storage Controller Board, how error reporting is done, and the concept behind each subtest program.

It should be noted that while the K450B Storage Controller Board contains provisions for a UART, this Diagnostic does not test the UART components.

There are 6 subtests written for the Storage Controller Board. each of these subtests are described individually on the following pages: Loop On Error, Error Count and Pass Count update are incorporated into each subtest. Details about interfacing to the diagnostic monitor can be found in the description of the Diagnostic Monitor .

All error messages will be preceded by a "*" while information messages will use the ">" prefix.

Early exit from each subtest is accomplished by pressing the "STOP" key.

Assumtions: This series of tests assumes that two other boards in the K450B are installed and functional. An operational MPU board as well as a fully functional Keyboard/Display board must be installed.

SUBTEST CATEGORIES

1. 6116 Data Integrity
2. 6116 Address Integrity
3. FDC Seek
4. Fixed FDC Write/Read
5. Random FDC Write/Read
6. FDC/DMA Address Logic

ERROR COUNT CATEGORIES

1. Subtest 1
2. Subtest 2
3. Subtest 3
4. Subtest 4
5. Subtest 5
6. Subtest 6
7. Seek Command Error Count
8. Recalibrate Command Error Count
9. Write Command Error Count
10. Read Command Error Count
11. Drive A Error Count
12. Drive B Error Count
13. Side 0 Error Count

14. Side 1 Error Count
15. Soft Error Count
16. Hard Error Count
17. Not Ready Error Count
18. Head Address Error Count
19. Ready Changed State Error Count
20. Missing Address mark Error Count
21. Write protected Error Count
22. Sector not found Error Count
23. FDC over run Error Count
24. FDC int timout Error Count
25. Access beyond end of Track Error Count
26. Missing Data Address mark Error Count
27. Bad Track Error Count
28. Wrong cylinder Error Count
29. Data Error CRC Error Count
30. Control mark : deleted Data Encountered Error Count
31. Unformatted Diskette Error Count
32. Diagnostic program Error Count

Storage System Controller Subtest 1

TITLE: 6116 DATA INTEGRITY TEST

PURPOSE:

This subtest confirms the ability of the DMA hardware to sucessfully write data into the 4k area of 6116 RAM. The integrity of the RAM is checked by running several patterns through the Memory.

The RAM is not directly Addressable; all access is through the DMA controller.

TARGET HARDWARE: 5D,5E,5F,5H,6E,6F,7E

TEST DESCRIPTION:

It is not possible to Write directly to the 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs, an Error message is printed.

The following is a summary of the Data written to the RAM during each test step:

TEST STEP INFORMATION:

Test step	Value written
1	0
2	AAH
3	55H
4	CCH
5	33H
6	01H
7	02H
8	04H
9	08H
10	10H
11	20H
12	40H
13	80H

ERROR MESSAGE:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step    xx
RAM Data Error
Data Expected  = aaH
Data Read      = bbH
Address Count  = ccccH
DMA Status     = ddH
```

where xx = test step number
aa = 00 - FF
bb = 00 - FF
cccc = 0000 - 0FFF
dd = 00 - FF

Storage System Controller Subtest 2

TITLE: 6116 ADDRESS INTEGRITY TEST

PURPOSE:

The purpose of this test is to selectively Write 1 byte of Data into the 4K of RAM on the storage controller board which has been preset to zero. Verification is then made to confirm that the only place the RAM is written to is the indicated Address.

TARGET HARDWARE: 5D,5E,5F,5H,6E,6F,7E

TEST DESCRIPTION:

It is not possible to Write directly to these 6116 RAMs. All access is through the DMA controller. Data is written to the DMA controller and the controller passes it on to the RAM. Reading is accomplished through the same type of cycle. Various Data patterns are written to the RAM then Read back. If a miscompare occurs an error message is printed.

All of the RAM in this test is preset to zero then the indicated Address is written with the value 0aah. All of RAM is then Read to verify the written Data. If a mis-compare is detected, then an error message is displayed.

TEST STEP INFORMATION:

Test step	Indicated Address
1	0000H
2	0001H
3	0002H
4	0004H
5	0008H
6	0010H
7	0020H
8	0040H
9	0080H
10	0100H
11	0200H
12	0400H

ERROR MESSAGES:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step     xx
All Storage Controller RAM Set to Zero.
Unique Testing Address    = ttttH
Data at Testing Address   = ddH
Checking Data at Address  = aaaaH
Data Expected             = eeH
Data Read                 = rrH
```

where:
```
   xx = test step number
 tttt = 0000 - 0FFF
   dd = 00 - FF
 aaaa = 0000 - 0FFF
   ee = 00 - FF
   rr = 00 - FF
```

Storage System Controller Subtest 3

TITLE: FDC SEEK TEST

PURPOSE:

The purpose of this subtest is to verify operation of the seek process on one or both Disk Drives.

TARGET HARDWARE: 2H,3D,3E,3F,3H,4C,4D,4E,4F,7D,7F

TEST DESCRIPTION:

The FDC is commanded to perform seeks to the given Track as outlined below. Tracks are accessed from Track 0 to 39, and 39 to 0. Finally, an alternating pattern of seeks spiraling, from outermost to innermost Tracks is performed.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed.

This operation is repeated for all selected Drive and Side options.

TEST STEP INFORMATION:

Test step number	Drive/Side	Disk action
1 - 40	A / 0	seek 0-39
41- 80	A / 0	seek 39-0
81- 120	A / 0	spiral inward
121-160	A / 1	seek 0-39
161-200	A / 1	seek 39-0
201-240	A / 1	spiral inward
241-280	B / 0	seek 0-39
281-320	B / 0	seek 39-0
321-360	B / 0	spiral inward
361-400	B / 1	seek 0-39
401-440	B / 1	seek 39-0
441-480	B / 1	spiral inward

ERROR MESSAGES:

If any errors are detected this subtest will display the error messages found in appendix 1.

Storage System Controller Subtest 4

TITLE: FDC WRITE/READ TEST

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's ability to Write and Read back information on all Tracks of the Disk Drive.

TARGET HARDWARE: 2H,3D,3E,3F,3H,4C,4D,4E,4F,7D,7F
2A,2B,2C,3A,3B

TEST DESCRIPTION:

The FDC is Commanded to Write Data to all Tracks on a given Disk surface on a sector-by-sector basis. If the Track written to is either Track 0 or Track 39, then all sectors are written to. On other Tracks, only sector 1 is actually tested. The Data is then Read back and compared to the pattern written. If a miscompare occurs, an error message is displayed.

As these operations are sent to the FDC controller, the status of the controller is monitored and if an error is detected an error message is displayed. This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test step number	Drive/Side	Disk action
1 - 40	a/0	Write/Read/compare
41 - 80	a/1	Write/Read/compare
81 - 120	b/0	Write/Read/compare
121 - 160	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step    xxx
Sector Compare Error
Track Number    = 0aa
Sector Number   = 00b
Address Count   = 0cccH
Data Expected   = ddH
Data Read       = eeH
```

where: xxx = test step number
aa = 0 - 39
bb = 0 - 8
ccc = 000 - FFF
dd = 00 - FF
ee = 00 - FF

Note : also see appendix 1.

Storage System Controller Subtest 5

TITLE: RANDOM FDC WRITE/READ

PURPOSE:

The purpose of this subtest is to verify the Storage Controller Board's ability to Write and Read back information on 63 random locations of the Disk Drive.

TARGET HARDWARE: 2H,3D,3E,3F,3H,4C,4D,4E,4F,7D,7F
2A,2B,2C,3A,3B

TEST DESCRIPTION:

This subtest generates random Data and performs 63 random Read/Write cycles. As Data is written it is then Read back and compared. If a miscompare of Data occurs, it is reported via an error message. As these operations are sent to the FDC controller, the status of the controller is monitored. If an error is detected, an error message is displayed.

This operation is repeated for all selected Drive and Side options selected.

TEST STEP INFORMATION:

Test step number	Drive/Side	Disk action
1- 64	a/0	Write/Read/compare
65- 126	a/1	Write/Read/compare
127- 190	b/0	Write/Read/compare
191- 254	b/1	Write/Read/compare

ERROR MESSAGES:

If any errors are detected this subtest will display the following message:

```
* Test FAILED--Test Step    xxx
Sector Compare Error
Track Number    = 0aa
Sector Number   = 00b
Address Count   = 0cccH
Data Expected   = ddH
Data Read       = eeH
```

where: xx = test step number
aa = 0 - 39
bb = 0 - 8
ccc = 000 - FFF
dd = 00 - FF
ee = 00 - FF

Note : also see appendix 1.

Storage System Controller Subtest 6

TITLE: FDC/DMA ADDRESS LOGIC

PURPOSE:

The purpose of this subtest is to verify integrity of the Address counters between the DMA controller and the floppy Disk controller.

TARGET HARDWARE: 2H,3D,3E,3F,3H,4C,4D,4E,4F,7D,7F
2A,2B,2C,3A,3B

TEST DESCRIPTION:

The Data pattern, 0aah, is written to the indicated Addresses on the Storage Controller Board. The entire RAM contents are written to Track 22 on the first available Drive. The RAM is zeroed out then a Read sector Command is issued. The RAM is then analyzed to determine if the DMA controller has placed Data in the original locations.

As these operations are sent to the FDC controller, the status of the controller is monitored. If an error is detected, an error message is displayed.

This operation is repeated for all selected Drive and Side options selected

TEST STEP INFORMATION:

Test step	Address range
1	0000H - 01FFH
2	0001H - 0200H
3	0002H - 0201H
4	0004H - 0203H
5	0008H - 0207H
6	0010H - 020FH
7	0020H - 021FH
8	0040H - 023FH
9	0080H - 027FH
10	0100H - 02FFH
11	0200H - 03FFH
12	0400H - 05FFH
13	0800H - 09FFH
14	1000H - 11FFH

ERROR MESSAGES:

If any errors are detected this subtest will display the following message

```
* Test FAILED--Test Step    xx
All Storage Controller RAM Set to Zero.
Unique Testing Address Range  = llllH to hhhhH
Data in Address Range         = ddH
Checking Data at Address      = aaaaH
Data Expected                 = eeH
Data Read                     = rrH
```

where xx = test step number
llll = 0000 - 0FFF
hhhh = 0000 - 0FFF
dd = AAH
aaaa = 0000 - 0FFF
ee = 00 - FF
rr = 00 - FF

Note : Also see Appendix 1.

Error messages common to all Disk activity:

Subtests 3-6 all use a common routine for Disk operations which can generate the following error message.

```
* Test FAILED--Test Step    aa
Retrying Disk Command
Retry Count = b
Disk Command: c
Drive  = d
Head   = e
Track  = 0ff
Sector = g
msg
```

where: aa = test step number
b = number of times Disk Command has been attempted
c = seek Command,
Read id Command,
recalibrate Command,
Write Track Command,
Write sector Command,
Read Track Command,
Read sector Command.
d = A or B
e = 0 or 1
ff = 0 to 39
g = 1 to 8

msg = Disk Drive Not Ready.
Head Address Error.
During Command, Ready Changed State.
Missing Address Mark.
Write Protected.
Sector Not Found.
FDC Over-run Error.
Data Error (CRC).
FDC Interrupt Timeout Error.
Access Beyond End of Track.
Missing Data Address Mark.
Bad Track.
Wrong Cylinder.
Data Error (crc).
Control Mark: Deleted Data Encountered.
Not a Formatted Disk.

CALIBRATION LAB

Chapter 6

OPTIONS INSTALLATION

GENERAL

This chapter describes procedures for installing the K450B Data Board Input Expansion Option and K450B Dual Disk Storage System (DSS) Option equipment at the user's site. This optional equipment is provided in kit form for users who desire to expand the operating capabilities of their existing equipment. Once installed, the K450B automatically recognizes the new hardware configuration when powered up. The Configuration Screen indicates which optional features are available for system operation. The following kits are available:

- o K450B 32-channel Number 2 Data Board (provides input expansion from 32 channels to 64 channels), Product No. A14566
- o K450B 16-channel Number 3 Data Board(provides input expansion from 64 channels to 80- channels), Product No. A14567
- o Dual-Disk Storage System Product No. A14548

Each kit contains installation instructions for the equipment option. The internal wiring harness assemblies that interface with optional printed circuit board edge connectors are installed in the K450B chassis by the factory to facilitate the addition of options by the user. These harness assemblies are located at the upper right-hand side of the card cage. Individual cables contained within the harness are labeled for identification. The entire bundle of cables is exposed when the top cover is removed from the K450B chassis.

Each of the K450B Data Board kits contains a Data printed circuit board assembly and a set of input cables, probes and grabbers which provide 32 or 16 additional inputs to the K450B. A separate kit is required for Input Sections C/D (32 inputs) and Section E (16 inputs).

The DDS Option Kit contains the dual-disk drive assembly mounting hardware and attached interface cable assemblies that must be installed by the user. The associated diagrams and wiring details are described in the installation procedure. The DSS functional description and operation are described in the K450B User's Manual Publication Number 0121-0460-10.

Card Cage Arrangement

The board ejector tabs on each printed circuit board are numbered to correspond to the assigned slot location in the card cage. For the most part, the assigned board is dedicated to reside in its assigned slot location except where specified below for the Data Boards. The installed boards are secured in the card cage by a slotted retainer bar, which is fastened to the top of the card cage by two screws.

Data Board Input Configurations

Three Data Boards reside in slot locations A2, A3 and A4. Two Data Boards at slot locations A3 and A4 contain circuitry for 32 channels each at Input Sections A/B and C/D. These two boards are also interchangeable. The Data Board for slot location A2 contains circuitry for 16 channels at Input section E.

The K450B unit configured for 32 Inputs (Sections A & B) use one Data Board installed in slot location A4. This is the minimum input configuration which can be expanded by adding one or two additional Data Boards.

Units configured for 64 Inputs (Sections A,B,C, and D) use an additional Data Board installed in slot location A3 to enable Inputs at Sections C and D. The expansion for Input Sections C and D requires jumper connections on the Clock Board to be repositioned to convert the BR and BS Sample Clocks into Latch Clocks as described in the installation procedure.

Units configured for 80 Inputs (Sections A,B,C,D and E) use an additional Data Board installed in slot location A4 to enable Input at Section E.

INSTALLATION OF K450B INPUT EXPANSION OPTION

General

The Data Board and probes supplied for the Input Expansion Option provide 32 additional channels for Input Sections C and D (Product No. A14566) and 16 additional channels for Input Section E (Product No. A1456). A separate kit is required to install the option for respective Input Sections. All hardware items required to install and operate this option at the user's site are contained in the kit. The components provided for each kit are described in Table 6-1.

Table 6-1 Expansion Option Components

QUANTITY		PART NUMBER	DESCRIPTION
32-channel (#A14566)	16-channel (#A14567)		
1		0121-0415-10	Data Board, Printed Circuit Board Assembly (32 channels)
	1	0121-0415-20	Data Board, Printed Circuit Board Assembly (16 channels)
4	2	0117-0294-30/-50	Input Cable Set
88	44	7100-0116-10	Grabbers
8	4	0117-0099-10	Probe Subassembly
1	1	0121-0492-10	K450B Input Expansion Option Instruction Sheet
4	2	0117-0740-10	Label, Active Probe Pod
2	1	0117-0208-01	Label, Output Cable

Unpacking and Inspection

All equipment was thoroughly inspected and checked out at the factory prior to packing for shipment. After removing the equipment from its shipping container, inspect for damage that might have occurred during shipping. Refer to the shipping papers to verify all items were received.

If equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Gould Inc., Design and Test Systems Division Customer Service department at once. Gould Inc., DTD will arrange for replacement of the equipment without waiting for settlement of the claim against the carrier.

Installation Procedure

Prior to beginning the option installation, position the carrying handle of the K450B to the front of the machine so that the chassis rests flat on the work surface.

****

WARNING

Disconnect the 115/230 Vac source to the K450B prior to installing any options. Otherwise, a shock hazard exists. Also, high voltage is present on the CRT and Data Display Board.

****

The following steps outline the procedure necessary to install the Number 2 Data Board for Input Sections C and D, and the Number 3 Data Board for Input Section E.

1. Remove the six Phillips-head screws that secure the top cover and DSS to the chassis, and carefully lift cover from the unit. Position top cover to side of chassis.

2. Remove the two screws that secure the card retainer bar to the top of at the card cage and lift it from the chassis. The card cage arrangement is shown in Figure 6-1.

3. Carefully locate the cable harness from board sockets at card cage locations A3, A4 and A5; note which sockets are associated with each cable.

4. Position the Data Board in card cage with the solder side toward the power supply of the unit. Carefully insert the Data Board into the designated card slot, A2 for Section C and D Inputs or A3 for Section E Inputs (refer to Figure 6-1). Ensure the Data Board is seated firmly in the mother board sockets.

5. If the Input Section C and D Data Board is being installed, remove the Clock Board from the card cage to change the jumper connections.

   Rearranging the jumper connections enables the Input Section C clock inputs and routes the BR and BS clocks into the user specified Latch Clock Equation. The K450B software will not recognize clock inputs at Section C unless these jumper connections are completed.

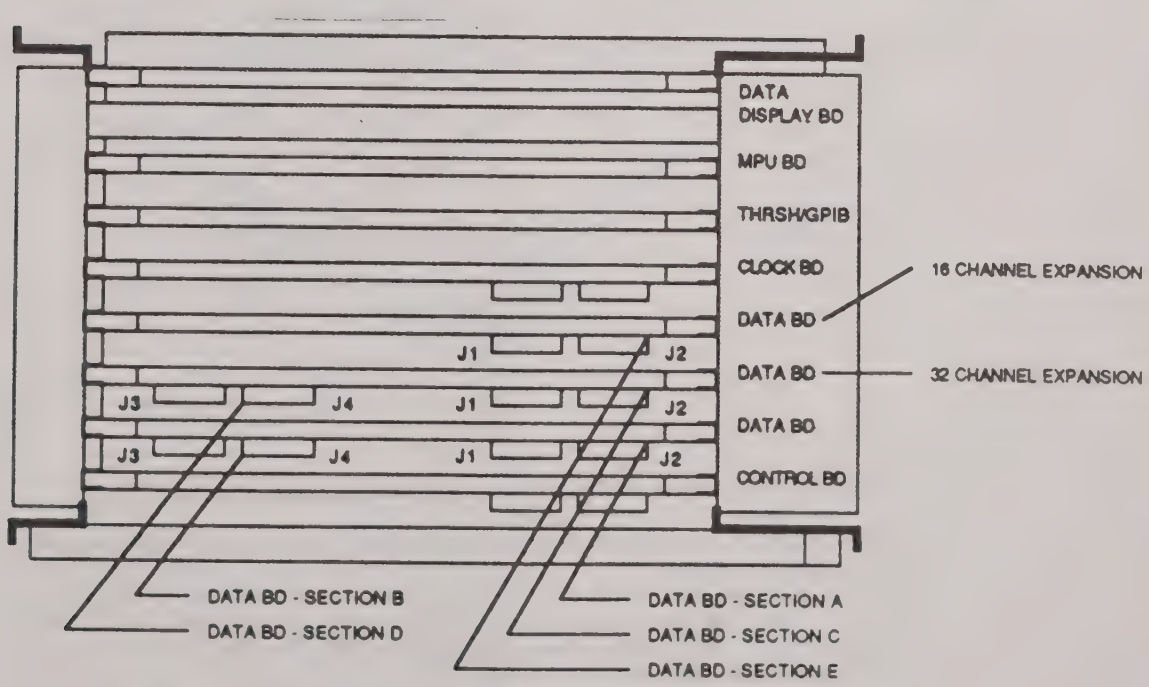


Figure 6-1. K450B Card Cage Arrangement, Top View

The eight jumpers are positioned at board location column 3, row K. These jumpers are to be relocated to pins from the common/lower row to pins at the common/upper row, to provide the following connection points:

T1-T2, T4-T5, T7-T8, T10-T11

T13-T14, T16-T17, T19-T20, T22-T23

6. Reinstall Clock Board in card cage after jumper connections are completed. Replace the card cage retainer bar and secure with the two screws.

7. Locate the unattached ribbon cables CLO, CHI, DLO and DHI (for Section C/D Data Board #2). See Figure 6-2. Install the CHI ribbon cable connector on J1. The dark-brown wire braid on the connector is located to the front of the machine.

NOTE: **If J1 is installed backwards, the equipment will not become damaged. The data at D0 will be displayed on channel D7. Reversing the connector corrects this condition.**

Install the CLO ribbon cable connector on J2 near the rear end of the machine. Install the DHI and DLO cables at connectors J3 and J4 respectively. Install the EHI and ELO ribbon cables to connectors J1 and J2 on Data Board #3.

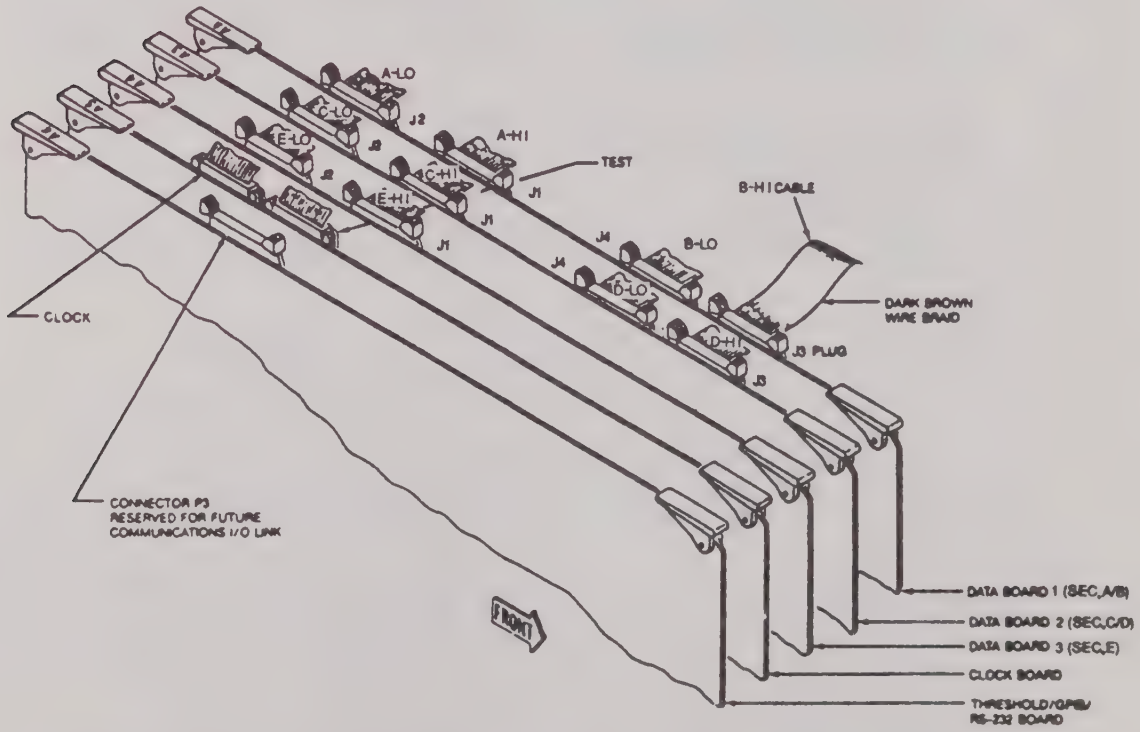


Figure 6-2. K450B Ribbon Cable Connections at Card Cage

8. Replace the harness connectors removed in Step 3. Ensure each harness is connected to its socket. See Figure 6-2.

9. Ensure the harness cables are properly positioned and do not interfere with reinstallation of the top cover. Reinstall the top cover and disk drive assembly.

10. Reinstall the six retaining screws to secure top cover.

11. Reconnect the 115/230 Vac source to the K450B. Operation of the K450B with 64 or 80

INSTALLATION OF DUAL-DISK STORAGE SYSTEM OPTION

General

The Dual-Disk Storage System Option Product # A14548, provides two 5 1/4 floppy disk drives with 312K bytes of storage per disk. This option provides the convenience of two floppy disk drives for storing set up parameters, trace information and data for later retrieval, and to load and execute the disk-based diagnostic routines. All hardware items required to install and operate the Dual-Disk Storage System (DSS) option at the user's site are shipped in packaged units. External cables for power and signal interface are included for connecting all components in the system. Components supplied for the DSS Option are described in Table 6-2.

Table 6-2. DSS Option Components

QUANTITY	PART NUMBER	DESCRIPTION
1	0114-0468-40	DSS Option Assembly (Includes interface cables for signal I/O and power.)
1	0121-0727-10	K450B DSS Option Instruction Sheet

Unpacking and Inspection

All equipment was thoroughly inspected and checked out at the factory prior to packaging for shipment. After removing the equipment from its container inspect for scratches, dents or other damage that might have occurred during shipping. Refer to the shipping papers to verify that all items were received.

If equipment received from the carrier is incomplete or damaged, do not install the equipment. File a claim with the shipping firm immediately, and notify Gould Inc., Design and Test Systems Division Customer Service department at once. Gould Inc., DTD will arrange for replacement of the equipment without waiting for settlement of the claim against the carrier.

Installation Procedure

Prior to beginning the option installation, position the carrying handle of the K450B to the front of the machine so that the chassis rests flat on the work surface.

****

WARNING

Disconnect the 115/230 Vac source to the K450B prior to installing any options. Otherwise, a shock hazard exists. Also, high voltage is present on the CRT and Display Board.

****

The following steps outline the procedure necessary to install the DSS option on the K450B chassis.

1. Remove the six Phillips-head screws that secure the top cover and single disk drive to the K450B chassis,. Disconnect the disk drive I/O cable and power harness and carefully lift the cover from the unit.

NOTE: It may be necessary to remove the card cage retainer bar and raise the Data Display Board approximately 2 inches in the card cage to gain access to the P4 connector shown in Figure 6-3.

2. Position the Dual-Disk DSS assembly on the K450B chassis and locate the I/O ribbon cable which extends through the access slot in the base of the DSS assembly. Connect the system I/O cable to P4 on Data Display Board.

3. Locate the DSS power harness connector and cable which extends through the access slot in base of DSS assembly. Connect the power harness connector to power supply interface harness.

4. Ensure that no cables interfere with the final positioning of the DSS assembly, and seat the assembly on the top of the K450B chassis.

5. Install the six retaining screws, the two screws that secure the DSS Base and ground lug to the top of the K450B chassis. Install the four screws that secure the sides of DSS unit to the K450B chassis.

6. Reconnect the 115/230 Vac source to the K450B unit.

7. Power up the K450B and unlock the latch handle on both disk drive assemblies. Remove the cardboard insert which protects read/write heads during transport. Operation of the Dual Disk Storage System is described in the K450B User's Manual.

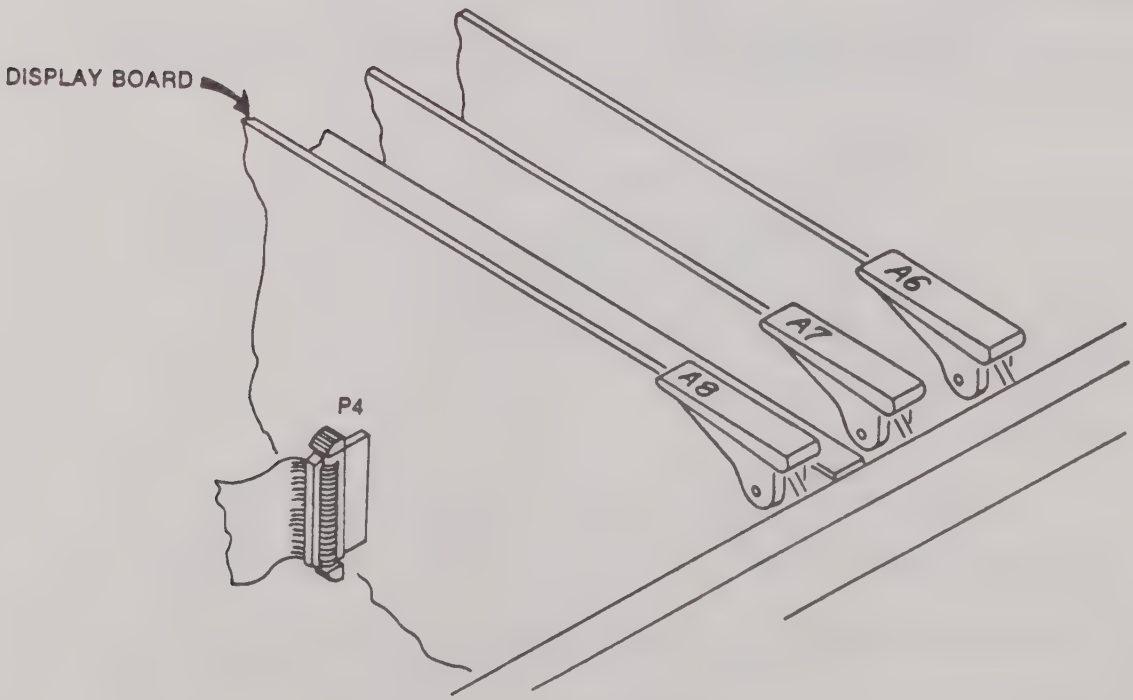


Figure 6-3. Disk Drive I/O Ribbon Cable Connection

Chapter 7

SCHEMATICS AND DRAWINGS

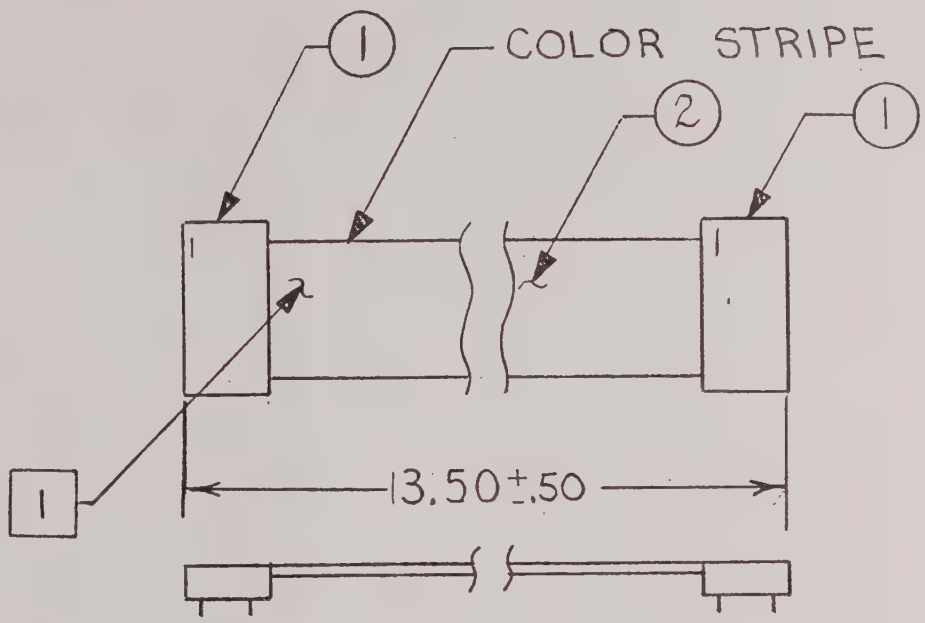
GENERAL

This chapter contains Assembly Drawings, Parts Lists, Schematic Diagrams and Wire Lists for the K450B Logic Analyzer. The drawings are arranged sequentially by part number to facilitate location by the user.

LIST OF DRAWINGS

The following drawings are provided in this chapter:

DRAWING NUMBER	DESCRIPTION
0112-0204-10	Keyboard Cable Assembly
0114-0054-10	Clock to Control Board, Cable Assembly
0114-0170-30	Threshold / GPIB / RS-232 Board Assembly
0114-0171	Threshold / GPIB / RS-232 Board Schematic
0114-0429-10	FDC Board Power-In, Cable Assembly
0114-0468-40	Dual Floppy Disk Storage, Top Assembly
0114-0481-20	FDC Board to Floppy, Power Cable Assembly
0114-0482-10	K450B to FDC Board, Signal Cable Assembly
0117-0040-30	Keyboard PCB Assembly
0117-0041	Keyboard PCB Schematic
0117-0095	100 MHz Probe Pod Schematic (Sheet #2)
0117-0099-10	Probe Subassembly
0117-0133-10	Chassis Ground Cable Assembly
0117-0626-10	DOS Ground Harness Assembly
0120-0043-01	Probe Test Cable Assembly
0120-0145-20	DOS Power Harness Assembly
0121-0037-10	FDC to Single Disk Drive Cable Assembly
0121-0082-10	K450 Fan Cable Assembly
0121-0090-10	Storage Controller Board Assembly
0121-0091	Storage Controller Board Schematic
0121-0167-10	Power Supply to Mother Board Harness Assembly
0121-0168-10	Single Disk Storage Top Assembly
0121-0200-30	Data Display Board Assembly
9000-0163	CRT and Video PCB Schematic
0121-0201	Data Display Board Schematic
0121-0205-10	CRT Board to Data Display Board Cable Assembly
0121-0405-10	Rear Casting Assembly
0121-0406-10	Chassis Top Assembly
0121-0410-10	Clock Board Assembly
0121-0411	Clock Board Schematic
0121-0415-10, -20	Data Board Assembly
0121-0416	Data Board Schematic
0121-0420-10	Control Board Assembly
0121-0421	Control Board Schematic
0121-0440-10	MPU Board Assembly
0121-0441	MPU Board Schematic
0121-0475-10	Probe Test Board Assembly
0121-0480-10	Mother Board Assembly
0121-0481	Mother Board Schematic
9000-0225-10	Power Supply Assembly Schematic



1. STAMP PART Nº, DASH Nº AND REV. LEVEL APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
10	0117-0040	1
10	0112-0120	1

KLINGLER K-VEL H

DWG. NO. 0112-0204 | SH 1 | REV. G

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
F	3871	REV'D + REDRAWN PER ECO #	STM	DGW	6-13-83
G	5454	REVISED PER ECO # 9/16	DGW	RTM	9/18/86

				1
PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION		ITEM

-40 -30 -20 -10

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES.
DIMENSIONS ARE IN INCHES AND APPLY
FOR ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .1 ANGLES ± .020 ± 1° ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

DRAWN G.GASSMAN	DATE 3-28-77
CHECKED T. McCANN	3-28-77
PROJ. ENG. ?	
MANUFACTURING ?	
QUALITY ASSUR	
G. SERV.	DATE

GOULD biomation

TITLE: KB TO FP CABLE ASSY

SCALE	SIZE	PART NUMBER	REV
	B	0112-0204	G

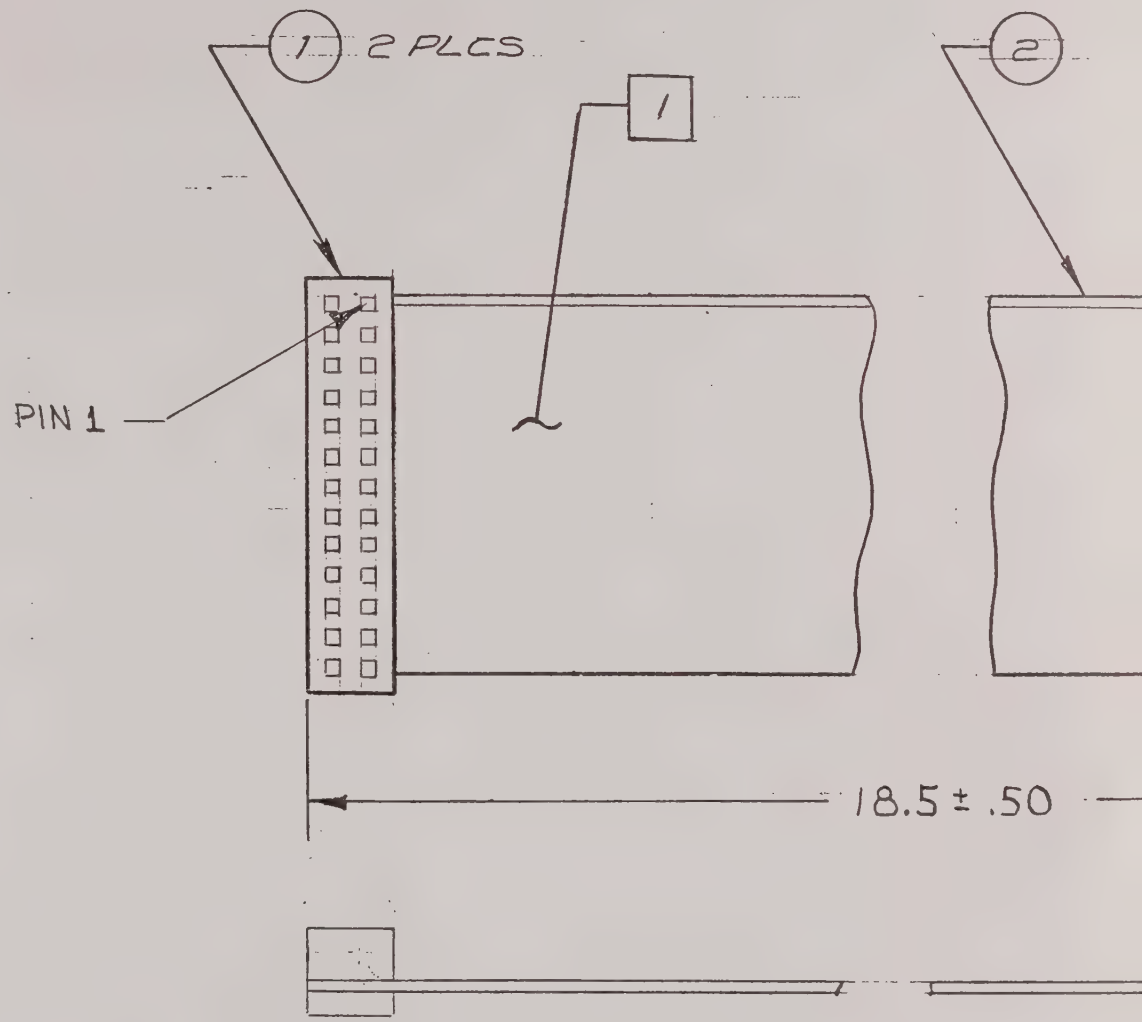
CODE K100 / K105 SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0112-0204-10 ASSY,CBL,KB TO FP
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0112-0204	DWG,ASSY,CABLE,KB TO FP	0	EA	REF
1	6000-0114-10	CONN 16 PIN DIP	2	EA	
2	7100-0028-10	CBL,FLAT,16 COND	1	FT	
2	7100-0095-10	CABLE,RIBBON FLAT 16 COND	13	FT	



1 STAMP WITH PART Nº, DASH Nº AND REV. LEVEL APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-10	0114-0160	1

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-4427

DWG. NO. 0114-0054 | SH 1 | REV. C

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		REL. PER ERN #116	JKP	[illegible]	
A		PROD REL ERN # 203	[illegible]	RG	10/8/81
B	2172	REVISED PER ECO#	JWC	RG	11-9-81
BRC	4634	PER ECO	George	DLW JMS	7/11/84
C	5454	REVISED PER ECO# 9/16	DLW	RTM	9/18/86

								1
0	−40	−30	−20	−10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

O NOT SCALE DRAWING

OVE ALL BURRS AND SHARP EDGES.
ENSIONS ARE IN INCHES AND APPLY
R ADDED FINISHES EXCEPT PAINT.
FACE ROUGHNESS

TOLERANCE

NSIONAL:	HOLE SIZE:
.1 ANGLES	.0-.599 ± .003
± .020 ± 1°	.600-.999 ± .004
± .010	1.000-1.499 ± .005

G. SERV.	DATE
[illegible]	10/8/81

DRAWN	J. PERGINS	DATE 3/10/81
CHECKED	[illegible]	3·17·81
PROJ. ENG.	Curt	10.8.81
MANUFACTURING	[illegible]	10/9/81
QUALITY ASSUR	[illegible]	[illegible]

GOULD biomation

TITLE CABLE ASSEMBLY- CLOCK BD. TO CONTROL BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0114-0054	C

CODE K101 | SHEET 1 OF 1

BILL OF MATERIAL

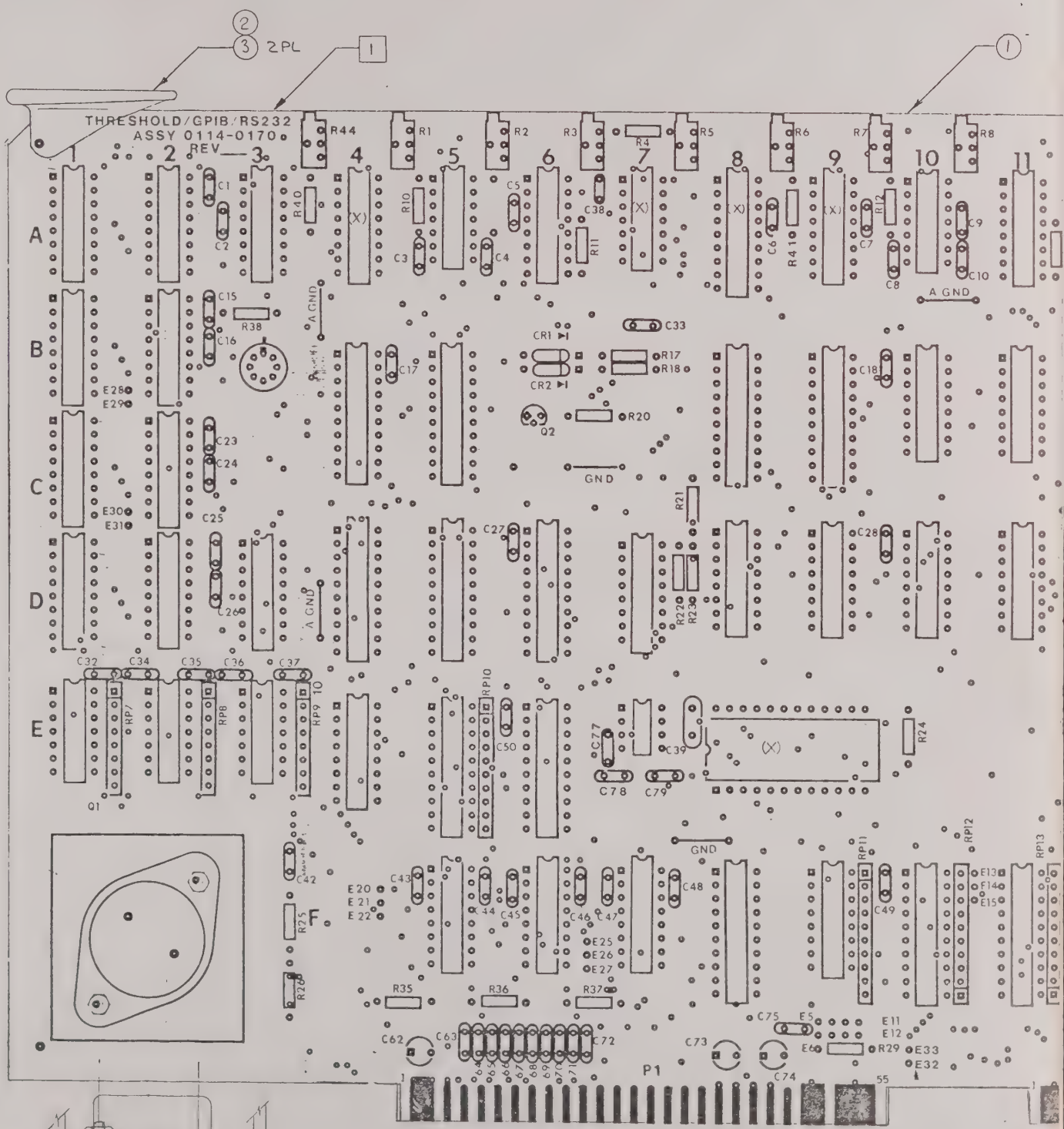
AS OF 10/30/87

0114-0054-10 ASSY,CBL,CLOCK BD TO CTRL BD
MODEL: K101

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0114-0054	DWG,ASSY,CABLE	0	EA	REF
1	6000-0272-10	CONN 20 PIN SKT	2	EA	
2	7100-0091-10	CBL,FLAT,20 COND	2	FT	
3	7200-0048-10	CABLE MARKER	1	EA	

NOTES: UNLES OTHERWISE SPECIFIED.

1. MARK ASSY DASH NO. AND REV LEVEL APPROX WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. (X) INDICATES SOCKET LOCATIONS - REF ONLY.



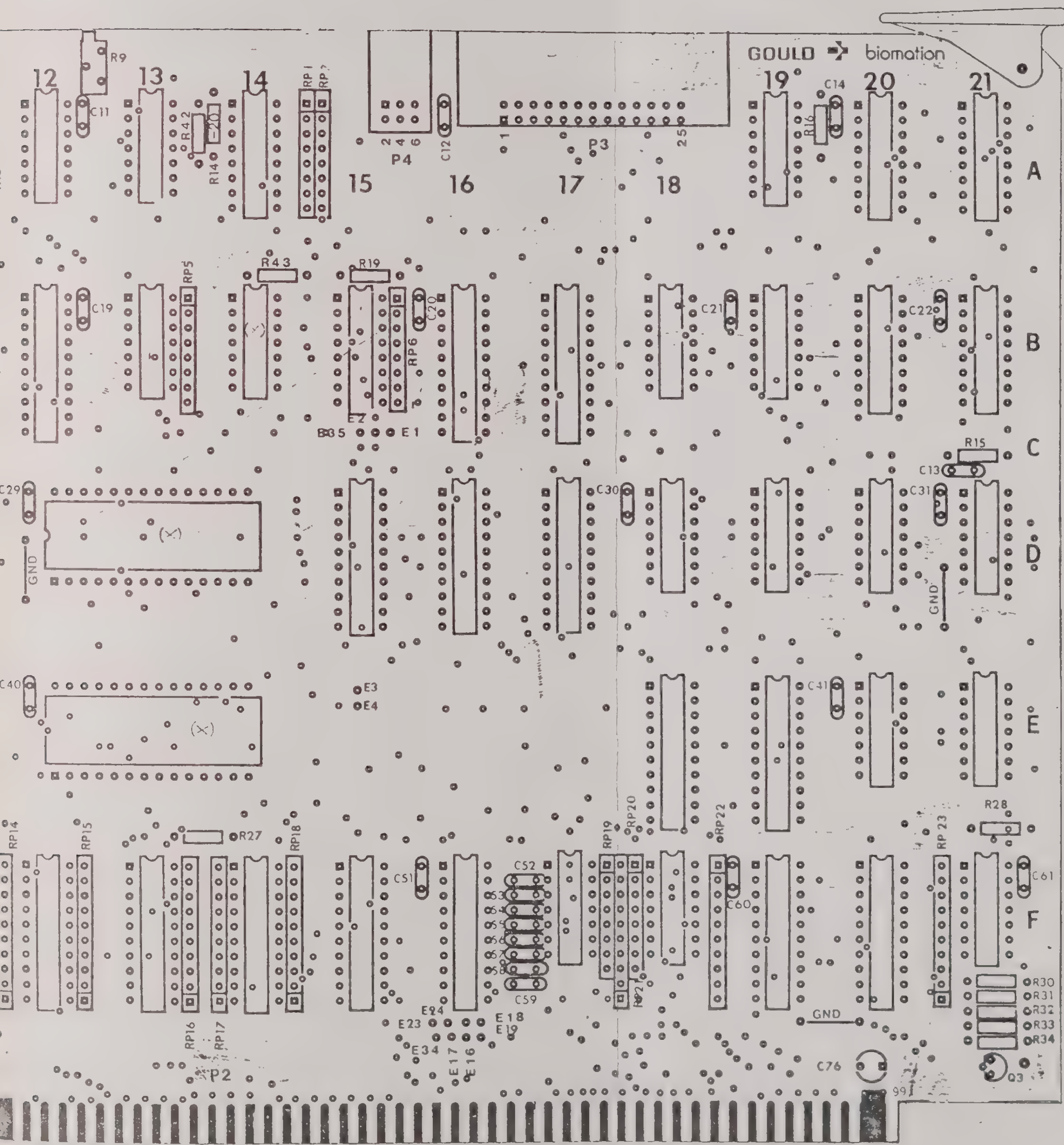
JUMPER LIST						DESCRIPTION	REF DES	AS ETCH
DESCRIPTION	REF DES	AS ETCH	K500 -10	K101 -20	K205 -30	SELECT M/IO	E13-E14	IN
RS449 RC	E1-E2	IN				SELECT IO PAGE	E4-E15	OUT
INTR 3	E3-E4	IN				RS449 SG	E16-E17	OUT
SELECT A11	E5-E6	IN				RS449 SC	E18-E19	IN
SELECT A10	E7-E8	OUT				SELECT+11V MONITOR	E20-E21	OUT
SELECT A9	E9-E10	OUT				SELECT VBB MONITOR	E22-E24	IN
SELECT A8	E11-E12	IN						
INTR 2	E23-E24	IN						

KLINGLER K-VEL M

AE	5805	REV ROLL ONLY	9/1/87	MM	DLW	9/3/87

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE HISTORY.			
	Z	405?	REVISED PER ECO.	[illegible]	DLW	[illegible]
	AA	4277	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	AB	4384	REVISED PER ECO	[illegible]	[illegible]	3/27/84
	AC	4909	REVISED PER ECO 5-7-85.	SAR	DLW	[illegible]
	AD	5520	REVISED PER ECO 12-16-86	MM	DLW	[illegible]
	AD-RC	5662	RECORD CHANGE ONLY 3/9-87	MM	DGW	3/13



-10	-20	-30	DESCRIPTION	REF DES	AS ETCH	-10	-20	-30
CUT				E25-E26	IN	CUT		
JUMPER				E26-E27	OUT	JUMPER		
	JMP			E28-E29	OUT		JUMPER	
CUT				E30-E31	OUT		JUMPER	
JUMPER			INTA	E32-E33	IN	CUT		
—				E17-E34	IN	CUT	CUT	
				E2-E35	IN	CUT	CUT	

								1
-50	-40	30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES. SYMBOLS OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1, .XX = .020, .XXX = .010; ANGLES ± 1°

ENG. SERV. DATE

DRAWN J. WELDON	DATE [illegible] 30-8
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	

GOULD biomation

TITLE ASSEMBLY THRESHOLD/GPIB/RS232

SCALE	SIZE	PART NUMBER	REV
2:1	D	0114-0170	AE

CODE [illegible] SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0114-0170	DWG,ASSY,THRESHOLD/GPIB/RS232	0	EA	REF
0	D0114-0171	DWG,SCHEM,THRESHOLD/GPIB,RS232	0	EA	REF
1	0114-0172-10	FAB PCB,THRESHOLD/GPIB,RS232	1	EA	
2	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
3	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
5	1700-0086-10	IC LM324AN QUAD OP AMP	4	EA	10A 1E,2E,5A
6	1700-0063-20	IC REF-01EJ VOLT REF	1	EA	3B
8	1820-0077-10	IC MP7533CD MULT DAC	2	EA	4A,9A
9	1820-0076-10	IC MP7508DIJN ANA MULT	11	EA	1A-1D,2A 2D,5F,6F 7F,2B,2C
10	1820-0075-10	IC AD7541 12BIT MONO MLT DAC	1	EA	8A
11	1800-0342-10	IC P8251A PROG COMM	2	EA	12D,12E
12	1800-0344-10	IC P8253-5 PROG INTER	1	EA	8E
13	1700-0101-10	IC DS1488N DR RS232	2	EA	13A,13B
14	1700-0102-10	IC AM26LS32PC QUAD DIFF	2	EA	14A,15B
15	1800-0200-10	IC 7433N QUAD 2-IN	1	EA	14B
16	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	1	EA	8D
17	1800-0231-10	IC 74LS273N 20 FF, D, X8	13	EA	15D,5E,6E 15F,12B 18E,19E 4B,5B,8B 9B,4D,6D
19	1800-0267-10	IC 74LS240N OCTAL LINE	5	EA	13F,16F 17B 20F,16B
20	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	5	EA	16D,17D 8F,10F,11F
21	1800-0268-10	IC 74LS245N BUS TRANS	2	EA	12F,14F
22	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	5	EA	10B,9D-11D 11B
24	1800-0311-10	IC 7438N QUAD 2-INPUT	7	EA	17F,18F 19D,20E 21E 21F,18D
25	1800-0110-10	IC 74LS10N TRIPLE NAND	1	EA	18B
26	1800-0105-10	IC 74LS00N 2-IN NAND LOW	3	EA	20D 21D,19B
27	1800-0068-10	IC 74LS112N DUAL J-K FF	4	EA	20A,21A 20B,21B
28	1800-0111-10	IC 74LS20N DUAL 4-IN	1	EA	12A
29	1800-0309-10	IC 74LS260PC DUAL 5 INPUT	1	EA	19A
31	1700-0071-10	IC LF356AN MONO OP AMP	1	EA	7E
32	1700-0106-10	IC OP-11EP OP AMP	1	EA	7A
33	3000-3300-10	RES,330,5%,1/4W,C	3	EA	R15,23,33

BILL OF MATERIAL
AS OF 10/30/87

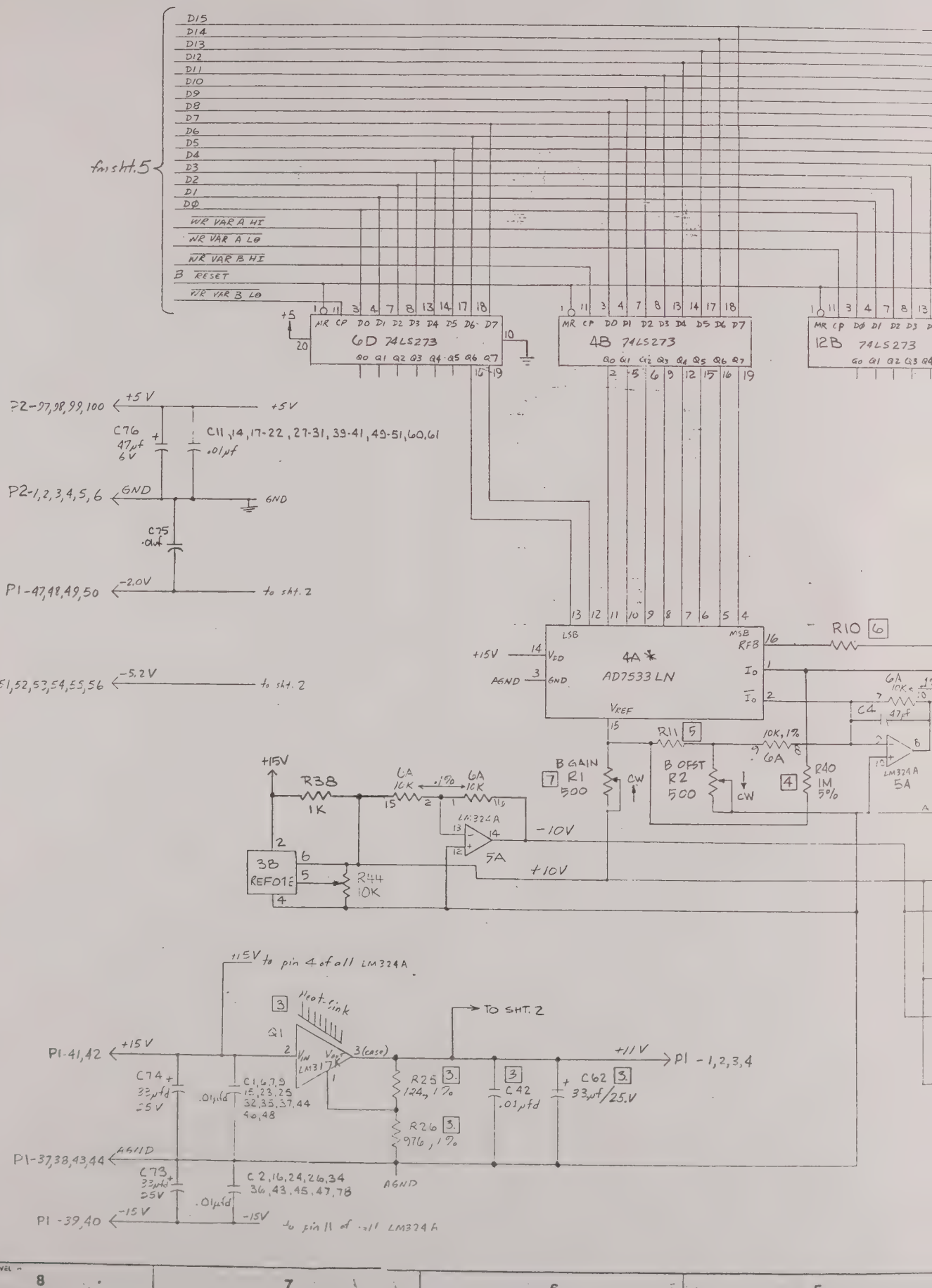
0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
34	3000-2201-10	RES,2.2K,5%,1/4W,C	6	EA	30,14,19 R20,24,28
35	3000-1001-10	RES,1K,5%,1/4W,C	4	EA	R35-38
36	3000-2200-10	RES,220,5%,1/4W,C	3	EA	R16,22,39
37	3000-1004-10	RES,1M,5%,1/4W,C	2	EA	R40,41
38	3000-2006-10	RES,20,5%,1/4W,C	1	EA	R31
39	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R34
40	3000-2701-10	RES,2.7K,5%,1/4W,C	1	EA	R21
41	3000-2002-10	RES,20K,5%,1/4W,C	3	EA	R18,42,43
45	3100-1003-10	RES,100K,1%,1/8W,MF	1	EA	R4
46	3100-4990-10	RES,499,1%,1/8W,MF	1	EA	R17
47	3000-3302-10	RES,33K,5%,1/4W,C	2	EA	R11,13
48	3300-0070-10	POT,10K,0.5W,10% 20T,PC,RTANG	3	EA	R7,8,44
49	3300-0060-10	POT,500,0.5W,10% 25T,PC,RTANG	4	EA	R2,3,5,9
50	3300-0012-10	POT,1K,0.5W,10% 20T,PC,RTANG	2	EA	R1,6
51	3700-0048-10	RPAK,10K,0.1W,16/8	4	EA	6A,11A,4E 7D
52	3700-0083-10	RPAK,2.2K,0.18W,2%,10/9	2	EA	RP10,11
53	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	9	EA	23 RP12-18,20
54	3700-0084-10	RPAK,2.7K,0.2W,2%,8/4	2	EA	RP2,6
55	3700-0056-10	RPAK,180,0.2W,2%,8/4	4	EA	5 RP19,21,1
56	3700-0076-10	RPAK,47,.2W,2%,8/4	2	EA	RP7,8
57	3000-7500-10	RES,750,5%,1/4W,C	2	EA	R10,12
58	1000-0003-10	DIO,5082-2811	2	EA	CR1,2
59	1300-0028-10	TRAN 2N3904	1	EA	Q2
60	1400-0019-10	TRAN 2N3906	1	EA	Q3
61	3000-2001-10	RES,2K,5%,1/4W,C	1	EA	R27
62	3000-3001-10	RES,3K,5%,1/4W,C	1	EA	R29
63	4010-0103-10	CAP,0.01UF,50V,10%,CER	46	EA	14-32 34-37 39-41 43-51 75,78,79 9,11,60,61 C1,2,6,7
65	4010-0470-10	CAP,47PF,50/100V,5%/10%,CER	16	EA	13,33,38 52-59 C3-5,8,10
66	4010-0471-10	CAP,470PF,50/100V,5%,CER	1	EA	C77
67	4010-0104-10	CAP,0.1UF,50V,10%,CER	10	EA	C63-72
68	4400-0045-10	CAP,33UF,25V,ELCTLT	2	EA	C73,74
69	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	1	EA	C76
71	6000-0417-10	CONN 6 PIN HDR RT ANGLE	1	EA	P4
72	6000-0388-20	CONN 26 PIN RT ANGLE HDR	1	EA	P3

BILL OF MATERIAL
AS OF 10/30/87

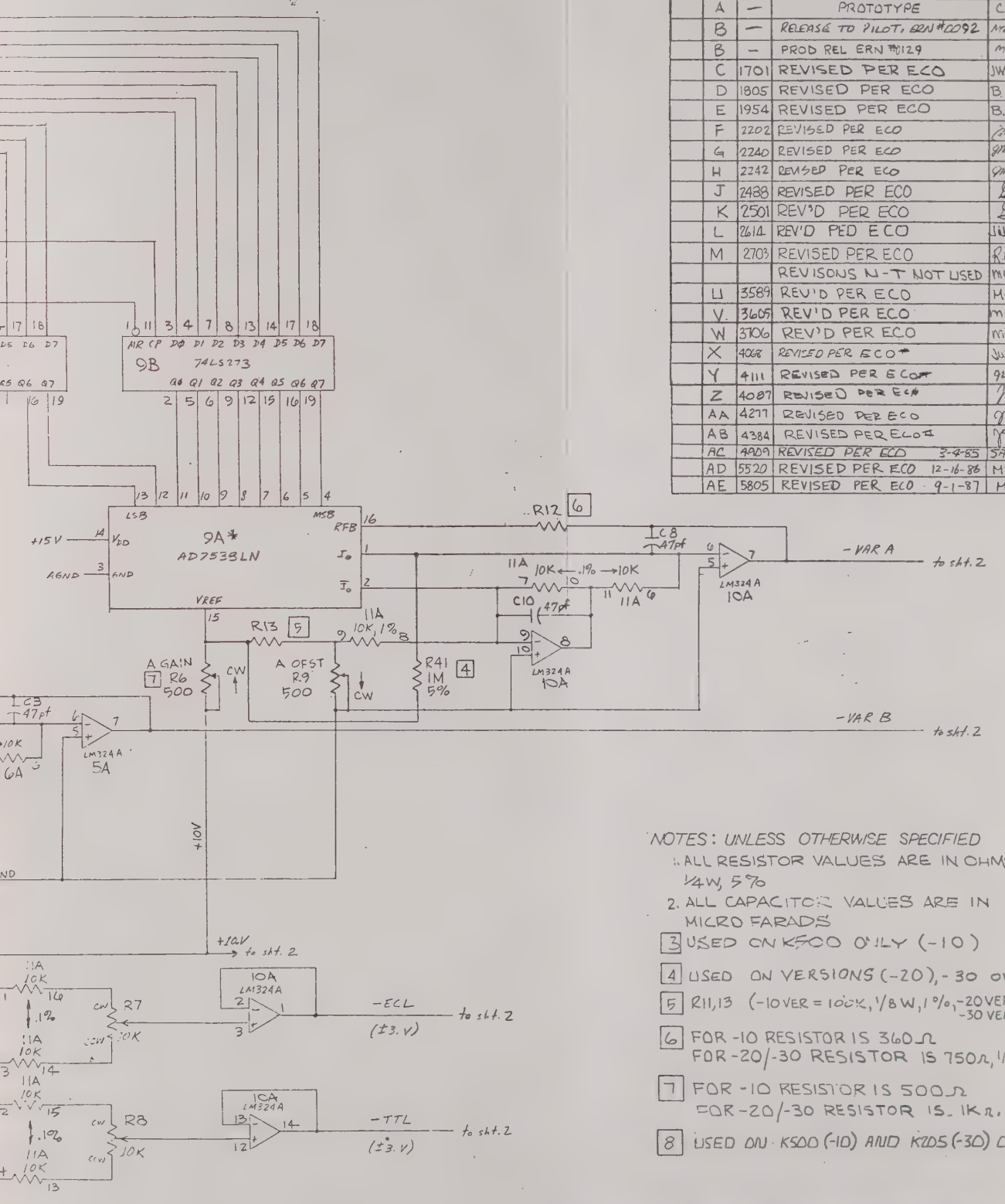
0114-0170-30 ASSY,PCB,THRESHOLD,GPIB,RS232
MODEL:

ITEM #	PART NUMBER		DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
74	6100-0119-10	SKT	14 PIN DIP LO-PROFIL	2	EA	X7A,X14B
75	6100-0120-10	SKT	16 PIN DIP LO-PROFIL	2	EA	X4A,9A
76	6100-0156-10	SKT	18 PIN	1	EA	X8A
77	6100-0122-10	SKT	24 PIN DIP	1	EA	X8E
78	6100-0151-10	SKT	28 PIN DIP LO PROFIL	2	EA	X12D,X12E



fm sht. 5
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
DØ
WR VAR A HI
WR VAR A LO
WR VAR B HI
B RESET
WR VAR B LO
6D 74LS273
4B 74LS273
12B 74LS273
P2-97,98,99,100
+5V
C76 47µf 6V
C11,14,17-22,27-31,39-41,49-51,60,61 .01µf
P2-1,2,3,4,5,6
GND
C75 .01µf
P1-47,48,49,50
-2.0V
to sht. 2
P1-51,52,53,54,55,56
-5.2V
4A * AD7533 LN
+15V
AGND
R10 6
R11 5
10K, 1%
6A
B GAIN R1 500
B OFST R2 500
CW
R40 1M 5%
C4 47pf
LM324A 5A
R38 1K
6A 10K
.1%
LM324A 5A
-10V
+10V
3B REF01E
R44 10K
+15V to pin 4 of all LM324A
Heat-sink
Q1
LM317K
TO SHT. 2
P1-41,42
+11V
P1 -1,2,3,4
C74 33µfd 25V
C1,6,7,9 15,23,25 32,35,37,44 46,48
.01µfd
R25 3. 124, 1%
R26 3. 976, 1%
C42 .01µfd
C62 3. 33µf/25.V
P1-37,38,43,44
AGND
C73 33µfd 25V
C2,16,24,26,34 36,43,45,47,78
P1 -39,40
-15V
to pin 11 of all LM324A

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	—	PROTOTYPE	CB		
	B	—	RELEASE TO PILOT, ERN #0092	MR		
	B	—	PROD REL ERN #0129	MB	RG	11/81
	C	1701	REVISED PER ECO	JWC	JL	
	D	1805	REVISED PER ECO	B.H.	JW	[illegible]
	E	1954	REVISED PER ECO	B.H.	JW	[illegible]
	F	2202	REVISED PER ECO	[illegible]	JW	[illegible]
	G	2240	REVISED PER ECO	[illegible]	JW	[illegible]
	H	2242	REVISED PER ECO	[illegible]	JW	[illegible]
	J	2488	REVISED PER ECO	[illegible]	[illegible]	[illegible]
	K	2501	REV'D PER ECO	[illegible]	[illegible]	[illegible]
	L	2614	REV'D PER ECO	JWC	T.J.	[illegible]
	M	2703	REVISED PER ECO	RR	JW	[illegible]
			REVISIONS N-T NOT USED	MW	DGW	5-16
	U	3589	REV'D PER ECO	MW	DGW	5-16
	V	3605	REV'D PER ECO	MW	DGW	5-16
	W	3706	REV'D PER ECO	MW	DGW	[illegible]
	X	4068	REVISED PER ECO	[illegible]	DGW MR	[illegible]
	Y	4111	REVISED PER ECO	[illegible]	DGW	[illegible]
	Z	4087	REVISED PER ECO	[illegible]	DGW MR	[illegible]
	AA	4277	REVISED PER ECO	[illegible]	DGW MR	[illegible]
	AB	4384	REVISED PER ECO	[illegible]	MR MR	[illegible]
	AC	4909	REVISED PER ECO 3-4-85	SAR	DGW	[illegible]
	AD	5520	REVISED PER ECO 12-16-86	MM	DGW	[illegible]
	AE	5805	REVISED PER ECO 9-1-87	MM	DGW	[illegible]



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, 5%
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS

[3] USED ON K500 ONLY (-10)

[4] USED ON VERSIONS (-20), -30 ONLY

[5] R11,13 (-10 VER = 100K, 1/8W, 1%, -20 VER = 33K, -30 VER = 33K

[6] FOR -10 RESISTOR IS 360Ω
FOR -20/-30 RESISTOR IS 750Ω, 1/8W, 1%

[7] FOR -10 RESISTOR IS 500Ω
FOR -20/-30 RESISTOR IS 1KΩ.

[8] USED ON K500 (-10) AND K1025 (-30) ONLY.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							THRESHOLD DAC'S	1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .03 = 1°; XXX = .010
HOLE SIZE: 0 399 = 003; 600 999 = 004; 1 000-1 499 = 005

DASH NO	NUMBER NEXT ASSEMBLY	QTY

ENG. SERV. DATE

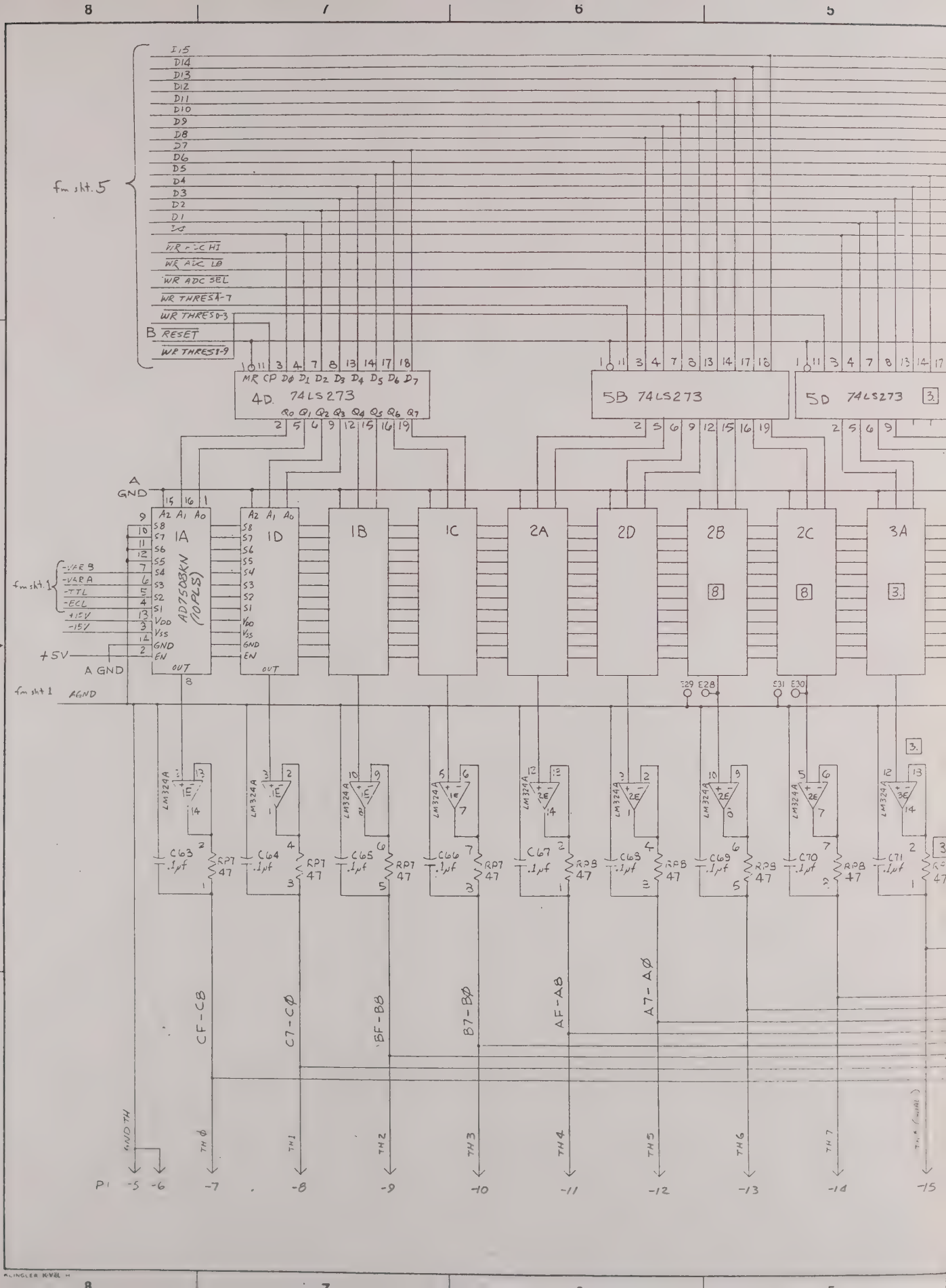
DRAWN	Curt	DATE 1-4-83
CHECKED	R. Dean	4/10/83
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		

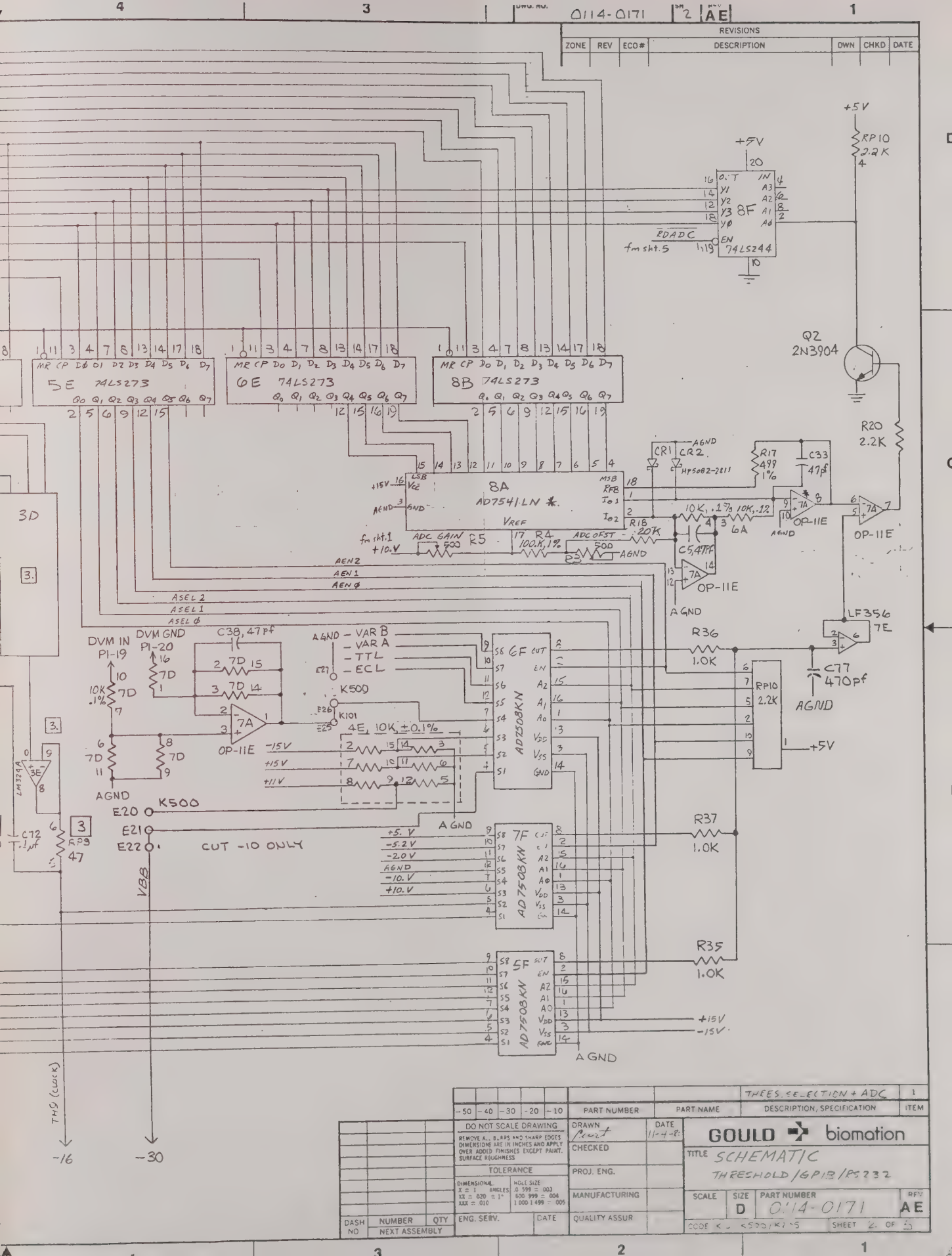
GOULD biomation

TITLE SCHEMATIC
THRESHOLD DAC, RS232

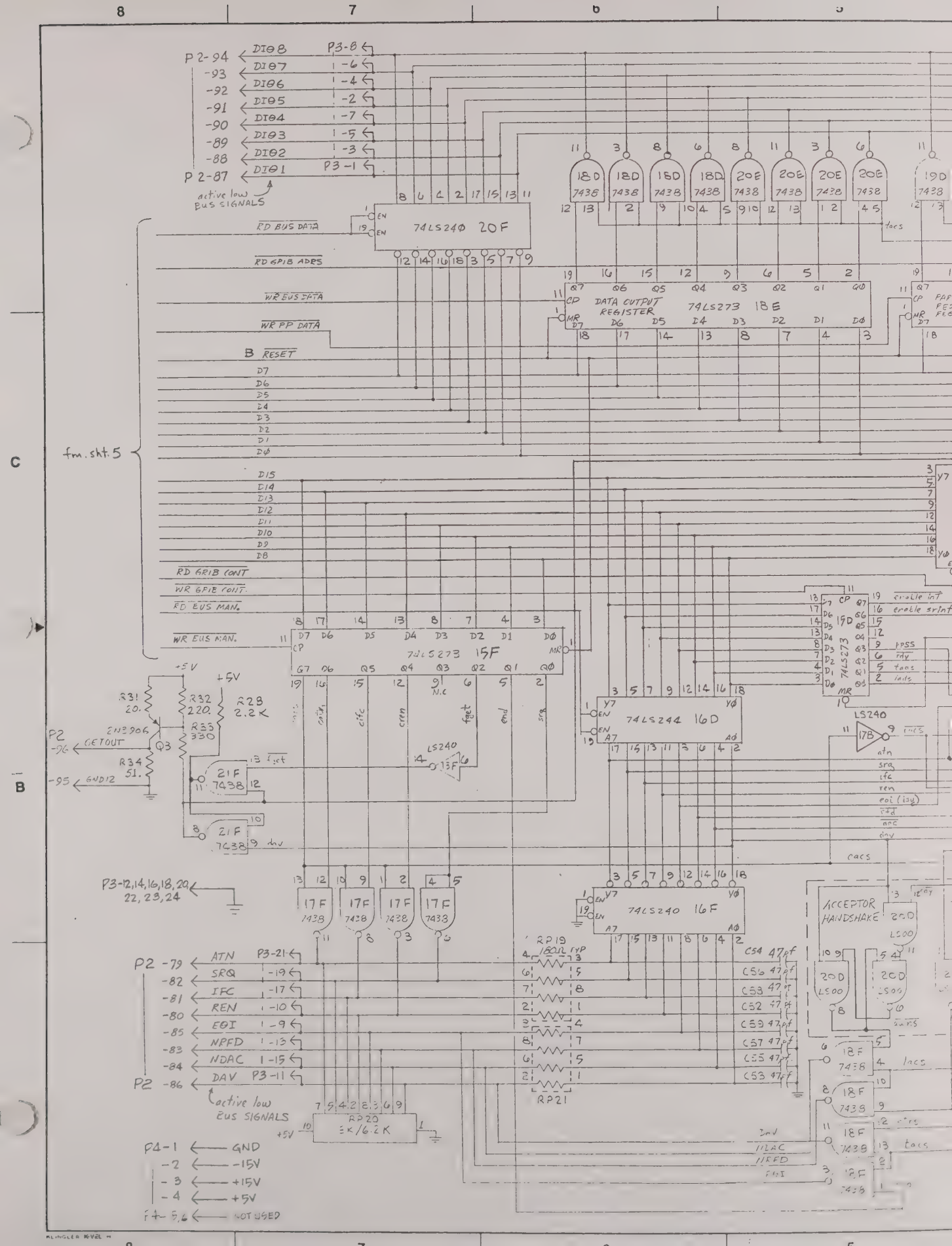
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0171	AE

CODE XIO1/K501/K1025 SHEET 1 OF 5

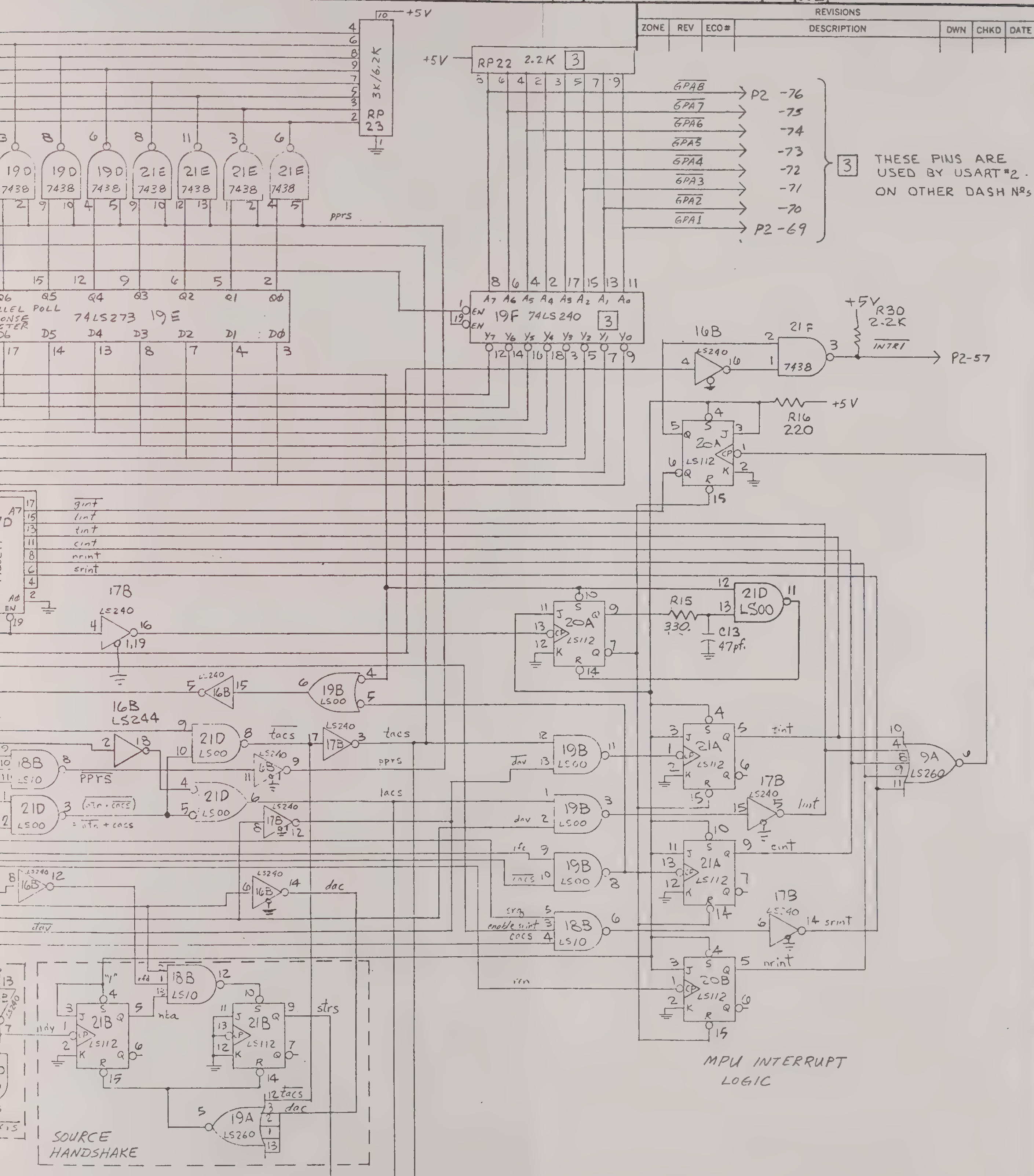

fm sht. 5
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D0
WR ADC HI
WR ADC LO
WR ADC SEL
WR THRES A-7
WR THRES D-3
B RESET
WR THRES B-9
4D 74LS273
5B 74LS273
5D 74LS273
A GND
AD7508KN (10PLS)
1A
1D
1B
1C
2A
2D
2B
2C
3A
fm sht. 1
-VREB
-VREA
-TTL
-ECL
+15V
-15V
+5V
A GND
AGND
LM324A
C63 .1μf
C64 .1μf
C65 .1μf
C66 .1μf
C67 .1μf
C68 .1μf
C69 .1μf
C70 .1μf
C71 .1μf
RP7 47
RP8 47
CF-C8
C7-C0
BF-B8
B7-B0
AF-A8
A7-A0
GND TH
TH 0
TH 1
TH 2
TH 3
TH 4
TH 5
TH 6
TH 7
P1 -5 -6 -7 -8 -9 -10 -11 -12 -13 -14 -15



0114-0171
SH 2
REV AE
REVISIONS
ZONE
REV
ECO#
DESCRIPTION
DWN
CHKD
DATE
+5V
RP10 2.2K
8F 74LS244
RDADC
fm sht.5
Q2 2N3904
R20 2.2K
5E 74LS273
6E 74LS273
8B 74LS273
8A AD7541LN
CR1
CR2
HP5082-2811
R17 499 1%
C33 47pf
OP-11E
R18 20K
C5,47PF
6A
AGND
LF356 7E
R36 1.0K
C77 470pf
RP10 2.2K
3D
ADC GAIN 500
R5
R4 100K,1%
ADC OFST 500
R3
AEN2
AEN1
AEN0
ASEL2
ASEL1
ASEL0
DVM IN P1-19
DVM GND P1-20
C38, 47pf
10K .1%
7A
OP-11E
AGND
VAR B
VAR A
TTL
ECL
K500
K101
4E, 10K, ±0.1%
-15V
+15V
+11V
6F AD7508KN
7F AD7508KN
5F AD7508KN
E20
E21
E22
CUT -10 ONLY
VBB
LM324A
C72 .1µf
RP9 47
R37 1.0K
R35 1.0K
+15V
-15V
THS (CLOCK)
-16
-30
THRES. SELECTION + ADC
1
-50 -40 -30 -20 -10
PART NUMBER
PART NAME
DESCRIPTION, SPECIFICATION
ITEM
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DIMENSIONAL
HOLE SIZE
DRAWN
DATE 11-4-8
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DATE
DASH NO
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE
SIZE D
PART NUMBER 0114-0171
REV AE
CODE
SHEET 2 OF 5



P2-94 DIØ8 P3-8
-93 DIØ7 -6
-92 DIØ6 -4
-91 DIØ5 -2
-90 DIØ4 -7
-89 DIØ3 -5
-88 DIØ2 -3
P2-87 DIØ1 P3-1
active low BUS SIGNALS
RD BUS DATA
RD GPIB ADRS
WR BUS DATA
WR PP DATA
B RESET
D7
D6
D5
D4
D3
D2
D1
DØ
fm. sht. 5
D15
D14
D13
D12
D11
D10
D9
D8
RD GPIB CONT
WR GPIB CONT
RD BUS MAN.
WR BUS MAN.
74LS240 20F
18D 7438
20E 7438
19D 7438
DATA OUTPUT REGISTER
74LS273 18E
74LS273 15F
74LS244 16D
74LS240 16F
74LS273 19D
LS240 17B
LS240 13F
21F 7438
17F 7438
18F 7438
ACCEPTOR HANDSHAKE
20D LS00
RP19 180Ω TYP
RP21
RP20 3K/6.2K
+5V
R31 20.
R32 220.
R28 2.2K
R33 330
R34 51.
2N3906 Q3
P2 -96 GETOUT
-95 GND12
P3-12,14,16,18,20,22,23,24
P2 -79 ATN P3-21
-82 SRQ -19
-81 IFC -17
-80 REN -10
-85 EOI -9
-83 NRFD -13
-84 NDAC -15
P2 -86 DAV P3-11
active low BUS SIGNALS
P4-1 GND
-2 -15V
-3 +15V
-4 +5V
P4-5,6 NOT USED
C54 47pf
C56 47pf
C58 47pf
C52 47pf
C59 47pf
C57 47pf
C55 47pf
C53 47pf
DAV
NDAC
NRFD
EOI
tacs
atn
srq
ifc
ren
eoi (isy)
rfd
dac
dav
eacs
enable int
enable srint
PPSS
rdy
tacs
lads



ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE

REVISIONS

			6PIB (488) INTERFACE		1
-50 -40 -30 -20 -10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION		ITEM

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. DATE

DRAWN Curt — DATE 11-4-8?

CHECKED

PROJ. ENG.

MANUFACTURING

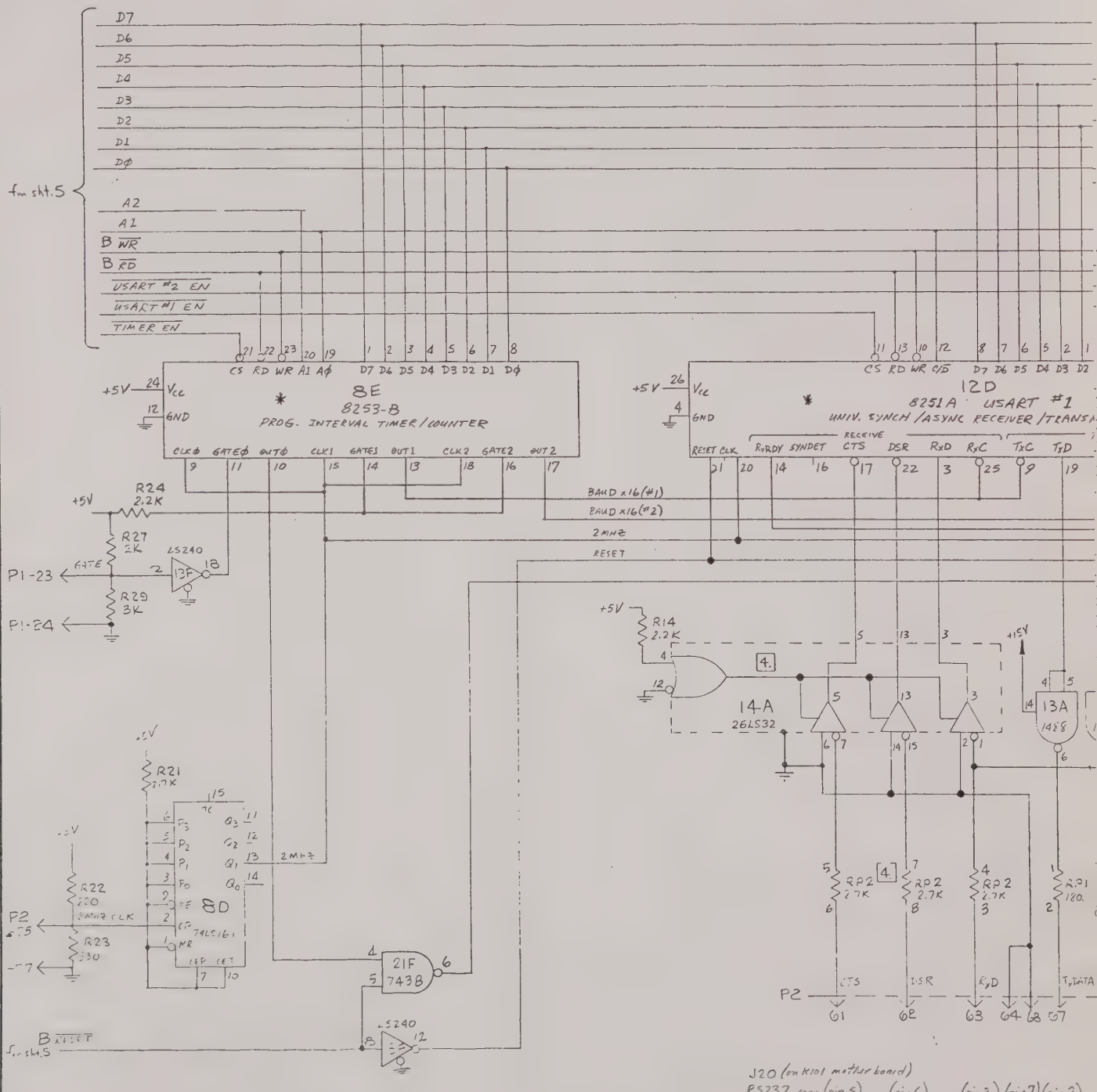
QUALITY ASSUR

GOULD biomation

TITLE SCHEMATIC THRESHOLD / GPIB / RS232

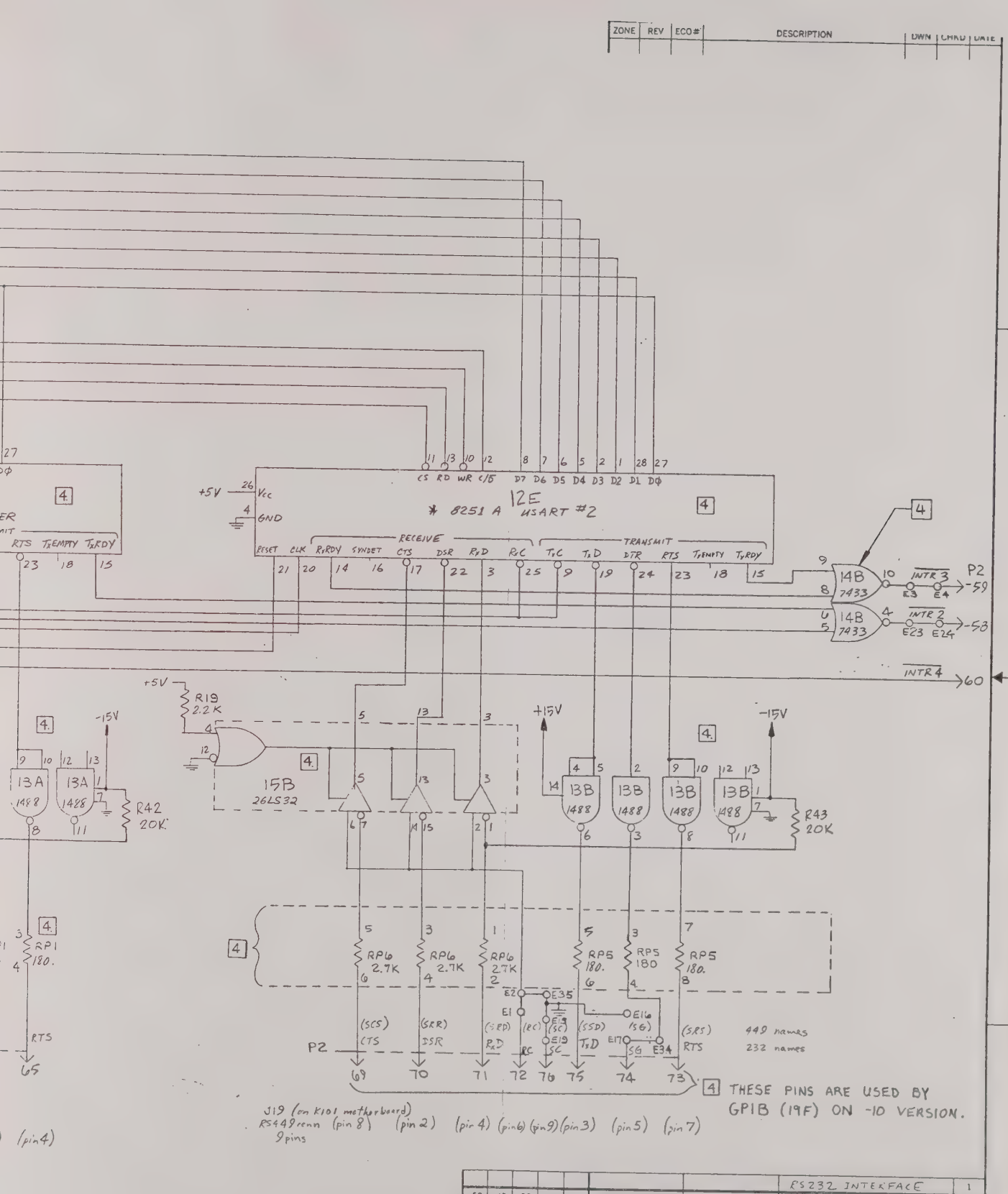
SCALE — SIZE D PART NUMBER 0114-0171 REV AE

CODE < SHEET 2 OF 5



J20 (on K101 mother board)
RS232 conn (pin 5) (pin 6) (pin 3) (pin 7) (pin 2)
25 pins

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
		RS232 INTERFACE	1

-50 -40 -30 -20 -10

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDITIONS EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; .XX = .020 = 1°; .XXX = .010

HOLE SIZE: 0.599 = 003; 600.999 = 004; 1.000-1.499 = 005

	DRAWN	DATE
	Curt	11-4-81
	CHECKED	
	PROJ. ENG.	
	MANUFACTURING	
ENG. SERV.	QUALITY ASSUR	

DASH NO | NUMBER NEXT ASSEMBLY | QTY | DATE

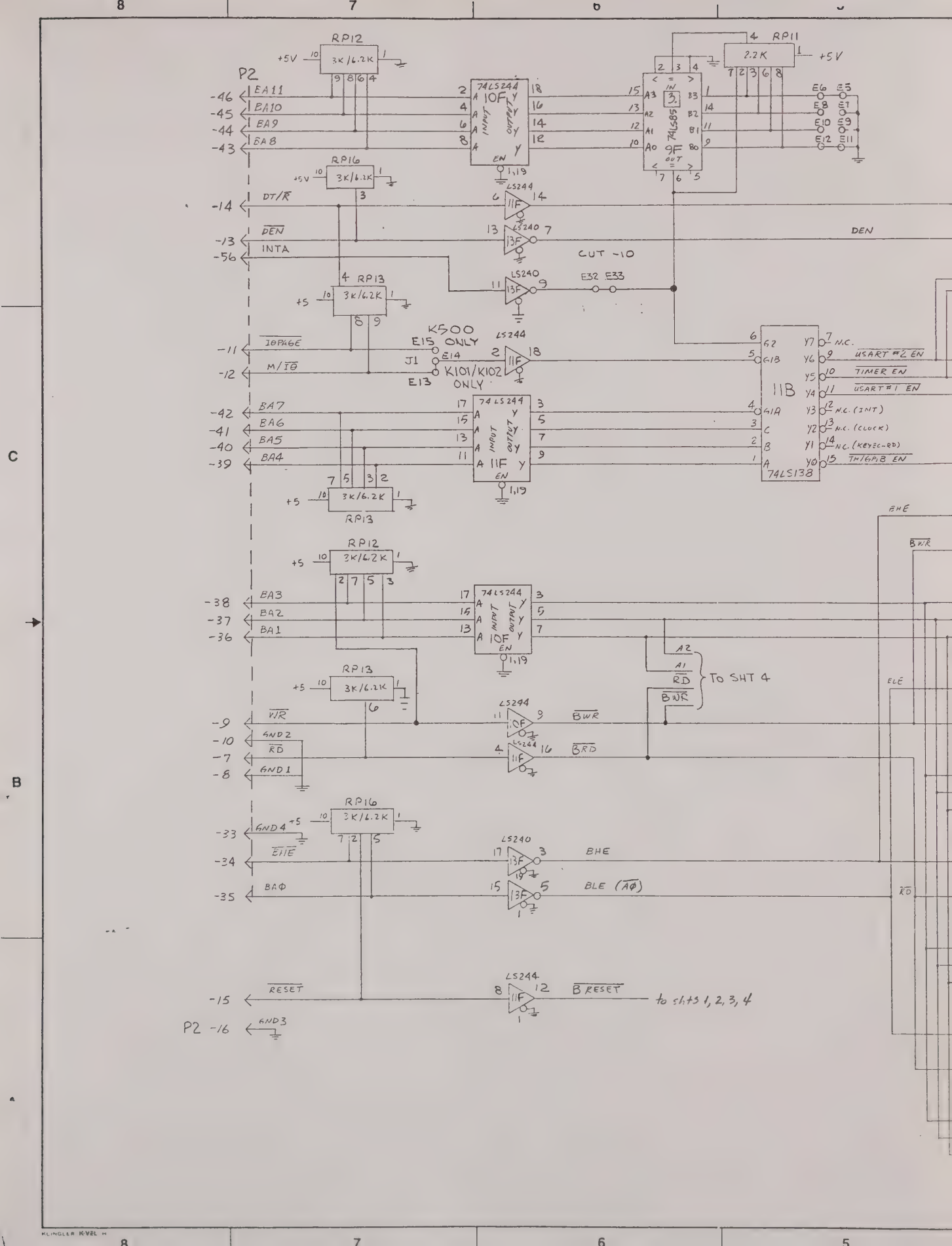
GOULD biomation

TITLE SCHEMATIC
THRESHOLD/GPIB/RS232

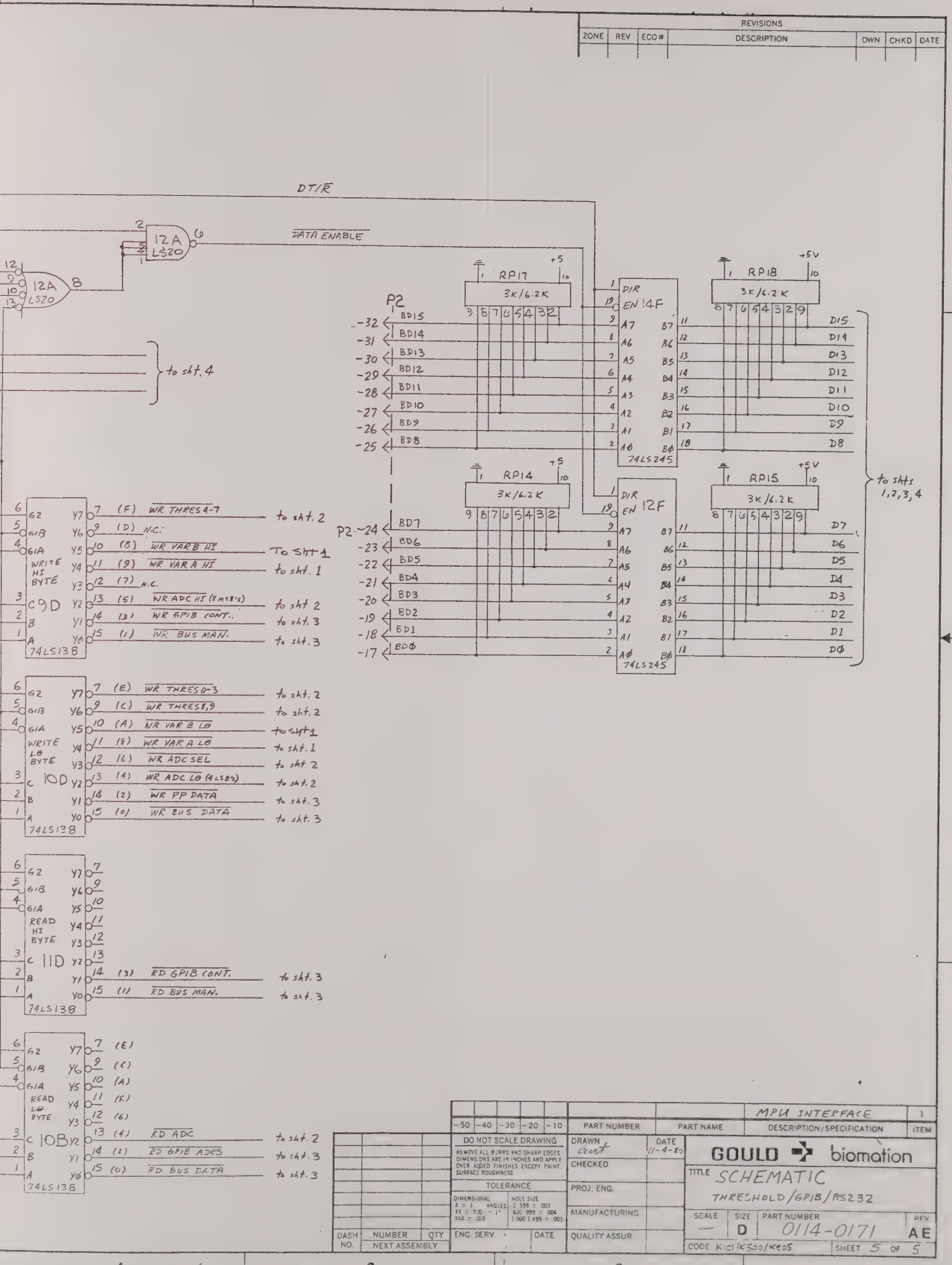
SCALE	SIZE	PART NUMBER	REV
—	D	0114-0171	AE

CODE K101/K500/4795 SHEET 4 OF 5

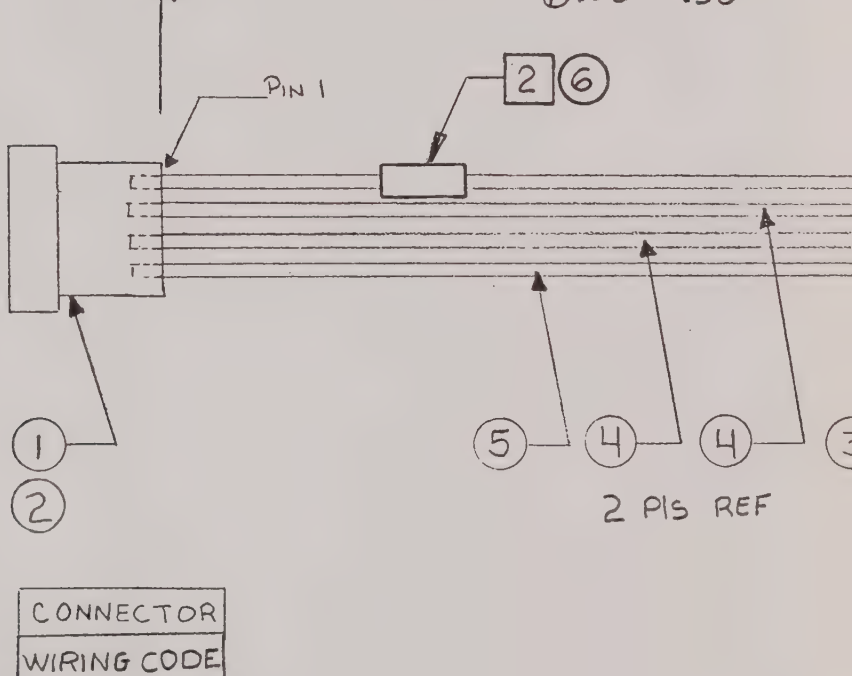
4 3 2 1



RP12
3K/6.2K
+5V
P2
-46 EA11
-45 BA10
-44 BA9
-43 BA8
74LS244
10F
INPUT
OUTPUT
EN
RP11
2.2K
+5V
74LS85
9F
IN
OUT
E6 E5
E8 E7
E10 E9
E12 E11
RP16
3K/6.2K
+5V
-14 DT/R
LS244
11F
-13 DEN
-56 INTA
LS240
13F
DEN
CUT -10
E32 E33
RP13
3K/6.2K
+5
-11 IOPAGE
-12 M/IO
K500 ONLY
E15
E14
J1
E13
K101/K102 ONLY
LS244
11F
11B
74LS138
N.C.
USART #2 EN
TIMER EN
USART #1 EN
N.C. (INT)
N.C. (CLOCK)
N.C. (KEYBOARD)
TH/GPIB EN
-42 BA7
-41 BA6
-40 BA5
-39 BA4
74LS244
11F
RP13
3K/6.2K
+5
RP12
3K/6.2K
+5
-38 BA3
-37 BA2
-36 BA1
74LS244
10F
RP13
3K/6.2K
+5
A2
A1
RD
BWR
To SHT 4
-9 WR
-10 GND2
-7 RD
-8 GND1
LS244
10F
BWR
LS244
11F
BRD
RP16
3K/6.2K
+5
-33 GND4
-34 BHE
-35 BAΦ
LS240
13F
BHE
BLE (AΦ)
LS244
11F
-15 RESET
B RESET
to shts 1, 2, 3, 4
P2 -16 GND3
BHE
BWR
ELE
RD



REVISIONS
ZONE REV ECO# DESCRIPTION DWN CHKD DATE
DT/R
DATA ENABLE
12A LS20
12A LS20
to sht. 4
RP17 3K/6.2K
RP18 3K/6.2K
RP14 3K/6.2K
RP15 3K/6.2K
+5
+5V
P2
14F
12F
74LS245
to shts 1,2,3,4
WRITE HI BYTE
C9D
74LS138
WR THRES 4-7 to sht. 2
N.C.
WR VAR B HI To sht 1
WR VAR A HI to sht. 1
N.C.
WR ADC HI (8 MSB's) to sht 2
WR GPIB CONT. to sht. 3
WR BUS MAN. to sht. 3
WRITE LO BYTE
10D
74LS138
WR THRES 0-3 to sht. 2
WR THRES 8,9 to sht. 2
WR VAR B LO to sht 1
WR VAR A LO to sht. 1
WR ADC SEL to sht. 2
WR ADC LO (4 LSB's) to sht. 2
WR PP DATA to sht. 3
WR BUS DATA to sht. 3
READ HI BYTE
11D
74LS138
RD GPIB CONT. to sht. 3
RD BUS MAN. to sht. 3
READ LO BYTE
10B
74LS138
RD ADC to sht. 2
RD GPIB ADRS to sht. 3
RD BUS DATA to sht. 3
MPU INTERFACE
DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS
TOLERANCE
DRAWN
DATE 11-4-80
CHECKED
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR
ENG. SERV.
DATE
DASH NO.
NUMBER
QTY
NEXT ASSEMBLY
GOULD biomation
TITLE SCHEMATIC
THRESHOLD/GPIB/RS232
SCALE —
SIZE D
PART NUMBER 0114-0171
REV AE
CODE K1C1 K500/K605
SHEET 5 OF 5



CONNECTOR	
WIRING CODE	
PIN	COLOR
1	WHT
2	BLK
3	BLK
4	RED

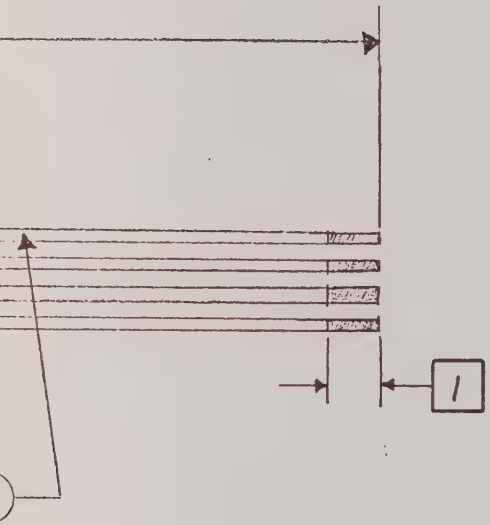
[2] TAG CABLE WITH ASSY. NO, DASH NO, AND REVISION LEVEL.

[1] STRIP AND TIN .25 INCH.

NOTES: UNLESS OTHERWISE SPECIFIED.

-10	0114-0475	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		REL PER ERN # 272	KA	JW 7/13/82	6-26-82
A	287	PROD REL PER ERN	[illegible]	JW 10/25/82	10/22/82
B	5270	ADD NOTE 2 & ITEM 6 4/14/86	RTM	DLW	4/15/86
BRC	5455	REVISED PER ECO 9/8/86	RTM	DLW	9/11/86



							1
−40	−30	−20	−10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

O NOT SCALE DRAWING

OVE ALL BURRS AND SHARP EDGES.
NSIONS ARE IN INCHES AND APPLY
ADDED FINISHES EXCEPT PAINT.
ACE ROUGHNESS

TOLERANCE

ISIONAL:	HOLE SIZE:
1 ANGLES	.0-.599 ± .003
.020 ± 1°	.600-.999 ± .004
± .010	1.000-1.499 ± .005

. SERV.	DATE
Gipson	11/12/82

	DATE
DRAWN K. ARNOLD	6-25-82
CHECKED J. Weldon	10-25-82
PROJ. ENG. Curt	7-19-82
MANUFACTURING P. [illegible]	11/12/82
QUALITY ASSUR [illegible]	11-12-82

GOULD biomation

TITLE Cable Assy
FDC POWER IN

SCALE	SIZE	PART NUMBER	REV
NONE	B	0114-0429	B

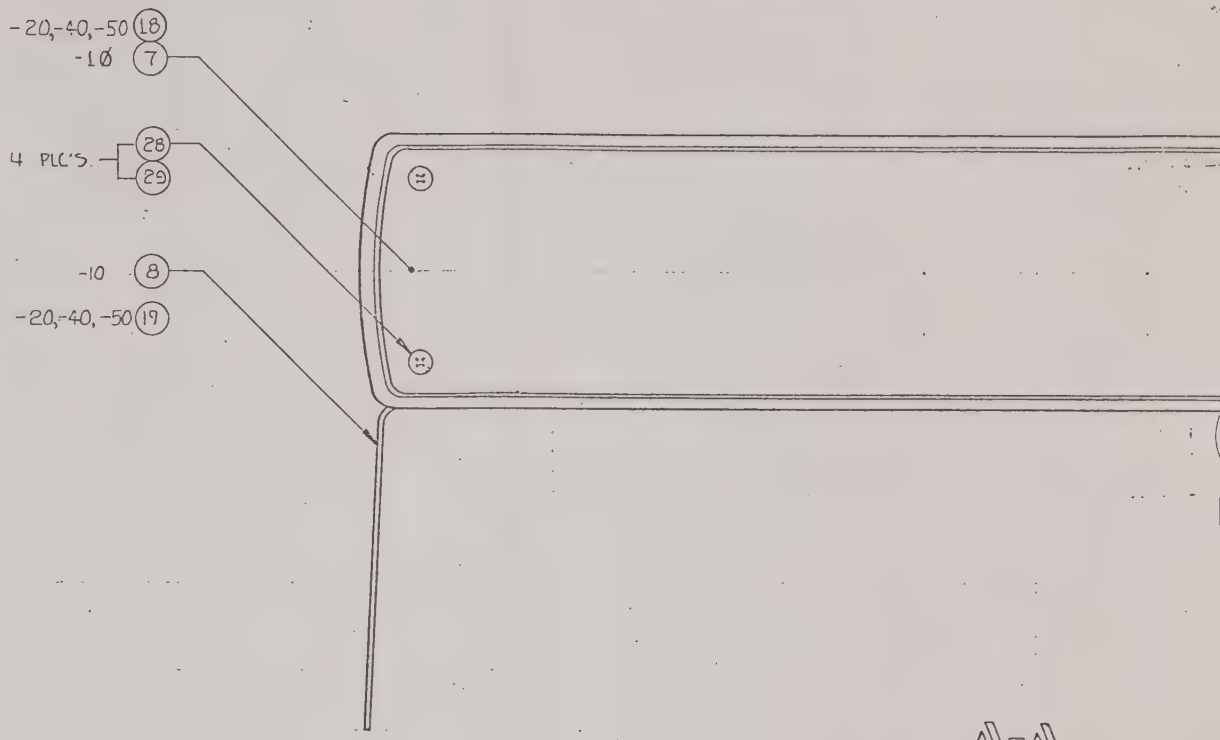
CODE SHEET 1 OF 1

BILL OF MATERIAL

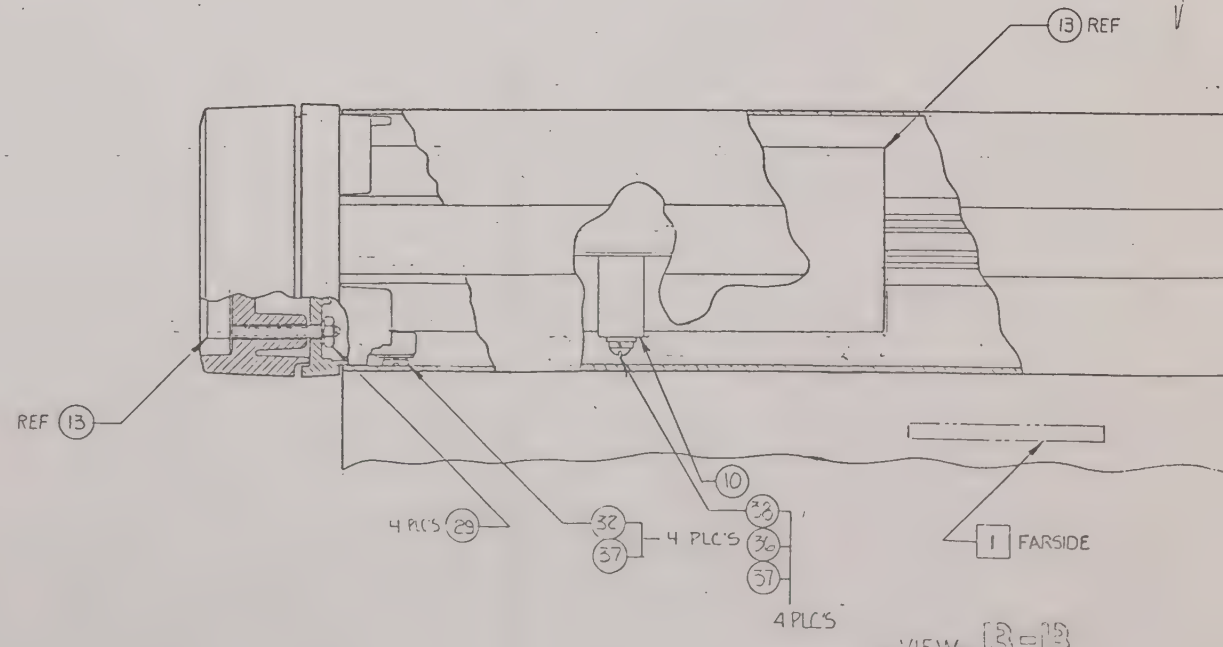
AS OF 10/30/87

0114-0429-10 ASSY,CBL,FDC PWR IN
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0114-0429	DWG,CBL ASSY,FDC POWER IN	0	EA	REF
1	6000-0024-10	CONN 4 PIN HOUSING	1	EA	
2	6000-0157-10	CONN PIN 24-18 AWG	4	EA	
3	7150-0018-09	WIRE,PVC,18 AWG,WHT	1	FT	
4	7150-0018-10	WIRE,PVC,18 AWG,BLK	1	FT	
5	7150-0018-02	WIRE;PVC,18 AWG,RED	1	FT	
6	7200-0039-10	TIE,MARKER,4"	1	EA	



VIEW A1-A1
ROTATED CLOCKWISE 90°

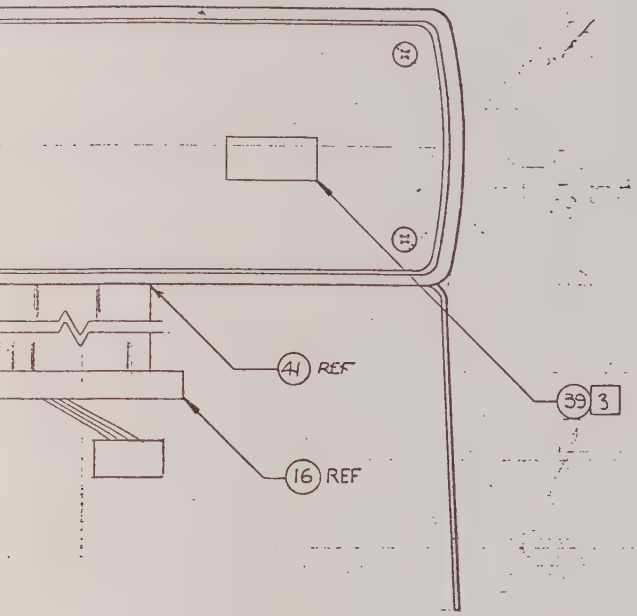


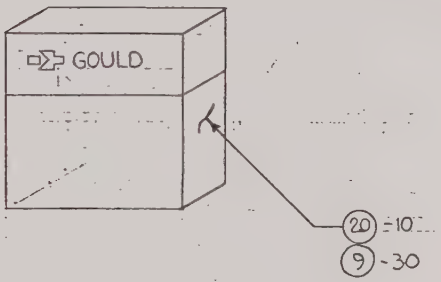
VIEW B1-B1
ROTATED COUNTER CLOCKWISE 90°

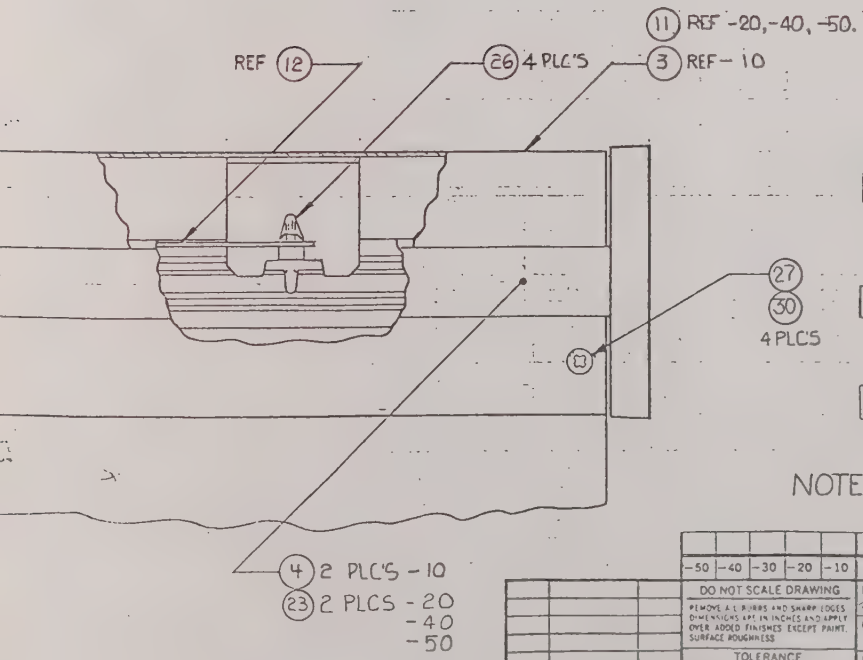
KLINGLER KVEL H

DWG. NO. 0114-0468 SH 1 REV W

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		REL PER ERN # 272	B.S	[illegible]	6/25/82
	B		PER ECO # 2718	George	[illegible]	9/16/82
	C	2728	REVISED PER ECO Nº	JWC	[illegible]	10-12-82
	C	-	PROD REL ERN # 287	JWC	[illegible]	10 12 82
	D	2766	REVISED PER ECO #	DGW	[illegible]	12/9/82
	E	3795	REVISED PER ECO Nº	JWC	DGW	10-12 83
	F	3767	REV'D PER ECO #	STM	DGW	9-13-83
	G	3980	REV'D PER ECO#	STM	DGW	10-28-83
	H	4015	REVISED PER ECO Nº	JWC	DGW	12-6/83
	J	4097	REVISED PER ECO Nº	JWC	DGW STM	12/7/83
	K	4125	REVISED PER ECO Nº	JWC	DGW STM	12/7/83
	L	4149	REVISED PER ECO	JWC	DGW STM	12/7/83
	M	4202	PER ECO 4202	Karen	DGW [illegible]	1/29/84
	N	4481	REVISED PER ECO	JWC	DGW JMS	9/16/84
	P	4604	PER ECO 7-3-84	George	DGW JMS	7/29/84
	Q	4792	REVISED PER ECO 11-21-84	SAR	DGW	11/20/84
	R	4937	REV L/M PER ECO 4-3-85	SAR	DGW	
	S	5098	REV PER ECO 11/13/85	RTM	DGW	11/13/85
	T	5144	REV. L/M PER ECO 11/13/85	RTM	DGW	11/13/85
	U	5172	REV'D BOM ONLY. 2/6/85	RTM	DGW	4/7/86
	V	5418	REVISED PER ECO 11/14/86	MM	DGW	12/5/86
	W	5850	REVISED PER ECO 11/4/87	MM	DGW	11/10/87







3 TYPE ASSY NO. 0114-0468 APPROPRIATE DASH NO, CURRENT REV LEVEL, AND SERIAL NO.

2 VIEW B-B SHOWS TEAC DRIVES. OTHER APPROVED DRIVES MAY BE USED. BOTH DRIVES MUST BE MFG'D BY THE SAME VENDOR.

1 TYPE ASSY NO. 0114-0468 APPROPIATE DASH Nº, CURRENT REVISION LETTER AND SERIAL NO.

NOTES: UNLESS OTHERWISE SPECIFIED.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
-40	A14548	1
-20	0120-0002	1
-10	[illegible]	1

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X = 1 ANGLES; XX = .020 ± 1°; XXX = .010

HOLE SIZE: 0.599 ± .003; 600.599 ± .004; 1.000.1.499 ± .005

ENG SERV. R. Gipson DATE [illegible]

DRAWN B. [illegible] DATE 6/21/82

CHECKED R. Gipson 11/12/82

PROJ. ENG. Curt 6/25/82

MANUFACTURING [illegible] 11/12/82

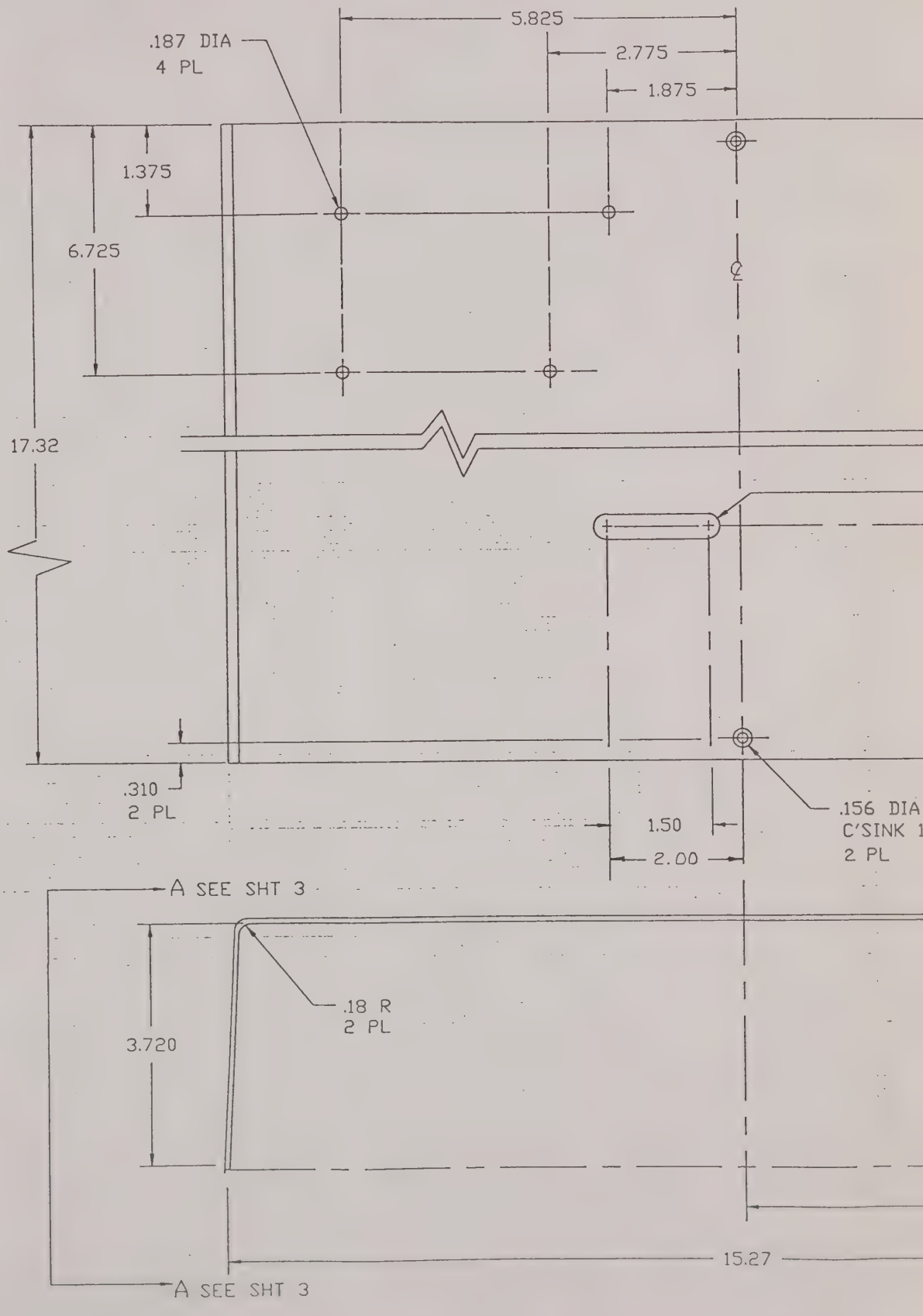
QUALITY ASSUR [illegible]

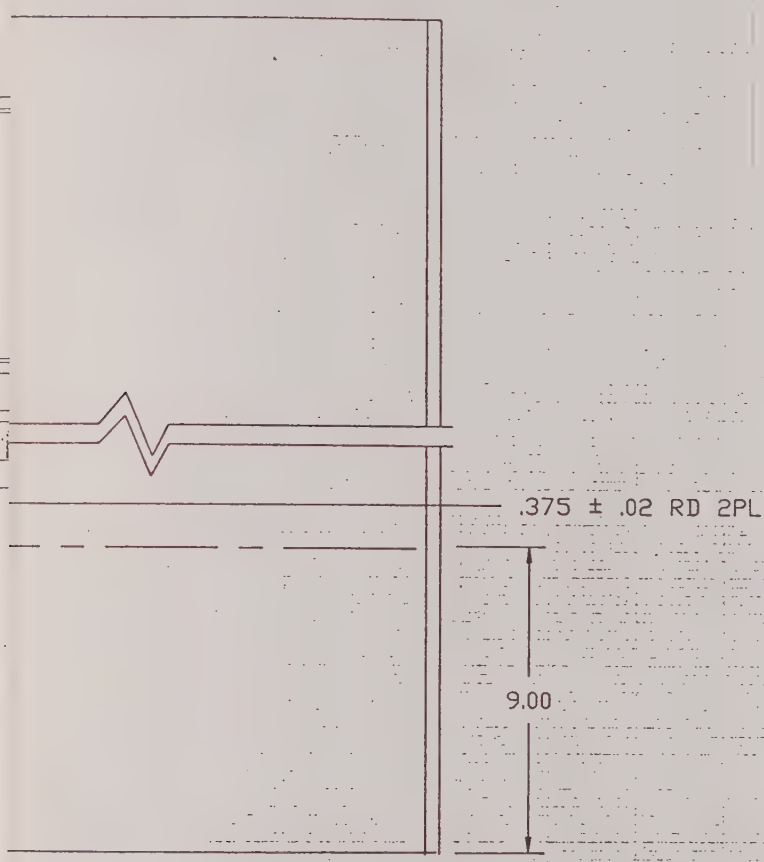
GOULD biomation

TITLE TOP ASSY, FLOPPY DISK HOUSING.

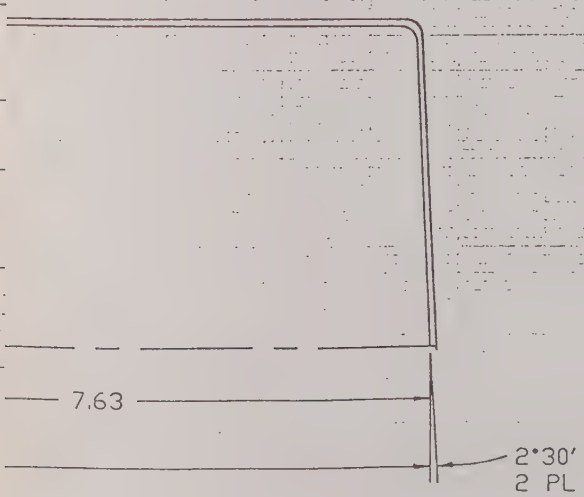
SCALE 1/1 SIZE D PART NUMBER 0114-0468 REV W.

CODE SHEET 1 OF 2


5.825
2.775
1.875
.187 DIA
4 PL
1.375
6.725
17.32
.310
2 PL
1.50
2.00
.156 DIA
C'SINK
2 PL
A SEE SHT 3
.18 R
2 PL
3.720
15.27
A SEE SHT 3



0° X .281ø



FILE NAME: COVER

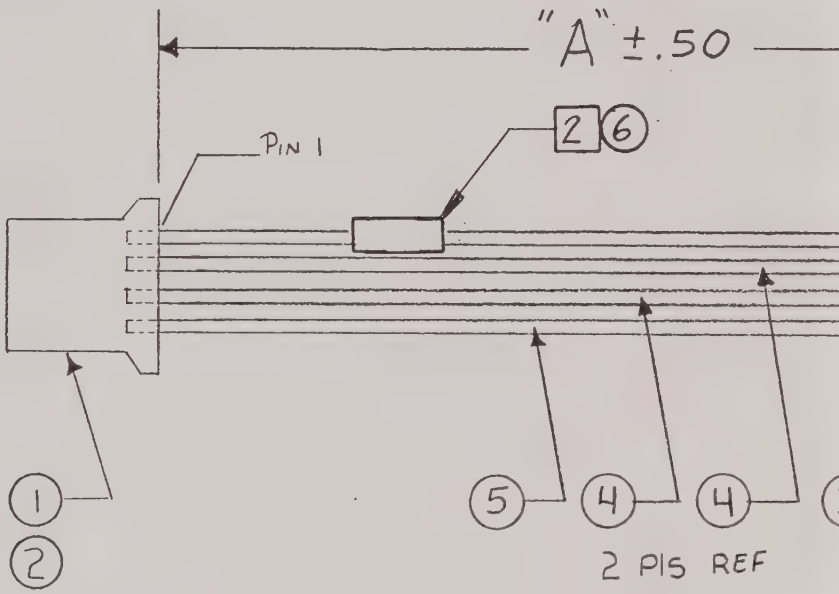
SIZE		DWG. NO.	REV.
D	GOULD	0121-0468	50
		SHEET 2 OF 2	

BILL OF MATERIAL

AS OF 10/30/87

0114-0468-40 ASSY,TOP,FLPY DSK HOUSING K450
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0697	DWG, DISK DRIVE JUMPER CONF.	0	EA	REF
0	D0114-0468	DWG,ASSY,FLOPPY DISK HOUSING	0	EA	REF
10	0114-0441-10	BRACKET,SUPPORT,FLOPPY DISK	1	EA	
11	0114-0466-30	COVER,TOP,K205	1	EA	
12	0121-0090-40	ASSY,STORAGE CONTROLLER,K450B	1	EA	
13	7500-0003-10	FLOPPY DISK DR 5" 1/2 HT	2	EA	
14	0114-0470-40	PANEL,FRONT,K205	1	EA	
15	0121-0037-20	ASSY,CBL,FDC TO DISK,DOUBLE DR	1	EA	
16	0114-0482-10	ASSY,CBL,K101 TO FDC SIGNALS	1	EA	
18	0117-0169-30	PANEL,REAR,DOS,K101,K102,K105	1	EA	
19	0121-0468-10	COVER,DUAL DISK K450B	1	EA	
21	0114-0485-10	ASSY,GROUND HARNESS,K101,K102	1	EA	
22	0114-0462-30	BEZEL,FRONT,K205	1	EA	
23	0114-0465-30	SIDE RAIL,K205	2	EA	
24	0114-0463-30	BEZEL,REAR,K205	2	EA	
25	7000-0334-10	HDWR "U" SPEED NUT FSTNR	4	EA	
26	7000-0461-10	HDWR PCB PLASTIC SPRT	6	EA	
27	7021-2632-12	SCR,X,FH 100,6-32 X 3/8,SS	8	EA	
28	7011-1632-16	SCR,X,PH,6-32 X 1/2,STZN	5	EA	
29	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	8	EA	
30	7072-1632-00	HEX NUT,NYLON LCKING #6	4	EA	
31	7012-1600-20	SCREW,X.PH,6-32 X .625	8	EA	
32	7000-0463-14	SCR,X,PH,3 X 14MM STZN	4	EA	
35	7086-1006-00	WSHR,EXT TOOTH LOCK,#6,STZN	1	EA	
36	7000-0463-08	SCREW 3MM X 8MM	4	EA	
37	7082-1004-00	WSHR,FLAT,#4,LP,STZN	8	EA	
38	7085-1004-00	WSHR,INT TOOTH LOCK,#4,STZN	4	EA	
40	7200-0044-10	GROMMET,FLEX,SPGS-2,ROLL	0	FT	



CONNECTOR	
WIRING CODE	
PIN	COLOR
1	WHT
2	BLK
3	BLK
4	RED

2 TAG WITH ASSY. NO., DASH NO., & REVISION LEVEL.

1 STRIP AND TIN .25 INCH.

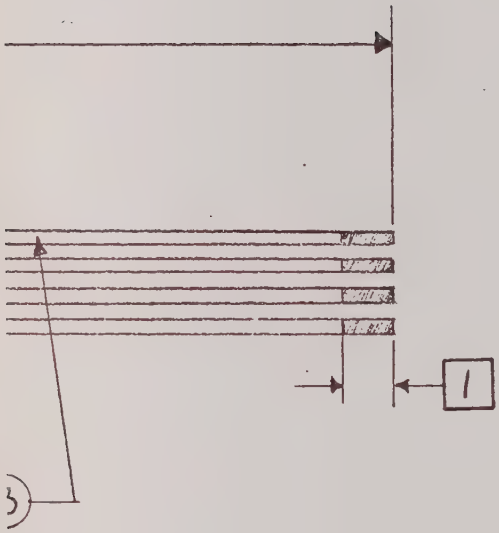
NOTE: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-20	0121-0090-20	1
-10	0121-0090-20	1
-20	0121-0090-10	1
-10	0114-0475	2

DWG. NO. 0114-0481 | SH 1 | REV. C

REVISIONS

REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		REL PER ERN # 272	KA	7/13/82	6-26-82
A	287	PROD REL PER ERN	[illegible]	JW	10/25/82
B	5254	ADD DASH 20 4/14/86	RTM	DGW	4/15/86
C	5270	ADD ITEM 6 & NOTE 2 4/14/86	RTM	DGW	4/15/86
CRC	5455	REVISED PER ECO 9/8/86	RTM	DGW	9/11/86



DASH NO.	"A" DIM.
-10	13.00 IN.
-20	6.50 IN.

								1
0	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

MOVE ALL BURRS AND SHARP EDGES.
IENSIONS ARE IN INCHES AND APPLY
R ADDED FINISHES EXCEPT PAINT.
RFACE ROUGHNESS

TOLERANCE

ENSIONAL:	HOLE SIZE:
.1 ANGLES	.0-.599 ± .003
± .020 ± 1°	.600-.999 ± .004
± .010	1.000-1.499 ± .005

G. SERV.	DATE
Gipson	11/12/82

	DATE
DRAWN K. ARNOLD	6-4-82
CHECKED J. Weldon	10/25/82
PROJ. ENG. Curt	7-19-82
MANUFACTURING P. Strassman	11/12/82
QUALITY ASSUR [illegible]	11-12-82

GOULD biomation

TITLE Cable Assy Power FDC to Floppy

SCALE	SIZE	PART NUMBER	REV
NONE	B	0114-0481	C.

CODE | SHEET 1 OF 1

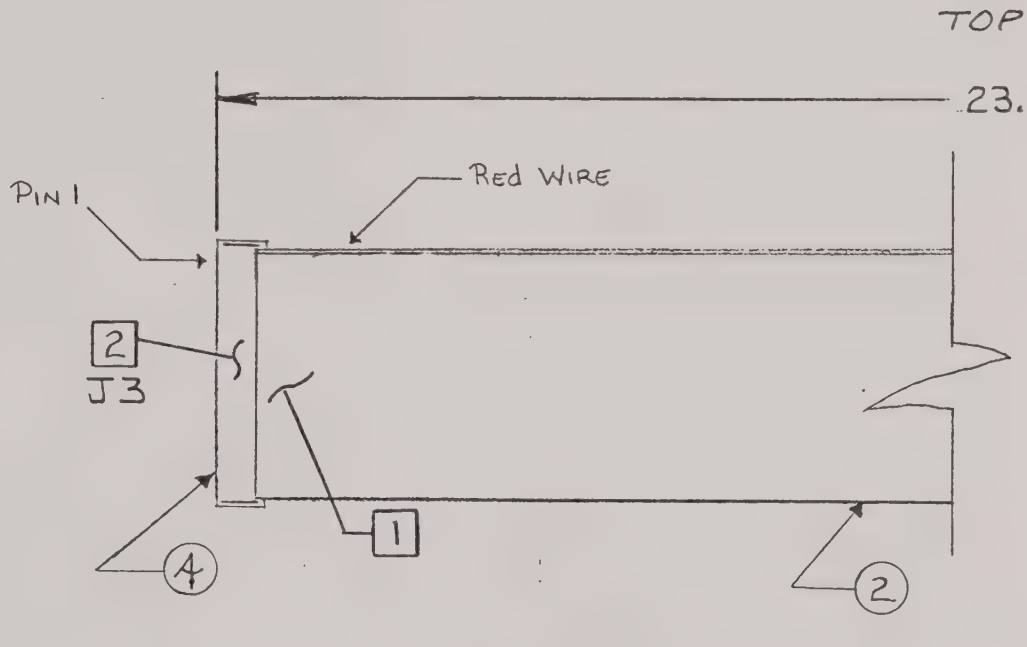
BILL OF MATERIAL

AS OF 10/30/87

0114-0481-20 ASSY,CBL,PWR,FDC TO FLOPPY DR.
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0114-0481	DWG,CBL ASSY,PWR FDC TO FLOPPY	0	EA	REF
1	6100-0062-10	SKT 4 PIN	1	EA	
2	6000-0185-10	CONN SKT 22-18 AWG	4	EA	
3	7150-0018-09	WIRE,PVC,18 AWG,WHT	1	FT	
4	7150-0018-10	WIRE,PVC,18 AWG,BLK	1	FT	
5	7150-0018-02	WIRE,PVC,18 AWG,RED	1	FT	
6	7200-0039-10	TIE,MARKER,4"	1	EA	

TOP V



2. STAMP CONN. DESIGNATION USING CONTRASTING INDELIBLE INK.

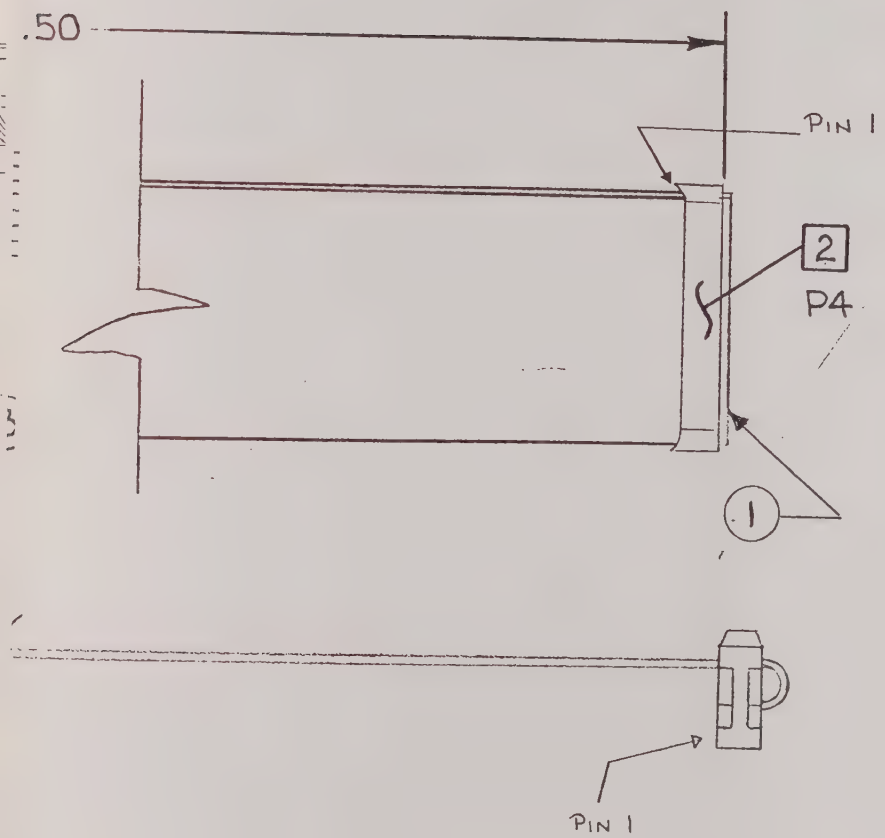
1. STAMP WITH PART Nº, DASH Nº AND REV. LEVEL APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-10	0114-0468	1

DWG. NO. 0114-0482 | SH 1 | REV. C

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		REL PER ERN # 272	KA	JW	9/25/82
B	2749	REVISED PER ECO #	[illegible]	JW	10/12/82
B	287	PROD REL PER ERN	JWC	JW	10/25/82
BRC	4634	PER ECO	George	DGW JMC	7/11/84
C	5454	REVISED PER ECO # 9/16	DGW	RTM	9/18/86



0								1
0	−40	−30	−20	−10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

MOVE ALL BURRS AND SHARP EDGES. MENSIONS ARE IN INCHES AND APPLY ER ADDED FINISHES EXCEPT PAINT. RFACE ROUGHNESS

TOLERANCE

ENSIONAL: ± .1 ± .020 ± .010 ANGLES ± 1°

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

IG. SERV. Gipson DATE 11/12/82

	DATE
DRAWN K. Arnold	6-4-82
CHECKED J Weldon	10/25/82
PROJ. ENG. Curt	7-19-82
MANUFACTURING P. [illegible]	11/12/82
QUALITY ASSUR [illegible]	11-12-82

GOULD biomation

TITLE Cable Assy Signals K101 to FDC

SCALE	SIZE	PART NUMBER	REV
NONE	B	0114-0482	C

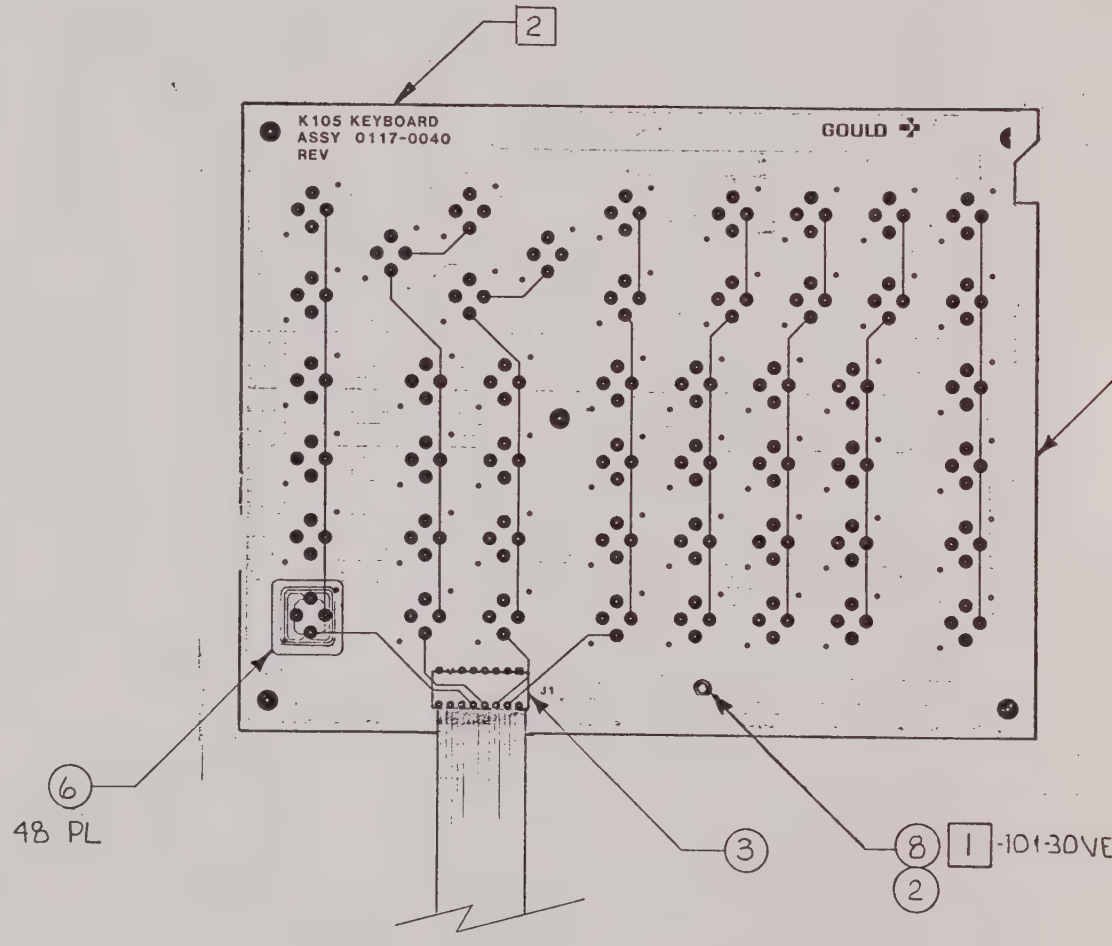
CODE | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0114-0482-10 ASSY,CBL,K101 TO FDC SIGNALS
MODEL: K101/K102

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0114-0482	DWG,ASSY,CBL,SIGS K101 TO FDC	0	EA	REF
1	6000-0391-10	CONN 34PIN W/ STRAIN REL	1	EA	
2	7100-0106-10	CBL,RIBBON,34 COND	2	FT	
2	7100-0111-10	CBL,FLAT,34 COND	2	FT	
3	7200-0048-10	CABLE MARKER	1	EA	
4	6000-0391-20	CONN 34PIN W/O STRAIN REL	1	EA	



5. DO NOT USE ROSIN BASED FLUX.
USE WATER SOLUABLE FLUX ONLY.

[4] APPLY A SMALL DROP OF LOCTITE BLACK MAX TO EACH KEYTOP BEFORE ATTACHING TO SWITCHS.

3 TEMPLATE TO BE USED DURING SOLDERING TO INSURE FLUSH MOUNTING OF SWITCHS TO PCB.

[2] MARK WITH ASSY DASH NO. AND REV LEVEL APPROX WHERE SHOWN USING CONTRASTING INDELIBLE INK.

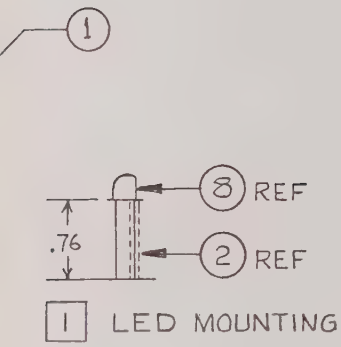
[1] SLEEVE FLAT SIDE (CATHODE) OF ITEM 8. GOES TO SQUARE PAD ON CIRCUIT BOARD, -101-30 VERSION ONLY.

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.
-
-30
-20
-10

KLINGLER K-VEL H

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN 316	STM		2-3-83
	51	3695	REV'D PER ECO #	MW	DGW	4/6/83
	52	3739	REV'D PER ECO #	MW	DGW	5/3/83
	A	3957	PROD REL PER ECO	JWD	DGW	9/16/83
	B	4220	PER ECO	K.R	DGW JMS	1/17/84
	C	4896	ROLL REV PER ECO 2-22-85	SAR	DGW	3/4/85
	D	5109	REVISE PER ECO # 11-2-85	DGW	RTM	11/7/85
	E	5520	REVISED PER ECO 12/16/86	MM	DGW	12/18/86
	E-RC	5779	REVISED PER ECO 8/6/87	MM	RTM	8/18/87



RSION ONLY

DWG. NO. 0117-0040 SH 1 REV E

0117-0040 182

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

NUMBER	QTY
117 0008	1
120-0008	1
117-0008	1

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES XX ± .020 ± 1° XXX ± .010

HOLE SIZE: 0 599 ± .003 600 999 ± .004 1 000 1 499 ± .005

ENG. SERV. R. Gipson DATE 2/18/83

		DATE
DRAWN	J.W. CARROLL	6-4-82
CHECKED	R. Wood	2/13/83
PROJ. ENG.	[signature]	2-18-83
MANUFACTURING	[signature]	2-18-83
QUALITY ASSUR		

GOULD biomation

TITLE ASSY —KEYBOARD

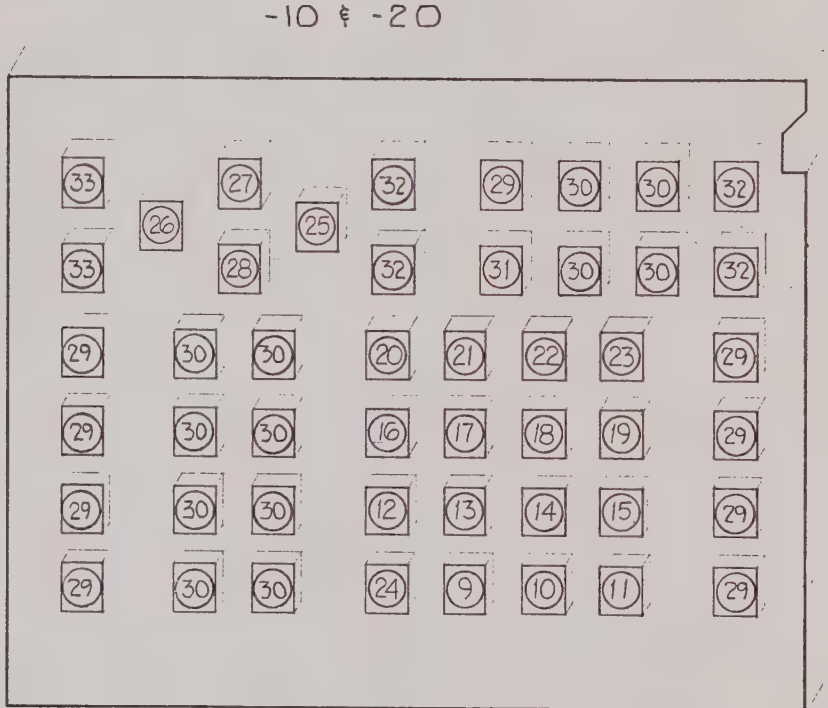
SCALE	SIZE	PART NUMBER	REV
1:1	C	0117-0040	E

CODE K105 SHEET 1 OF 2

4 3

D C B A

-10 & -20



(1) REF.

DASH NO.

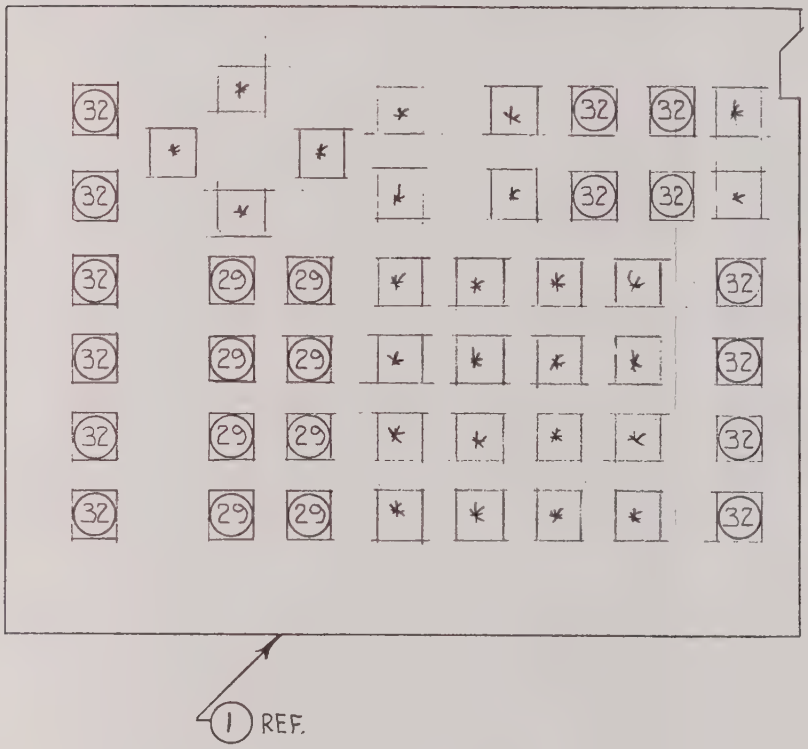
KLINGLER K-VEL H

4 3

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	-		SEE SH.1	George		

-30

*(ALL REF. DESG. NOT SHOWN SAME AS -10 & -20)



DWG. NO. 0117-0040 SH 2 REV. E

0117-0040 282

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: .0 599 ± .003; .600 999 ± .004; 1.000 1.499 ± .005

DRAWN	George Colindo	DATE 12-7-82
CHECKED	R. Wood	2-15-83
PROJ. ENG.	[illegible]	2-18-83
MANUFACTURING	[illegible]	2-18-83
QUALITY ASSUR		

GOULD biomation

TITLE ASSEMBLY KEYBOARD

SCALE	SIZE	PART NUMBER	REV
	C	0117-0040	E

CODE K105 SHEET 2 OF 2

NUMBER	QTY
EXT ASSEMBLY	

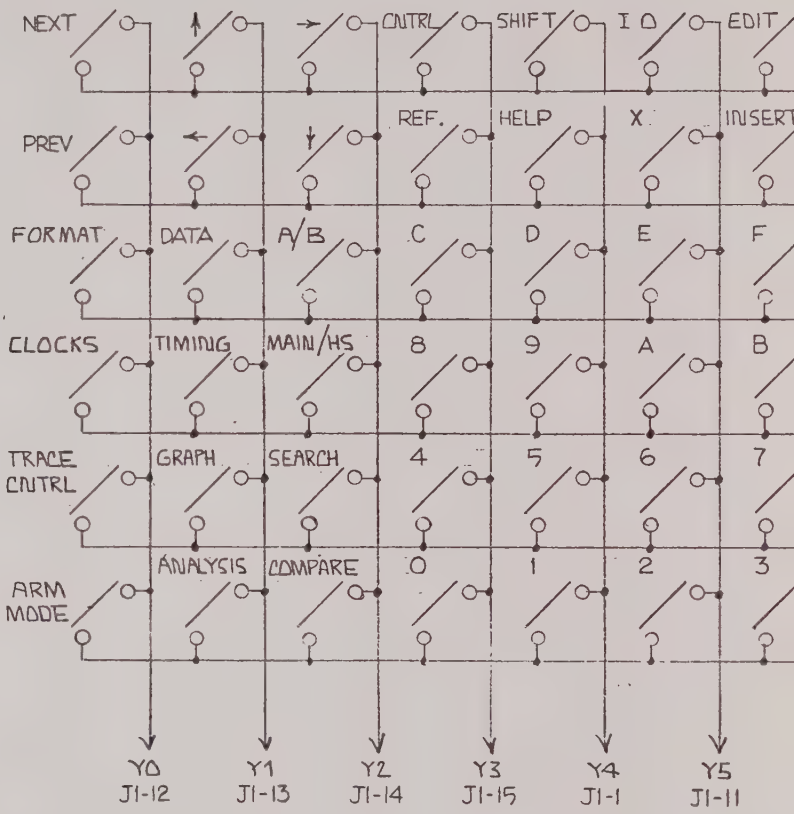
ENG. SERV. R. Gipson DATE 2/18/83

BILL OF MATERIAL

AS OF 10/30/87

0117-0040-30 ASSY,KEYBOARD,K115
MODEL: K105

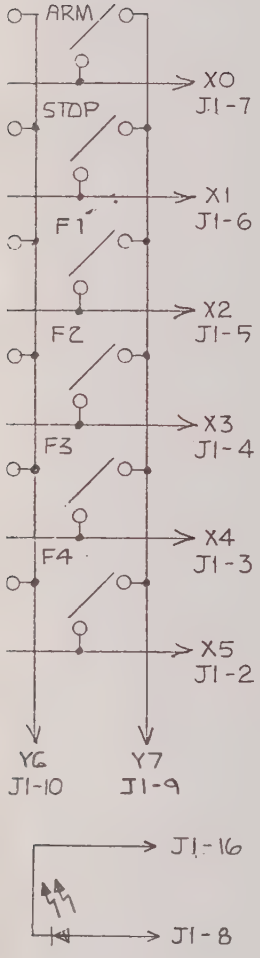
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0040	DWG,ASSY,KEYBOARD	0	EA	REF
0	C0117-0041	DWG,SCHEM,KEYBOARD	0	EA	REF
1	0117-0042-10	FAB, KEYBOARD	1	EA	
2	7200-0151-10	SLEEVING,24 AWG	0	FT	
3	0112-0204-10	ASSY,CBL,KB TO FP	1	EA	
4	8200-0039-10	ADHESIVE, LOCITITE BLACK MAX	0	EA	
6	6600-0118-10	SW KYBD. LO-PROFILE	48	EA	
8	6400-0039-10	LED 1 AMP RED	1	EA	CR1
9	0112-0079-01	KEYTOP,WHITE,'1',K100D	1	EA	"1"
10	0112-0079-02	KEYTOP,WHITE,'2',K100D	1	EA	"2"
11	0112-0079-03	KEYTOP,WHITE,'3',K100D	1	EA	"3"
12	0112-0079-04	KEYTOP,WHITE,'4',K100D	1	EA	"4"
13	0112-0079-05	KEYTOP,WHITE,'5',K100D	1	EA	"5"
14	0112-0079-06	KEYTOP,WHITE,'6',K100D	1	EA	"6"
15	0112-0079-07	KEYTOP,WHITE,'7',K100D	1	EA	"7"
16	0112-0079-08	KEYTOP,WHITE,'8',K100D	1	EA	"8"
17	0112-0079-09	KEYTOP,WHITE,'9',K100D	1	EA	"9"
18	0112-0079-10	KEYTOP,WHITE,'A',K100D	1	EA	"A"
19	0112-0079-11	KEYTOP,WHITE,'B',K100D	1	EA	"B"
20	0112-0079-12	KEYTOP,WHITE,'C',K100D	1	EA	"C"
21	0112-0079-13	KEYTOP,WHITE,'D',K100D	1	EA	"D"
22	0112-0079-14	KEYTOP,WHITE,'E',K100D	1	EA	"E"
23	0112-0079-15	KEYTOP,WHITE,'F',K100D	1	EA	"F"
24	0112-0079-16	KEYTOP,WHITE,'0',K100D	1	EA	"0"
25	0112-0059-23	KEYTOP,BLUE,K100D	1	EA	">"
26	0112-0059-24	KEYTOP,K100D	1	EA	"<"
27	0112-0059-25	KEYTOP,BLUE,K100D	1	EA	"^"
28	0112-0059-26	KEYTOP,BLUE,K100D	1	EA	"v"
29	0112-0049-10	KEYTOP, (BLUE PLAIN) BUTTON	9	EA	
31	0112-0049-50	KEYTOP, (RED) BUTTON	1	EA	
32	0112-0049-40	KEYTOP, (GREY) BUTTON	18	EA	



10	21
DASH NO.	

KLINGLER K-VEL H

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	50		PILOT REL PER ERN #316	STM		2-3-83
	51	—	REV SKIPPED	mw		4-15-83
	52	3739	REV'D PER ECO	mw	DGW	5/3/83
	A	3957	PROD REL PER ECO N6	JWC	DGW	9/16/83
	B	4220	PER ECO	Karen	DGW Tms	1/17/84
	C	4896	CHG'D SWITCH TITLES 2-22-85	SAR	DGW	3/4/85
	D	5109	REVISED PER ECO # 11-2-85	DGW	RTM	11/7/85
	E	5520	REV ROLL ONLY 12-16-86	MM	DGW	12/16/86



DWG. NO. 0117-0041 SH. 1 REV. E

0117-0041

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1, XX ± .020, .XXX ± .010; ANGLES ± 1°

HOLE SIZE: 0 599 - 003, 600 999 - 004, 1.000-1.499 - .005

DRAWN		DATE	10/12/81
CHECKED	R. Wood		2-15-83
PROJ. ENG.			2-18-83
MANUFACTURING			2-15-83
QUALITY ASSUR			

GOULD biomation

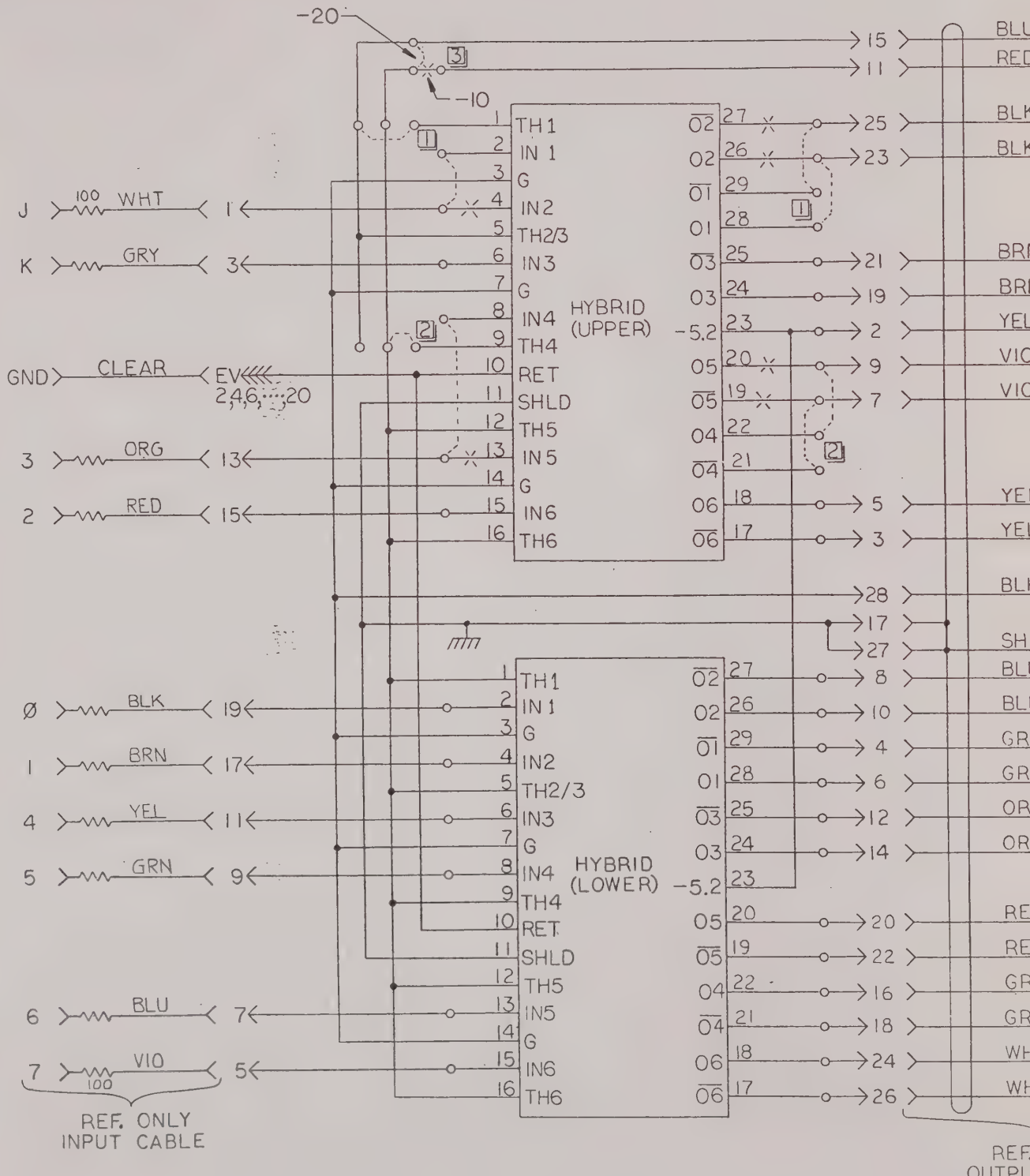
TITLE SCHEMATIC KEYBOARD, K105

SCALE	SIZE	PART NUMBER	REV
—	C	0117-0041	E

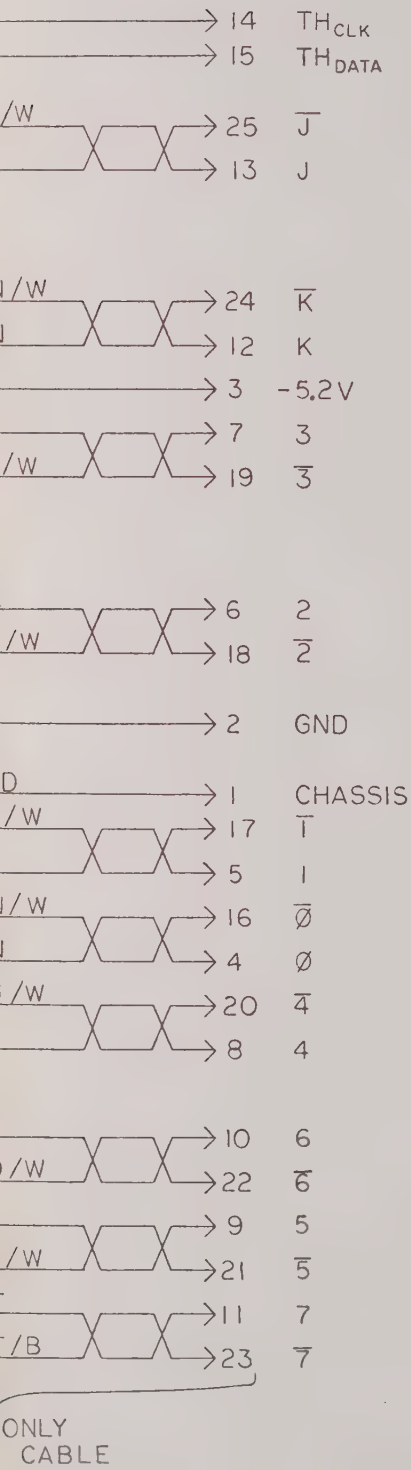
CODE KFRUSAL SHEET 1 OF 1

NUMBER	QTY
0117-0040	1
EXT ASSEMBLY	

ENG. SERV. R. Hixson DATE 2/18/83


-20
-10
3
1
2
HYBRID (UPPER)
TH1
IN 1
G
IN2
TH2/3
IN3
G
IN4
TH4
RET
SHLD
TH5
IN5
G
IN6
TH6
02
02
01
01
03
03
-5.2
05
05
04
04
06
06
HYBRID (LOWER)
J 100 WHT 1
K GRY 3
GND CLEAR EV 2,4,6,...,20
3 ORG 13
2 RED 15
Ø BLK 19
1 BRN 17
4 YEL 11
5 GRN 9
6 BLU 7
7 VIO 100 5
REF. ONLY INPUT CABLE
REF OUTPU
BLU
RED
BLK
BLK
BRN
BRN
YEL
VIO
VIO
YEL
YEL
BLK
SH
BLU
BLU
GRN
GRN
ORN
ORN
RED
RED
GRN
GRN
WHT
WHT

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SH. 1			



1. J OR K CHANNEL MAY BE REPAIRED WITH 3 CUTS AND 3 JUMPERS (J SHOWN).
2. Ø TO 7 MAY BE REPAIRED AS IN 1 BUT NOTE DIFFERENCE IN "TH" JUMPER (3 SHOWN).
3. PROBE MAY BE CONVERTED TO SINGLE THRESHOLD (K101 STYLE) WITH 1 CUT AND 1 JUMPER.
   - -10 JUMPER INSTALLED FOR K105
   - -20 JUMPER INSTALLED FOR K101/K102

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0 599 ± .003; 600 999 ± .004; 1 000 1 499 ± .005

DRAWN: J. Stinger — DATE: 4/26/83

CHECKED: R. Wood — 5/12/83

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD — Instruments Division, Santa Clara Operations

TITLE: SCHEMATIC - 100 MHZ PROBE POD PWB

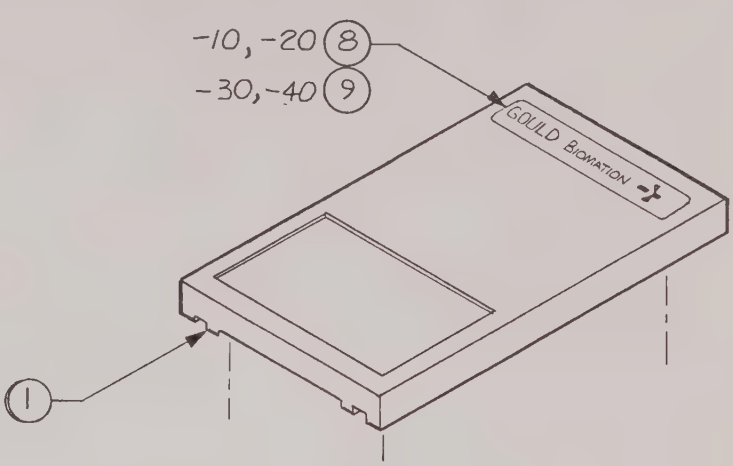
SCALE	SIZE	PART NUMBER	REV
	D	0117-0095	51

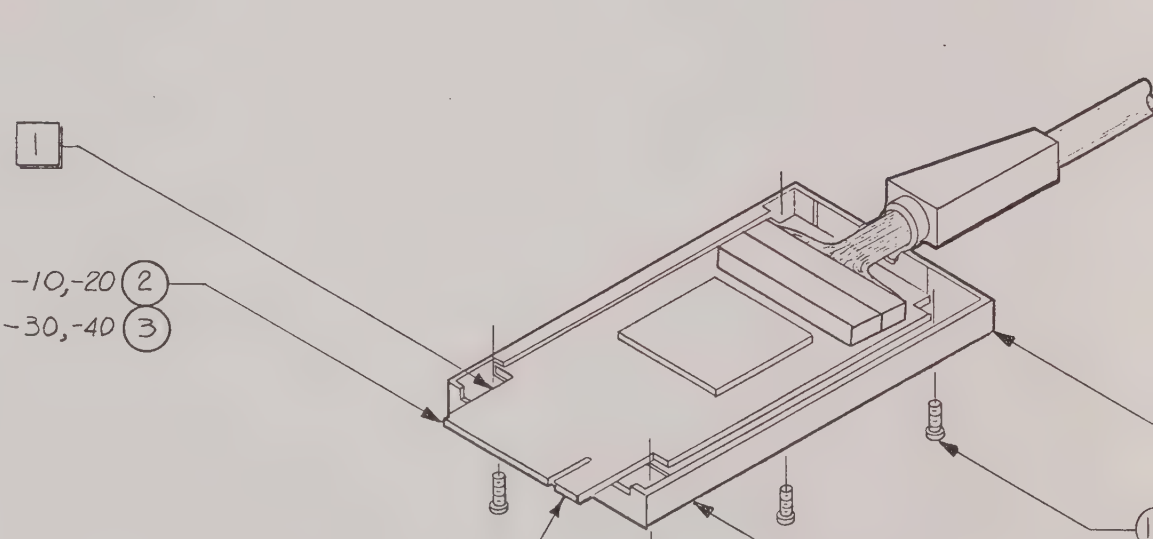
MODEL

SHEET 2 OF 3

DASH NO	NUMBER	QTY
	NEXT ASSEMBLY	

ENG. SERV. — DATE





3 MARK BOTTOM OF CASE LARGE RECTANGULAR RECESS WITH THE FOLLOWING: XXX XX XX XXXXX
MFG N° YEAR WEEK SERIAL N°
0117-0099-XX REV. X
DASH CURRENT REV. LEVEL

2 BAG AND TAG WITH P/N 0117-0099, DASH NO. AND REV. LEVEL.

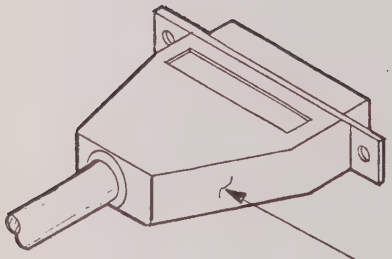
1 PIN 1 (FARSIDE).

NOTES: UNLESS OTHERWISE SPECIFIED

40
40
30
30
20
10
DASH NO.

KLINGLER K-VEL H

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	01		PROTOTYPE	STM		1-8-83
	50		PILOT REL PER ERN 335	STM		4-18-83
	51	3960	REVISED PER ECO #	DWC	DGW	8-24-83
	52	3749	REV'D PER ECO 3749	RTM	DGW 5/4	2/4/14



(4) -10, -30

(5) -20, -40

(6)

4 PL

USAGE CHART		
DASH	MODEL	LENGTH
10	K105	6'
20	K105	9'
30	K101	6'
40	K101	9'

DWG. NO. 0117-0099 | SH 1 | REV 52

0099-0110

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1
					0114-1092			1
					0114-1091			1
					0114-1062			1
					0114-1061			1
					0117-0174			1
					0117-0173			1

NUMBER | QTY

NEXT ASSEMBLY

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: .0 599 ± .003; 600-999 ± .004; 1 000-1 499 ± .005

ENG. SERV. R. Gipson — DATE 4/25/83

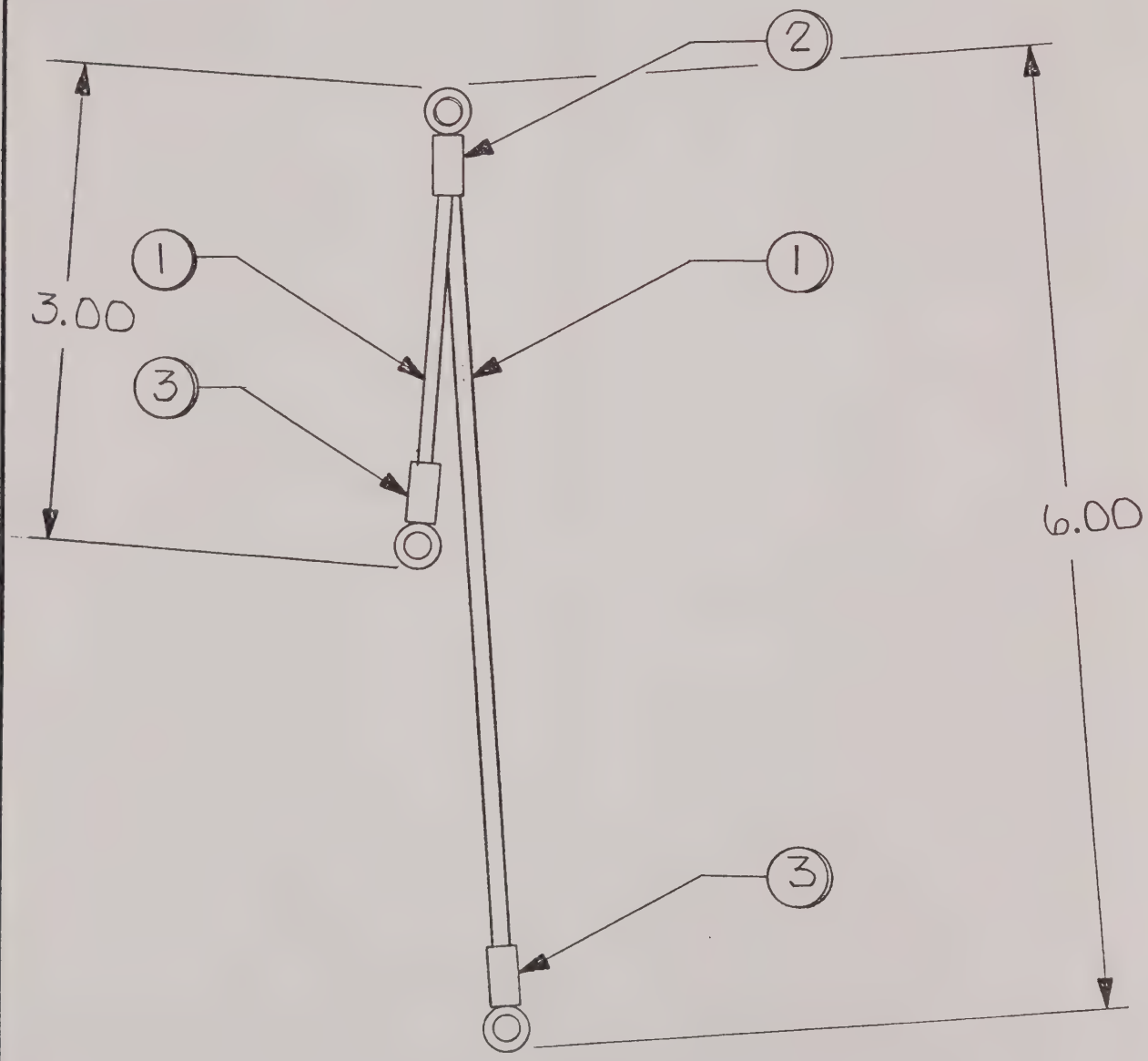
DRAWN	STM	DATE 1-8-83
CHECKED	R. Wood	4/19/83
PROJ. ENG.		5/12/83
MANUFACTURING		5-13-83
QUALITY ASSUR		5/12/83

GOULD biomation

TITLE: PROBE SUB ASSY

SCALE	SIZE	PART NUMBER	REV
NONE	C	0117-0099	52

CODE K105/K101 — SHEET 1 OF 1



2. BAG & TAG WITH P/N 0117-0133 DASH NO AND REV LEVEL.

1. DRAWING IS TO SCALE & MAY BE USED AS TEMPLATE

NOTES: UNLESS OTHERWISE SPECIFIED

10	0117-0003	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DWG. NO. 0117-0133 | SH 1 | REV. A

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
01		PROTOTYPE	STM		2-4-83
50		PILOT REL. PER ERN 322			2-13-83
51	3872	REVISED PER ECO №	JWC	DGW	7-7-83
A	3957	PROD. REL PER ECO#	STM	DGW	9-16-83

-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
							1

O NOT SCALE DRAWING

OVE ALL BURRS AND SHARP EDGES. ENSIONS ARE IN INCHES AND APPLY R ADDED FINISHES EXCEPT PAINT. FACE ROUGHNESS

TOLERANCE

NSIONAL: .1 ± .020 ± .010 ANGLES ± 1°

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

G. SERV. DATE 3/25/83

	DATE
DRAWN STM	2-4-83
CHECKED	2/28/83
PROJ. ENG.	3/23/83
MANUFACTURING	3-25-83
QUALITY ASSUR	3-25-3

GOULD biomation

TITLE CHASSIS GND CABLE

SCALE	SIZE	PART NUMBER	REV
1:1	B	0117-0133	A

CODE K105 | SHEET 1 OF 1

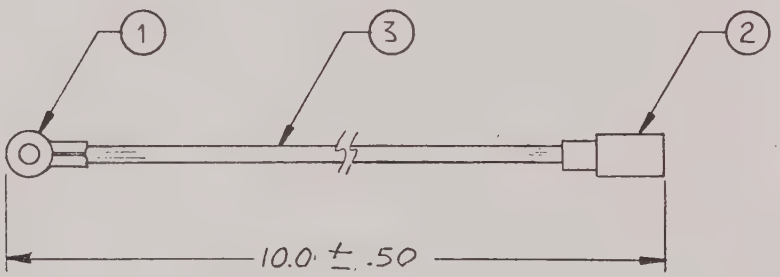
BILL OF MATERIAL

AS OF 10/30/87

0117-0133-10 CABLE,CHASSIS GROUND,K105
MODEL K105

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0117-0133	DWG,ASSY,CHASSIS GND CABLE	0	EA	REF
1	7150-0020-10	WIRE,PVC,20 AWG BLK	1	FT	
2	6200-0030-10	TERM RING TONGUE BLUE	1	EA	
3	6200-0025-10	TERM LUG RING #6 16-22AWG RED	2	EA	

ANGL.
± 1°



-03	-0
QTY PE	
UNLESS OTI DIMENSIONS TOLERANCE FRACTIONS =	
MATERIAL	5
FINISH	
DO N	

-10	0117-0715	
DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

DIETERICH POST REORDER NO. R4499

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	A	5110	PROD. REL PER ECO	RTM	DW	

D

C

B

A

NOTES: UNLESS OTHERWISE SPECIFIED

1. BAG & TAG WITH PART NO., DASH NO., AND REV LEVEL.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.

2 -01 R ASSY	PART NUMBER	DESCRIPTION	ITEM NO.

PARTS LIST

ERWISE SPECIFIED
ARE IN INCHES
S ARE:
DECIMALS ANGLES
.XX = / ±
.XXX = /

E L/M

OT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN Scott Rico	10-24-84
CHECKED R Mercer	
PROJ ENG	11/5/85
	11-7-85

GOULD Electronics

TITLE: ASSEMBLY, GROUND HARNESS

SIZE C | DWG NO. 0117-0626 | REV A

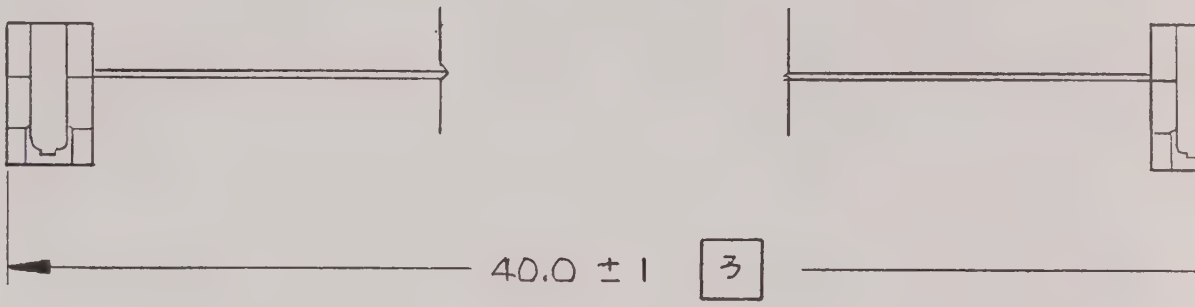
SCALE NONE | MODEL K115 | SHEET 1 OF 1

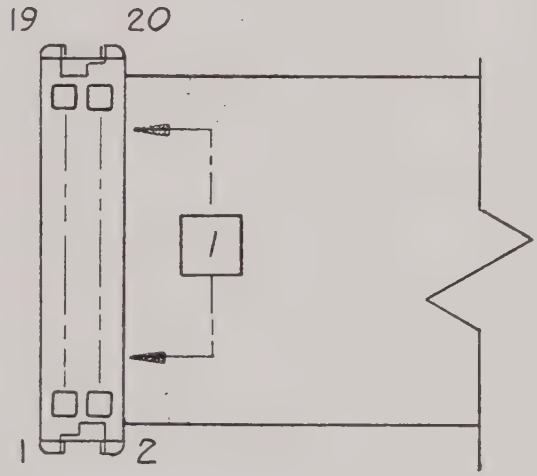
BILL OF MATERIAL

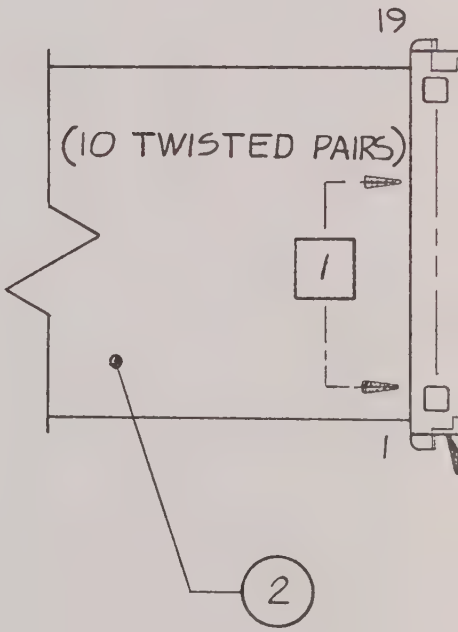
AS OF 10/30/87

0117-0626-10 ASSY,GND HARNESS,DOS/2
MODEL: K115

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0117-0626	DWG,ASSY,GND HARNESS	0	EA	REF
1	6200-0025-10	TERM LUG RING #6 16-22AWG RED	1	EA	
2	6200-0035-10	TERM DISC FEM .187TAB 18-22	1	EA	
3	7150-0022-10	WIRE,PVC,22 AWG,BLK	1	FT	







01	0120-0004	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DWG. NO. 0120-0043 | SH 1 | REV. 51

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4293	PILOT REL. PER ECO	RM	DLW	1/12/84
51	4468	REVISED PER ECO Nº	JWC	DGW JML	4/2/84
51RC	5455	REVISED PER ECO 9-9-86	Rickey	DLW	9/11/86

NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP CABLE WITH ASSY. NO., DASH NO. AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK. (2 PL)
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. CONNECTORS MUST BE INSTALLED ON FLAT PORTIONS OF CABLE.

								1
-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

MOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY FOR ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL:	HOLE SIZE:
.1 ANGLES ± .020 ± 1° ± .010	.0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

G. SERV.	DATE

	DATE
DRAWN RMerrey	1/4/83
CHECKED DLWRIGHT	1-12-84
PROJ. ENG. [signature]	1/10/84
MANUFACTURING [signature]	1/10/84
QUALITY ASSUR [signature]	1/10/84

GOULD biomation

TITLE ASSY., CABLE, PROBE TEST TO CLOCK BD.

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0043	51

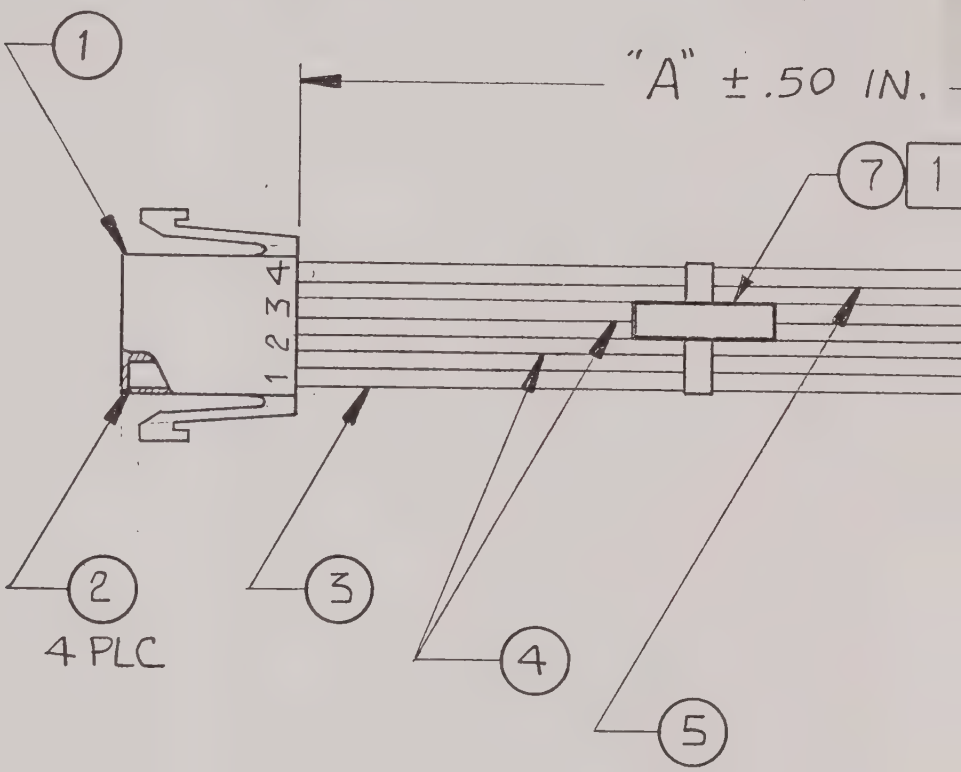
CODE K205 | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0120-0043-01 ASY CBL PROBE TEST TO CLK,K205
MODEL: K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0043	DWG,ASSY,CBL,PRB TST TO CLK BD	0	EA	REF
1	6000-0273-10	CONN 20 PIN SKT	2	EA	
2	7100-0009-10	CBL,FLAT,28 AWG,10PR,TW	3	FT	

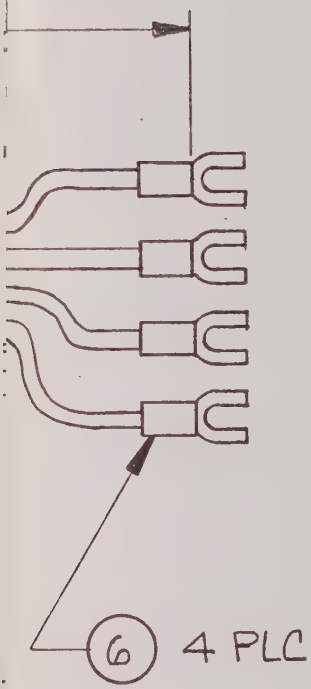


1 .STAMP PART NUMBER, DASH NUMBER AND REV LEVEL

-10	0120-0004	1
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DWG. NO. 0120-0145 SH 1 REV 54

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
50	4604	PROTOTYPE REL	SAR	DLW JMS	7/24/84
51	4800	REVISED PER ECO 12-5-84	SAR	DGW JMS	12/5/84
52	5274	ADD DASH 20 4-23-86	RTM	DLW	4/23/86
53	5429	REVISED PER ECO 8/12/86	RTM	DLW	8/12/86
54	5454	REVISED PER ECO 9-17-86	RTM	DLW	9/18/86



DASH NO.	"A" DIM
-10	15.00 IN.
-20	24.00 IN.

								1
-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM

DO NOT SCALE DRAWING

MOVE ALL BURRS AND SHARP EDGES. MENSIONS ARE IN INCHES AND APPLY ER ADDED FINISHES EXCEPT PAINT. RFACE ROUGHNESS

TOLERANCE

MENSIONAL:	HOLE SIZE:
± .1 ANGLES	.0-.599 ± .003
± .020 ± 1°	.600-.999 ± .004
X ± .010	1.000-1.499 ± .005

NG. SERV.	DATE

DRAWN	S. Rico	4-23-84
CHECKED	[signature]	7/24/84
PROJ. ENG.	[signature]	7/24/84
MANUFACTURING		
QUALITY ASSUR		

GOULD

TITLE ASSEMBLY, DOS-PWR HARNESS

SCALE	SIZE	PART NUMBER	REV
NONE	B	0120-0145	54

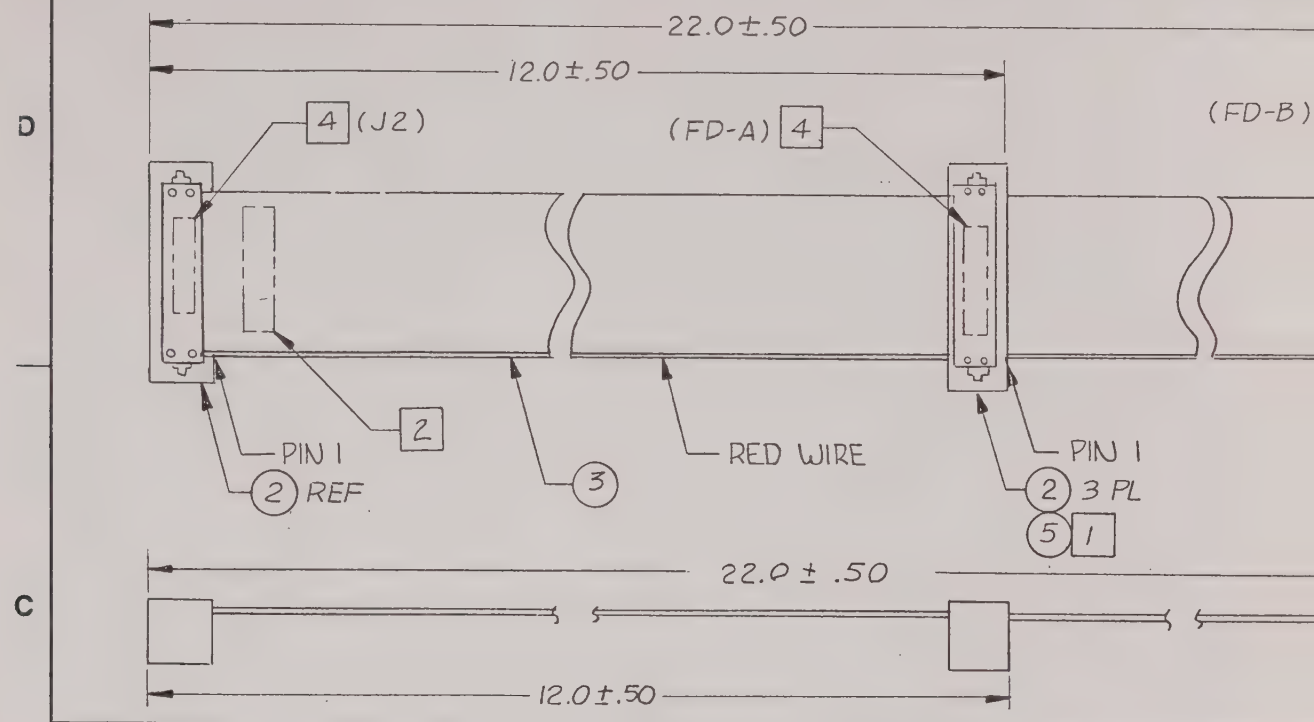
CODE | SHEET 1 OF 1

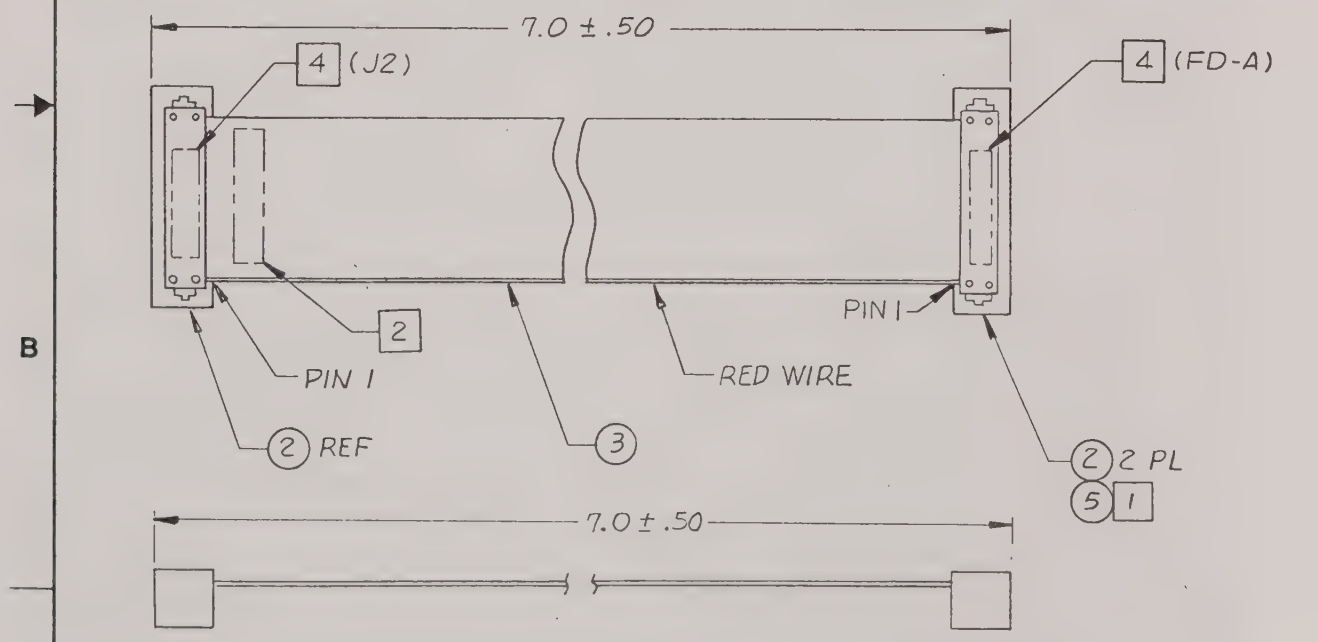
BILL OF MATERIAL

AS OF 10/30/87

0120-0145-20 ASSY,HARNESS,DOS-PWR,K450,1 DD
MODEL:

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0120-0145	DWG,ASSY,DOS,PWR HARNESS	0	EA	REF
1	6000-0023-10	CONN 4 PIN SKT HOUSING	1	EA	
1	6100-0062-10	SKT 4 PIN	1	EA	
2	6000-0185-10	CONN SKT 22-18 AWG	4	EA	
3	7150-0018-09	WIRE,PVC,18 AWG,WHT	2	FT	
4	7150-0018-10	WIRE,PVC,18 AWG,BLK	4	FT	
5	7150-0018-02	WIRE,PVC,18 AWG,RED	2	FT	
6	6200-0069-10	TERM LUG SNAP SPADE 22G INSLT	4	EA	
7	7200-0039-10	TIE,MARKER,4"	1	EA	





3 CUT CONDUCTORS 10 THRU 12 AND 14 THRU 16 LOOSE FROM STRIP, ROTATE 180° AND CRIMP INTO CONN ITEM 2 AS SHOWN (-20 ONLY).

4 STAMP CONN. DESIGNAT CONTRASTING INDELIBLE

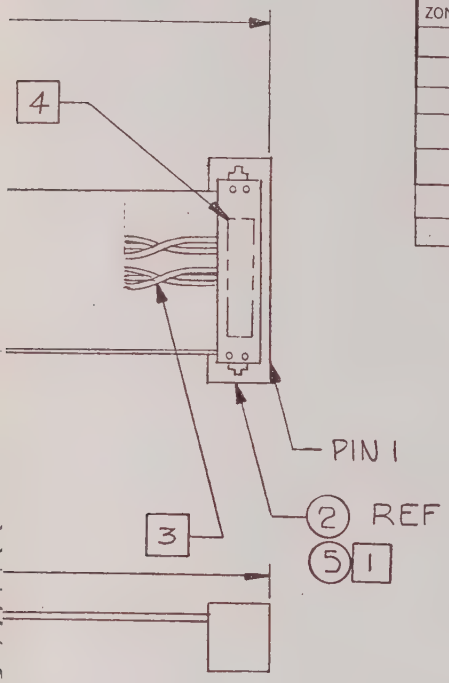
2 STAMP PART NO. 0121-0037 DASH NO. AND REV. LEVEL APPROX. AS SHOWN. USING CONTRASTING INDELIBLE INK.

1 KEY INSERTED BETWEEN LOCATIONS 4 AND 6

NOTES: UNLESS OTHERWISE SPECIFIED

20
10
DASH NO.

KLINGLER K-VEL H



REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A	5265	PROD REL PER ECO 4/24/86	RTM	DGW	4/27/86
	B	5356	REVISED PER ECO 6/30/86	RTM	DGW	7/1/86
	C	5454	REVISED PER ECO 9-17-86	RTM	DGW	9/18/86
	D	5459	REVISED PER ECO 11-20-86	MM	DGW	12/5/86
	D-RC	5509	REVISED PER ECO 12-2-86	MM	DGW	12/5/86
	E	5562	REVISED PER ECO 1-29-87	MM	DGW	2/2/87
	E-RC	5777	REVISED PER ECO 8-7-87	MM	RTM	8/8/87

-20

-10

0121-0037
p. 1 of 2

DWG. NO. 0121-0037 SH 1 REV. E

ON USING
INK.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES XX ± .020 ± 1° XXX ± .010

HOLE SIZE 0.599 - .003 .600 .999 ± .004 1.000 1.499 - .005

NUMBER	QTY
NEXT ASSEMBLY	

ENG. SERV. DATE

DRAWN Revised By RTM DATE 4/24/86

CHECKED DGWRIGHT 4/27/86

PROJ. ENG.

MANUFACTURING

QUALITY ASSUR

GOULD biomation

TITLE CABLE ASSY I/O TO FLOPPY

SCALE	SIZE	PART NUMBER	REV
NONE	C	0121-0037	E

CODE K450 SHEET 1 OF 2

-10

WIRE LIST	
J2	FD-A
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10
11	11
12	12
13	13
14	14
15	15
16	16
17	17
18	18
19	19
20	20
21	21
22	22
23	23
24	24
25	25
26	26
27	27
28	28
29	29
30	30
31	31
32	32
33	33
34	34

-20

WIRE LIST [3]			
J2	FD-A	FD-B	COMMENTS
1	1	1	
2	2	2	
3	3	3	
4	4	4	
5	5	5	
6	6	6	
7	7	7	
8	8	8	
9	9	9	
10	10	12	[3]
11	11	11	
12	12	10	[3]
13	13	13	
14	14	16	[3]
15	15	15	
16	16	14	[3]
17	17	17	
18	18	18	
19	19	19	
20	20	20	
21	21	21	
22	22	22	
23	23	23	
24	24	24	
25	25	25	
26	26	26	
27	27	27	
28	28	28	
29	29	29	
30	30	30	
31	31	31	
32	32	32	
33	33	33	
34	34	34	

DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

DIETRICH POST REORDER NO 84699

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
			SEE SHEET 1			

DRAWING NUMBER

0121-0037

-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
Y PER ASSY				

PARTS LIST

S OTHERWISE SPECIFIED
SIONS ARE IN INCHES
ANCES ARE:
ONS DECIMALS ANGLES
.XX ±
.XXX ±

IAL

O NOT SCALE DRAWING

GOULD PART NO.

GOULD Electronics

APPROVALS	DATE
DRAWN REVISED BY RTh	4/24/86
CHECKED	
PROJ ENG	

TITLE:
CABLE ASSY
I/O TO FLOPPY

SIZE C | DWG. NO. 0121-0037 | REV E

SCALE — | MODEL K450 | SHEET 2 OF 2

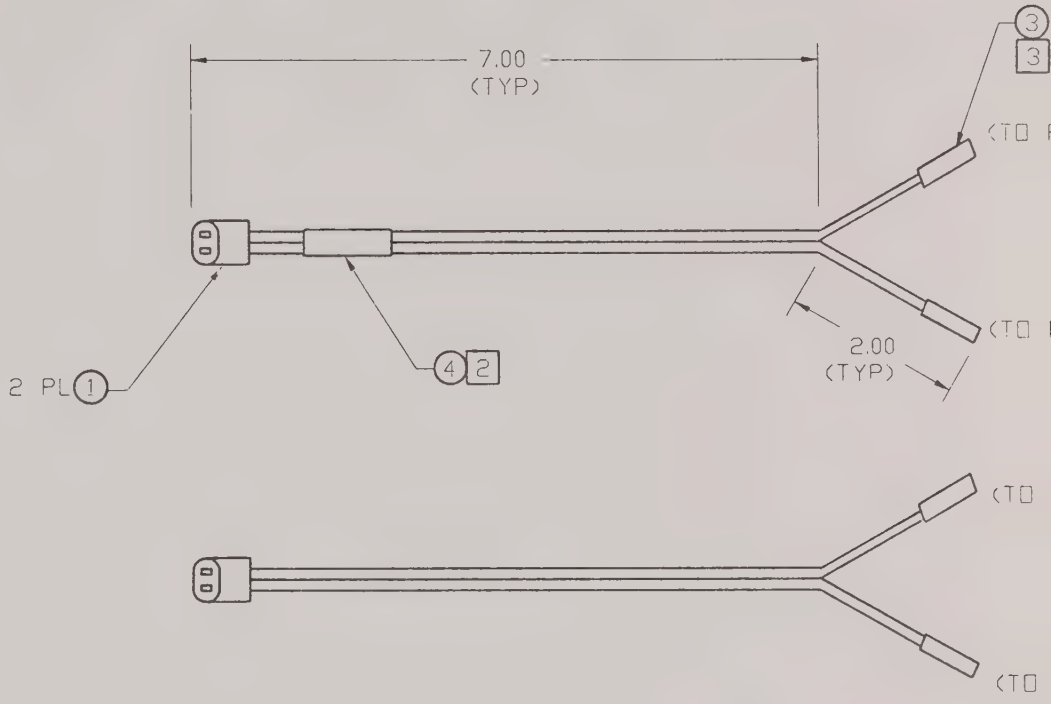
P. 2 of 2

BILL OF MATERIAL

AS OF 10/30/87

0121-0037-10 ASSY,CBL,FDC TO DISK,SINGLE DR
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0121-0037	DWG ASSY,CBL,FDC TO DISK	0	EA	REF
2	6000-0392-10	CONN 34 PIN EDGE CARD	2	EA	
3	7100-0111-10	CBL,FLAT,34 COND	1	FT	
4	7200-0048-10	CABLE MARKER	1	EA	
5	6000-0261-10	CONN PLZ KEY	1	EA	


7.00
(TYP)
3
3
(TO
(TO
2.00
(TYP)
2 PL
1
4
2
(TO
(TO

DWG. NO. 0121-0082	SH 1	REV A

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	A	RC 5509	RECORD CHANGE PER ECO #	DGW	RTM	12/15/86

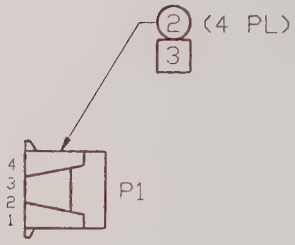
4 PL

1-4)

1-3)

1-2)

P1-1)



NOTES: UNLESS OTHERWISE SPECIFIED

1. DRAWING IS TO SCALE AND MAY BE USES AS A TEMPLATE.

[2] TAG HARNESS WITH ASSEMBLY NO., DASH NO., & REVISION LEVEL WHERE SHOWN.

[3] CONNECT CABLE CONNECTORS (ITEM 3) TO APPROPRIATE P1 SOCKET (ITEM 2) DESIGNATIONS.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
-10	0114 0005-20	K450
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .25 .XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN RTM	9-3-86
CHECKED DGW	9-12-86
PROJ ENG	

GOULD Electronics

TITLE: ASSY, CBL, FAN K450

SIZE	DWG NO	REV
D	0121-0082	A

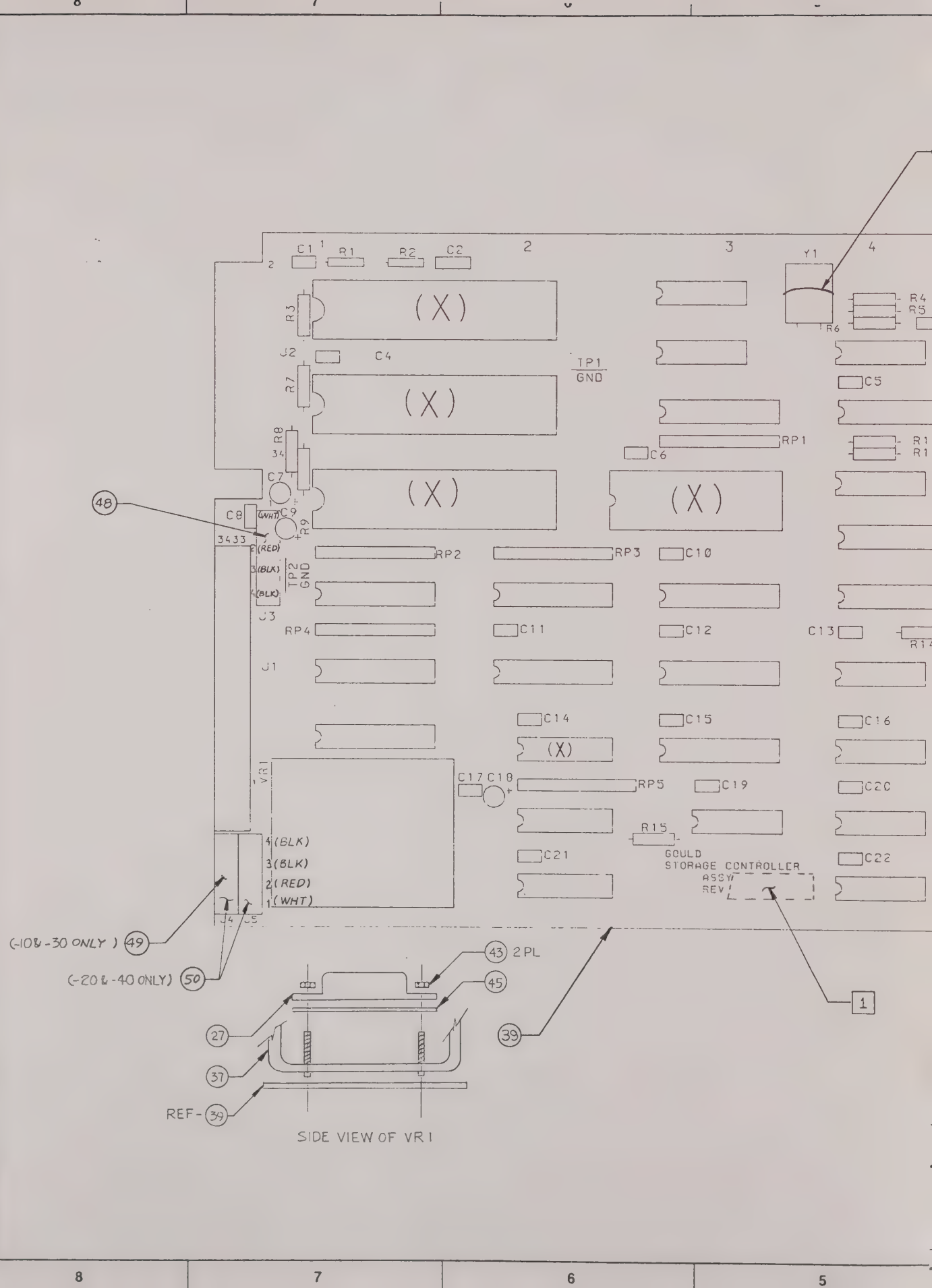
SCALE | MODEL | SHEET 1 OF

BILL OF MATERIAL

AS OF 10/30/87

0121-0082-10 ASSY CABLE, FAN K450
MODEL

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	C0121-0082	DWG, ASSY CABLE FAN, K450	0	EA	REF
1	2900-0009-10	FAN CORD 24" LONG	2	EA	
2	6100-0062-10	SKT 4 PIN	1	EA	
3	6000-0185-10	CONN SKT 22-18 AWG	4	EA	
4	7200-0039-10	TIE,MARKER,4"	1	EA	



C1
R1
R2
C2
2
3
4
Y1
R3
(X)
R4
R5
R6
J2
C4
TP1
GND
R7
C5
R8
34
RP1
R1
R1
C6
C7
C8
(WHT)
C9
R9
48
3433
2(RED)
3(BLK)
4(BLK)
TP2
GND
RP2
RP3
C10
J3
RP4
C11
C12
C13
R14
J1
C14
C15
C16
VR1
C17
C18
RP5
C19
C20
R15
4(BLK)
3(BLK)
2(RED)
1(WHT)
C21
GOULD
STORAGE CONTROLLER
ASSY
REV
C22
J4
J5
(-10 & -30 ONLY) 49
(-20 & -40 ONLY) 50
43 2PL
45
27
37
REF- 39
39
1
SIDE VIEW OF VR1

REVISIONS							
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5229	PILOT RELEASE PER ECO Nº	[illegible]	DGW	
	51	5254	REVISED PER ECO 4/14/86	RTM	DGW	4/15/86
	52	5270	REVISE PER ECO 4/14/86	RTM	DGW	4/15/86
	53	5356	REVISED PER ECO 6/30/86	RTM	DGW	7/3/86
	54	5440	ADD SOCKETS PER ECO 9-22-86	RTM		
	55	5520	REVISED PER ECO 12-16-86	MM	DGW	12-17-86
	A	5661	REVISED PER ECO 5/6-87	MM		

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. MARK ASSY Nº, DASH & REV. LEVEL APPOX. WHERE SHOWN USING INDELIBLE INK.
2. ASSY REFLECT SCH. DWG. (0121-0091) AND FAB. DWG. (0121-0092).
3. MANUFACTURE PER GOULD WORKMANSHIP STANDARD.
4. (X) INDCATES SOCKET LOCATIONS - REF ONLY.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± .02 .XXX ± .010 ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN APPLICAD	1/27/86
CHECKED DGLSRIGHT	1/27/86
PROJ ENG	

GOULD Electronics

TITLE: ASSY, STORAGE CONTROLLER PCB

SIZE D | DWG NO. 0121-0090 | REV A

SCALE | MODEL X450 | SHEET 1 OF 1

4 3 2 1

BILL OF MATERIAL

AS OF 10/30/87

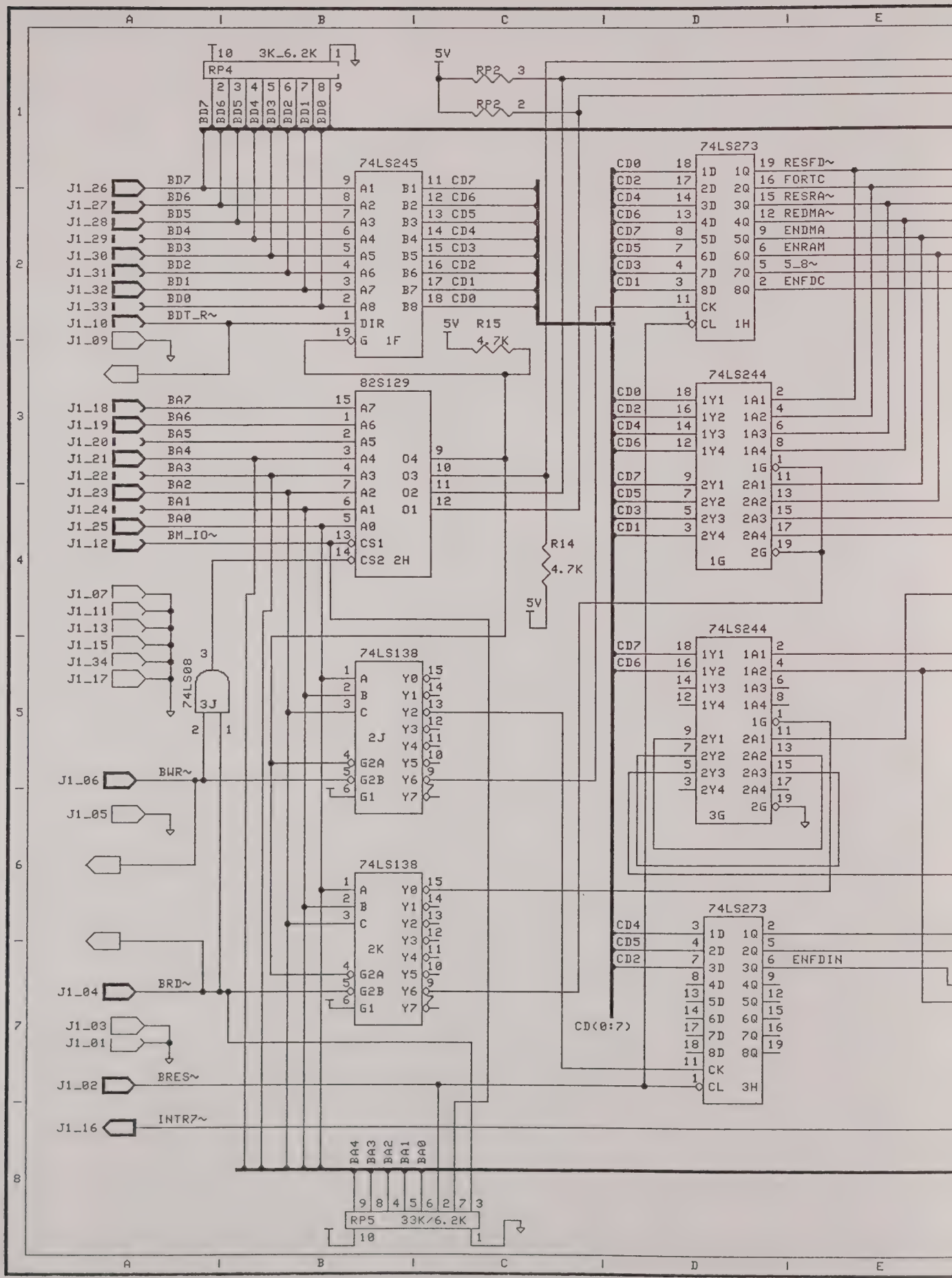
0121-0090-10 ASSY STORAGE CONTROLLER BOARD
MODEL: K450

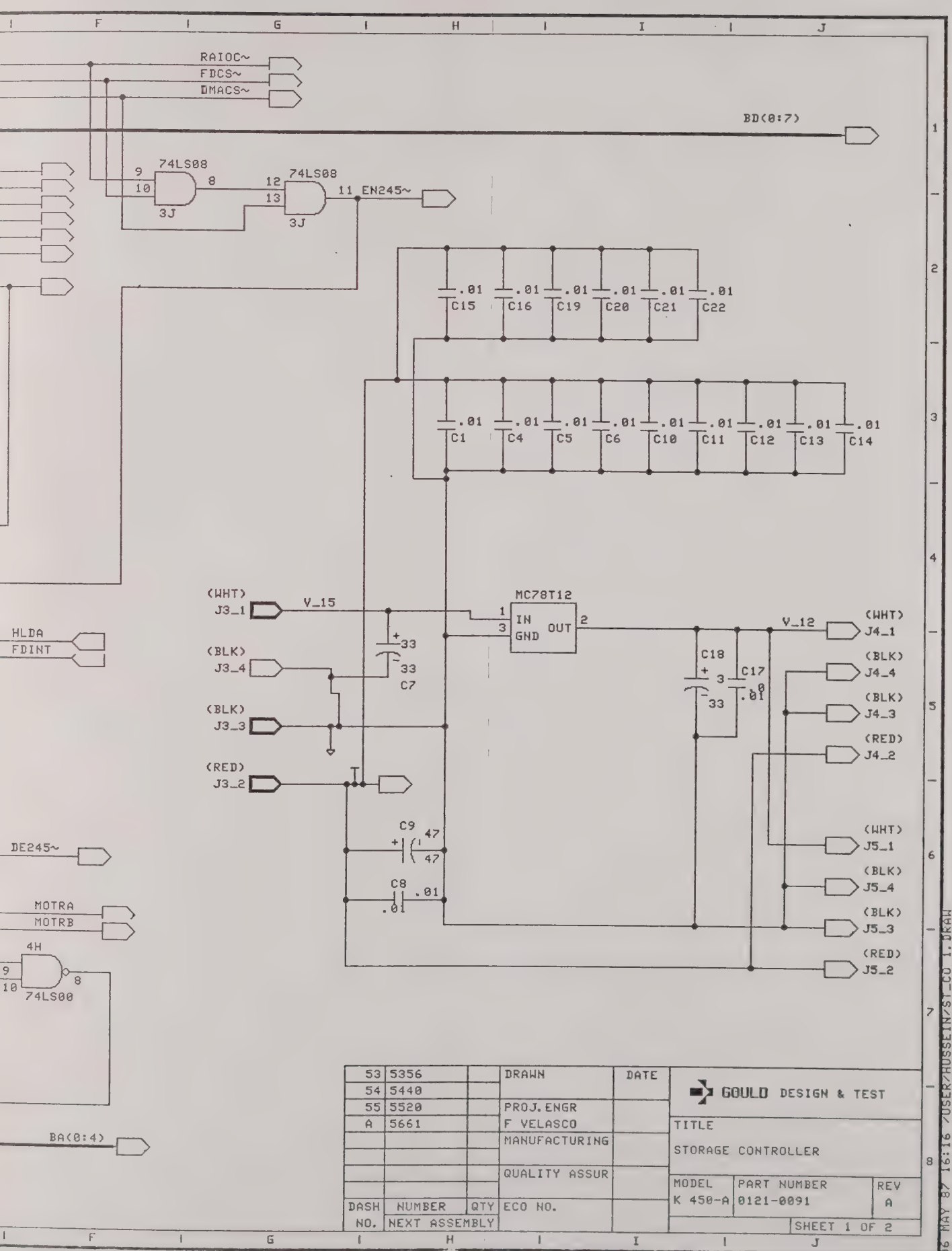
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0091	DWG STPRAGE CONTROLLER SCH	0	EA	REF
0	D0121-0090	DWG STORAGE CONTROLLER ASSY	0	EA	REF
1	5100-0021-10	XTAL 16.00 MHZ	1	EA	Y1
2	1800-0585-10	I/C, STATIC RAM,CMOS,8KX8	1	EA	3D
3	1800-0097-10	IC 7406N HEX INV BUF/DR	1	EA	3B
4	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	4H
5	1800-0107-10	IC 74LS04N HEX INV	1	EA	4B
6	1800-0109-10	IC 74LS08N 14, AND, X4	2	EA	3J,4G
7	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	2	EA	2J,2K
8	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	3A
9	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	1	EA	4F
10	1800-0267-10	IC 74LS240N OCTAL LINE	1	EA	4C
11	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	3	EA	1G,3G,4E
12	1800-0268-10	IC 74LS245N BUS TRANS	3	EA	1F,2F,3F
13	1800-0231-10	IC 74LS273N 20 FF, D, X8	2	EA	1H,3H
14	1800-0216-10	IC 74LS32N QUAD 2-INPUT	2	EA	4D,4K
15	1800-0298-10	IC 74LS373N OCTAL D TYP	1	EA	3C
16	1800-0293-10	IC 74LS374N D F/F 3 STA	1	EA	2G
17	1800-0115-10	IC 74LS74N, 14, FF, D, X2	1	EA	4J
18	1800-0358-10	IC P8257-5 DMA CONTROLLER	1	EA	1E
19	1800-0342-10	IC 8272 FLOP DISK CONT	1	EA	1C
20	0114-0479-10	PROM, I/O ADRS DECOD STOR SYS	1	EA	2H
21	1800-0584-10	IC, FLOPPY DISK INTERFACE	1	EA	1A
22	4010-0103-10	CAP,0.01UF,50V,10%,CER	17	EA	12,13,14, 15,16,17, 19,20,21, 22,4,5,6, 8 C1,10,11,
23	4000-0011-10	CAP,2.2UF,50V,20%,0.2LS,CER	1	EA	C2
24	4100-0006-10	CAP,20PF,500V,5%,MICA	1	EA	C3
25	4400-0045-10	CAP,33UF,25V,ELCTLT	2	EA	C18,C7
26	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	1	EA	C9
27	1700-0140-10	IC,REGULATOR, 3AMP,12V,TO-3	1	EA	VR 1
28	3000-1000-10	RES,100,5%,1/4W,C	1	EA	R1
29	3000-1002-10	RES,10K,5%,1/4W,C	1	EA	R7
30	3000-1500-10	RES,150,5%,1/4W,C	5	EA	R10,11,3,8 R9
32	3000-2400-10	RES,240,5%,1/4W,C	1	EA	R5
33	3000-2402-10	RES,24K,5%,1/4W,C	1	EA	R2
34	3000-5600-10	RES,560,5%,1/4W,C	2	EA	R4,6
36	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	5	EA	RP1-5
37	7000-0460-20	HEATSINK TO-3 BASE ONLY	1	EA	VR1
39	0121-0092-10	FAB STORAGE CONTROLLER BD	1	EA	
40	6000-0574-10	CONN HEADER 34 PIN	1	EA	J1

BILL OF MATERIAL
AS OF 10/30/87

0121-0090-10 ASSY STORAGE CONTROLLER BOARD
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
41	6100-0123-10	SKT 40 PIN DIP	3	EA	X1A,X1C, X1E
43	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	2	EA	VR1
45	7200-0016-10	INSULATOR TO-3	1	EA	VR1
47	7100-0017-10	WIRE,BUS,22 GA,TINNED	0	FT	Y-1
48	0114-0429-10	ASSY,CBL,FDC PWR IN	1	EA	J3
49	0114-0481-20	ASSY,CBL,PWR,FDC TO FLOPPY DR.	1	EA	J4
51	3000-4701-10	RES,4.7K,5%,1/4W,C	2	EA	R14,15
52	6100-0151-10	SKT 28 PIN DIP LO PROFIL	1	EA	X3D
53	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	1	EA	X2H


RP4 10 3K_6.2K 1
BD7 BD6 BD5 BD4 BD3 BD2 BD1 BD0
5V
RP2 3
RP2 2
74LS245
J1_26 BD7
J1_27 BD6
J1_28 BD5
J1_29 BD4
J1_30 BD3
J1_31 BD2
J1_32 BD1
J1_33 BD0
J1_10 BDT_R~
J1_09
A1 A2 A3 A4 A5 A6 A7 A8 DIR G 1F
B1 B2 B3 B4 B5 B6 B7 B8
11 CD7
12 CD6
13 CD5
14 CD4
15 CD3
16 CD2
17 CD1
18 CD0
5V R15 4.7K
74LS273
CD0 CD2 CD4 CD6 CD7 CD5 CD3 CD1
1D 2D 3D 4D 5D 6D 7D 8D CK CL
1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q 1H
19 RESFD~
16 FORTC
15 RESRA~
12 REDMA~
9 ENDMA
6 ENRAM
5 5_8~
2 ENFDC
82S129
J1_18 BA7
J1_19 BA6
J1_20 BA5
J1_21 BA4
J1_22 BA3
J1_23 BA2
J1_24 BA1
J1_25 BA0
J1_12 BM_IO~
A7 A6 A5 A4 A3 A2 A1 A0 CS1 CS2 2H
O4 O3 O2 O1
74LS244
1Y1 1Y2 1Y3 1Y4 2Y1 2Y2 2Y3 2Y4 1G 2G
1A1 1A2 1A3 1A4 2A1 2A2 2A3 2A4
R14 4.7K
5V
J1_07
J1_11
J1_13
J1_15
J1_34
J1_17
74LS08 3J 2J 2K 3G
74LS138
A B C G2A G2B G1
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7
J1_06 BWR~
J1_05
J1_04 BRD~
J1_03
J1_01
J1_02 BRES~
J1_16 INTR7~
CD(0:7)
ENFDIN
BA4 BA3 BA2 BA1 BA0
RP5 33K/6.2K 10 1



53	5356		DRAWN	DATE
54	5440			
55	5520		PROJ. ENGR	
A	5661		F VELASCO	
			MANUFACTURING	
			QUALITY ASSUR	
DASH NO.	NUMBER	QTY	ECO NO.	
	NEXT ASSEMBLY			

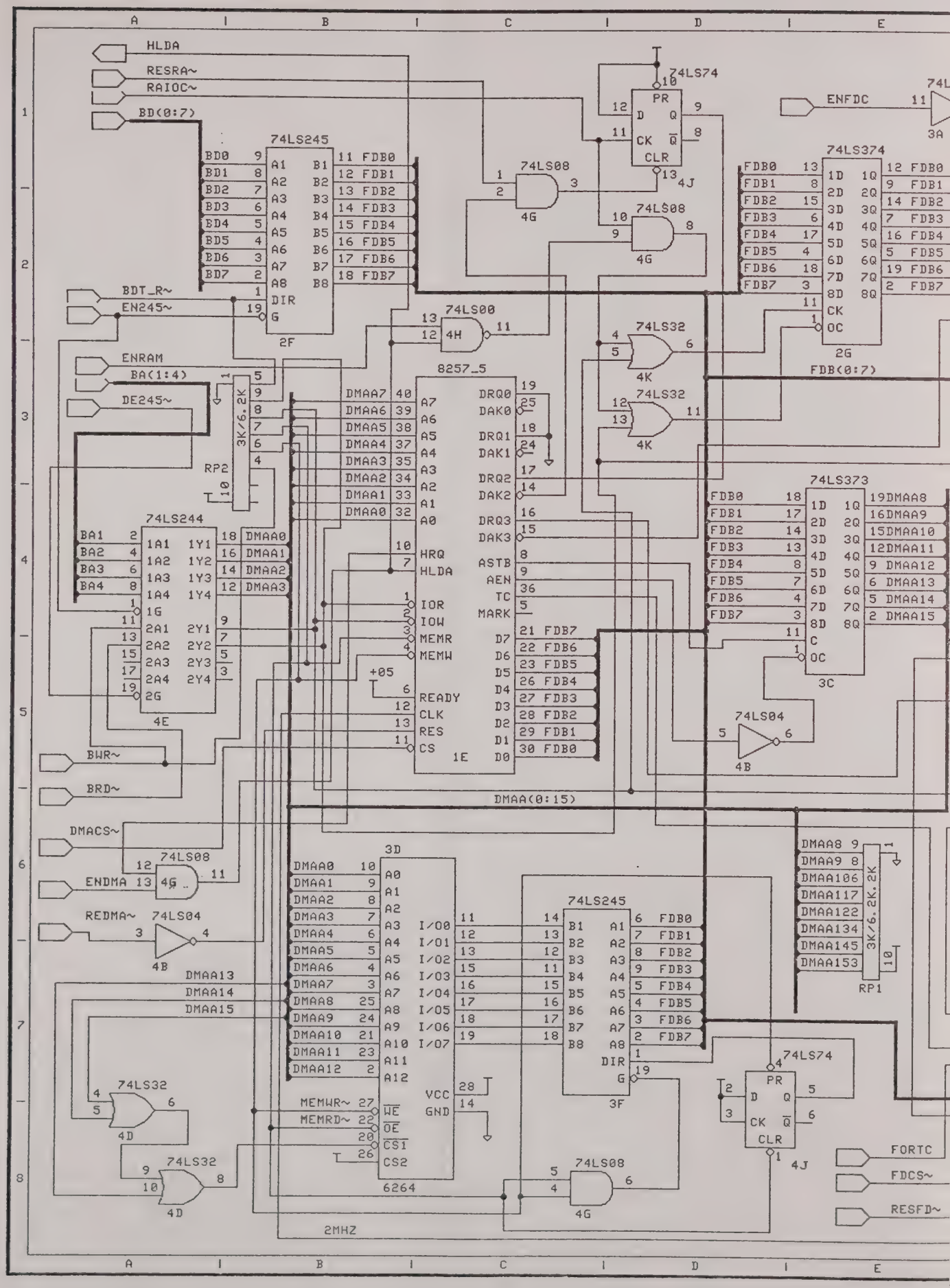
GOULD DESIGN & TEST

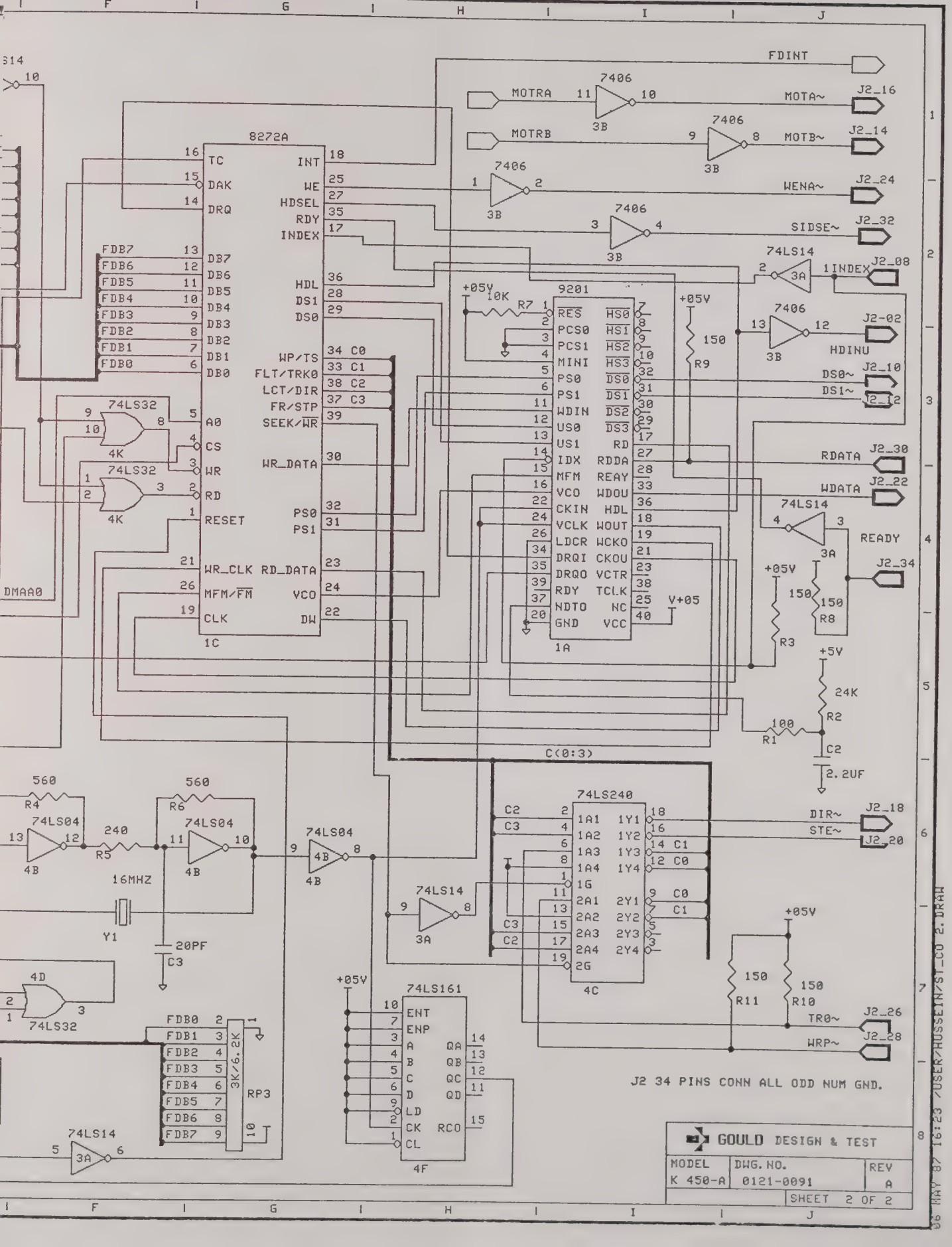
TITLE
STORAGE CONTROLLER

MODEL	PART NUMBER	REV
K 450-A	0121-0091	A

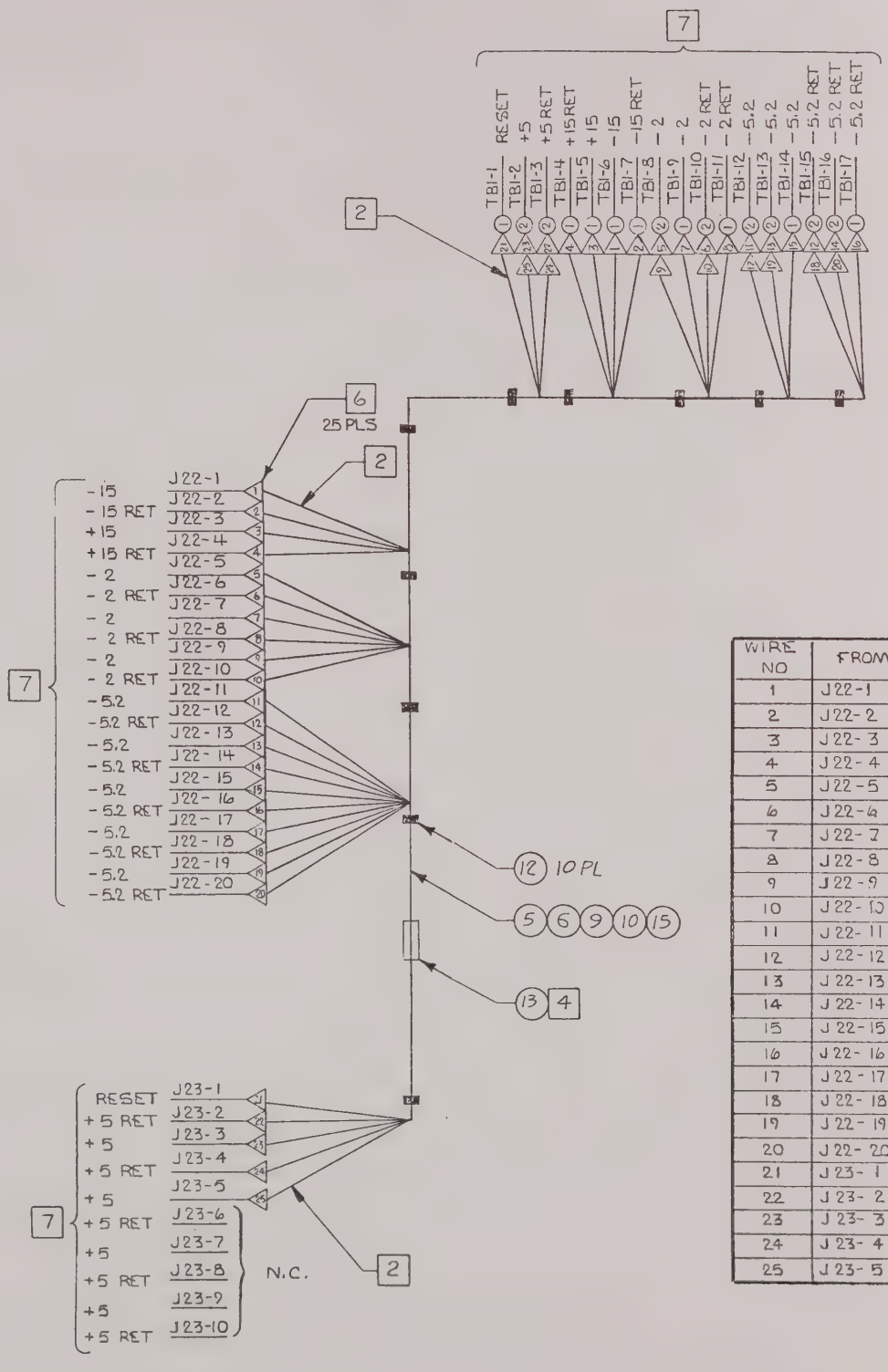
SHEET 1 OF 2

06 MAY 87 16:16 /USER/HUSSEIN/ST_CO 1.DRAW


HLDA
RESRA~
RAIOC~
BD(0:7)
74LS245
2F
BDT_R~
EN245~
ENRAM
BA(1:4)
DE245~
3K/6.2K
RP2
74LS244
4E
BWR~
BRD~
DMACS~
74LS08
ENDMA
4G
REDMA~
74LS04
4B
DMAA13
DMAA14
DMAA15
74LS32
4D
74LS32
4D
74LS00
4H
8257_5
1E
HRQ
HLDA
IOR
IOW
MEMR
MEMW
+05
READY
CLK
RES
CS
DRQ0
DAK0
DRQ1
DAK1
DRQ2
DAK2
DRQ3
DAK3
ASTB
AEN
TC
MARK
DMAA(0:15)
74LS08
4G
74LS74
4J
74LS08
4G
74LS32
4K
74LS32
4K
FDB(0:7)
74LS374
2G
ENFDC
74LS373
3C
74LS04
4B
3D
6264
MEMWR~
MEMRD~
2MHZ
74LS245
3F
74LS74
4J
74LS08
4G
DMAA8
DMAA9
DMAA10
DMAA11
DMAA12
DMAA13
DMAA14
DMAA15
3K/6.2K
RP1
FORTC
FDCS~
RESFD~



8272A
1C
9201
1A
74LS240
4C
74LS161
4F
74LS32
74LS04
74LS14
7406
3B
3A
4B
4D
4K
FDINT
MOTRA
MOTRB
MOTA~
MOTB~
WENA~
SIDSE~
INDEX
HDINU
DS0~
DS1~
RDATA
WDATA
READY
DIR~
STE~
TR0~
WRP~
J2_16
J2_14
J2_24
J2_32
J2_08
J2-02
J2_10
J2_12
J2_30
J2_22
J2_34
J2_18
J2_20
J2_26
J2_28
C(0:3)
16MHZ
Y1
20PF
C3
RP3
3K/6.2K
DMAA0
+05V
V+05
10K
R7
150
R9
R3
R8
24K
R2
100
R1
C2
2.2UF
560
R4
R6
240
R5
R11
R10
J2 34 PINS CONN ALL ODD NUM GND.
GOULD DESIGN & TEST
MODEL K 450-A
DWG. NO. 0121-0091
REV A
SHEET 2 OF 2
06 MAY 87 16:23 /USER/HUSSEIN/ST_CO 2.DRAW



WIRE NO	FROM	TO
1	J22-1	TB1-6
2	J22-2	TB1-7
3	J22-3	TB1-5
4	J22-4	TB1-4
5	J22-5	TB1-8
6	J22-6	TB1-10
7	J22-7	TB1-9
8	J22-8	TB1-11
9	J22-9	TB1-8
10	J22-10	TB1-10
11	J22-11	TB1-12
12	J22-12	TB1-15
13	J22-13	TB1-13
14	J22-14	TB1-16
15	J22-15	TB1-14
16	J22-16	TB1-17
17	J22-17	TB1-12
18	J22-18	TB1-15
19	J22-19	TB1-13
20	J22-20	TB1-16
21	J23-1	TB1-1
22	J23-2	TB1-3
23	J23-3	TB1-2
24	J23-4	TB1-3
25	J23-5	TB1-2

REVISIONS						
ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	A	5279	PROD REL PER ECO 5/1/86	RTM	DGW	5/1/86

AWG	LNG ±.25	COLOR	
16	7.9	VIO	-15
16		BLK	-15 RET
16		ORN	+15
16	7.9	BLK	+15 RET
16	10.5	GRY	-2
16		BLK	-2 RET
16		GRY	-2
16		BLK	-2 RET
16		GRY	-2
16	10.5	BLK	-2 RET
16	13.8	VIO	-5.2
16	14.9	BLK	-5.2 RET
16	13.8	VIO	-5.2
16	14.9	BLK	-5.2 RET
16	13.8	VIO	-5.2
16	14.9	BLK	-5.2 RET
16	13.8	VIO	-5.2
16	14.9	BLK	-5.2 RET
16	13.9	VIO	-5.2
16	14.9	BLK	-5.2 RET
16	14.2	YEL	RESET
16		BLK	+5 RET
16		GRY	+5
16		BLK	+5 RET
16	14.2	GRY	+5

7

NOTES: UNLESS OTHERWISE SPECIFIED

1. DRAWING IS TO SCALE AND MAY BE USED AS A TEMPLATE.
2. IDENTIFY LUGS & ENDS OF WIRES WITH DESTINATION AS SHOWN.
3. TIP OF TERMINATION TRIANGLE DENOTES END OF CUT WIRE BEFORE LUGGING.
4. TAG HARNESS WITH ASSY NO, DASH NO, AND REV. LEVEL.
5. ▷ TERMINATION TRIANGLE INDICATES WIRE NO.
   ◯ CIRCLE INDICATES ITEM NO. ON PARTS LIST.
6. ENDS OF WIRES STRIPPED & TINNED 1/4 IN.
7. SIGNAL NAMES SHOWN FOR REFERENCE ONLY.
8. WIRE ROUTING SEQUENCE: 15, 16, 17, 12, 13, 14, 10, 11, 8, 9, 4, 5, 6, 7, 3, 2, 1.
9. AFTER REMOVAL OF HARNESS FROM NAIL-BOARD, BEND ALL WIRE ENDS 90° DOWNWARD AT BUNDLE.
10. LUG ORIENTATION: FLAT SIDE OF LUGS TO FACE INWARD TOWARDS POWER SUPPLY.
11. ALL CABLE TIE CLAMPS TO FACE INWARD TOWARDS POWER SUPPLY.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
-10	0121-0006-20	K450

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± / DECIMALS .XX ± .XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN REVISED BY RTMoney	5/1/86
CHECKED DGWright	5/1/86
PROJ ENG	

GOULD Electronics

TITLE: ASSY, HARNESS, P.S. TO MOTHER BD, K450

SIZE D | DWG NO 0121-0167 | REV A

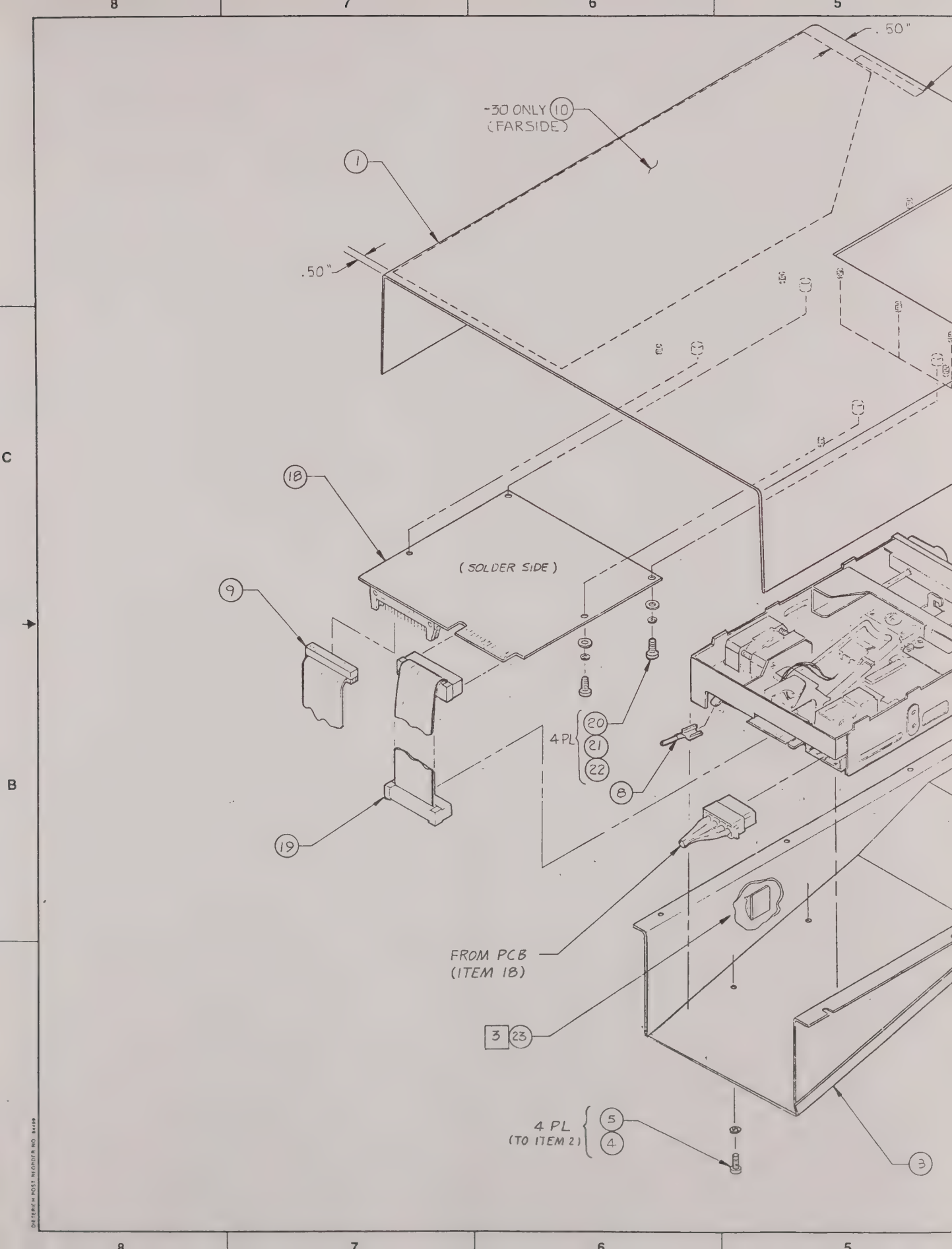
SCALE 1/1 | MODEL K450 | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

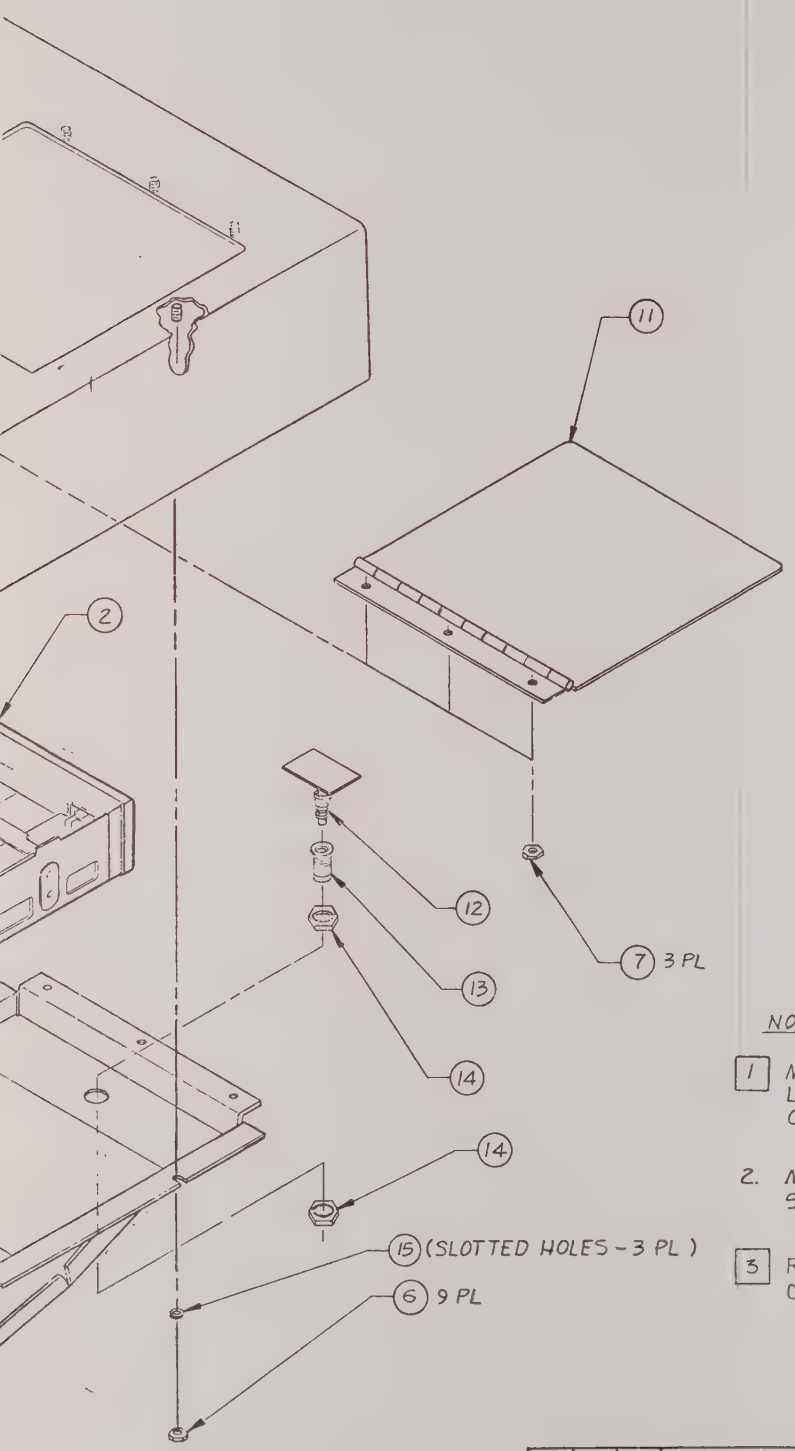
0121-0167-10 ASSY,HARNESS,PS TO MOTHER,K450
MODEL K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0167	DWG,ASSY,HARNESS,PS TO MBD,K45	0	EA	REF
1	6200-0069-10	TERM LUG SNAP SPADE 22G INSLT	9	EA	
2	6200-0055-10	TERM LUG SPADE 10-12 #6	8	EA	
5	7150-0016-08	WIRE,PVC,16 AWG,GRY	5	FT	
6	7150-0016-03	WIRE,PVC,16 AWG,ORN	1	FT	
9	7150-0016-07	WIRE,PVC,16 AWG,VIO	7	FT	
10	7150-0016-10	WIRE,PVC,16 AWG,BLK	13	FT	
12	7200-0003-10	TIE,CBL,4"	10	EA	
13	7200-0039-10	TIE,MARKER,4"	1	EA	
15	7150-0016-04	WIRE,PVC,16 AWG,YEL	1	FT	


.50"
-30 ONLY (10)
(FARSIDE)
1
.50"
18
(SOLDER SIDE)
9
4 PL
20
21
22
8
19
FROM PCB
(ITEM 18)
3
23
4 PL
(TO ITEM 2)
5
4
3

DWG. NO. 0121-0160. SH 1 REV B

REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION		DWN	CHKD	APPD
	50	5465	PILOT REL PER ECO	10-1-86	RTM	DGW	10/1/86
	51	5495	REVISED PER ECO	11-20-86	MM	DGW	11/25/86
	52	5541	REVISED PER ECO	1-7-87	MM	DGW	1/12/87
	52	5556	RELEASE FOR SIEMAN	1-20-87	MM	DGW	1/20/87
	A	5661	REV ROLL ONLY	5-6-87	MM		
	B	5718	REVISED PER ECO	6-12-87	MM	DGW	6/15/87
	B	5723	ADD - 40	6-17-87	MM	DGW	6/17/87



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY NO., DASH NO., AND REVISION LEVEL APPROXIMATELY WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.
3. ROUTE ITEM 9 AND POWER HARNESS THRU CABLE CLAMP. (FARSIDE)

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
-30	K450B-1XX	K450B
-10	K450-1XX	K450

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN RTM	10/1/86
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: TOP ASSEMBLY, SINGLE DISK DRIVE

SIZE D | DWG. NO. 0121-0168 | REV. B

SCALE 1/2 | MODEL A450 | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

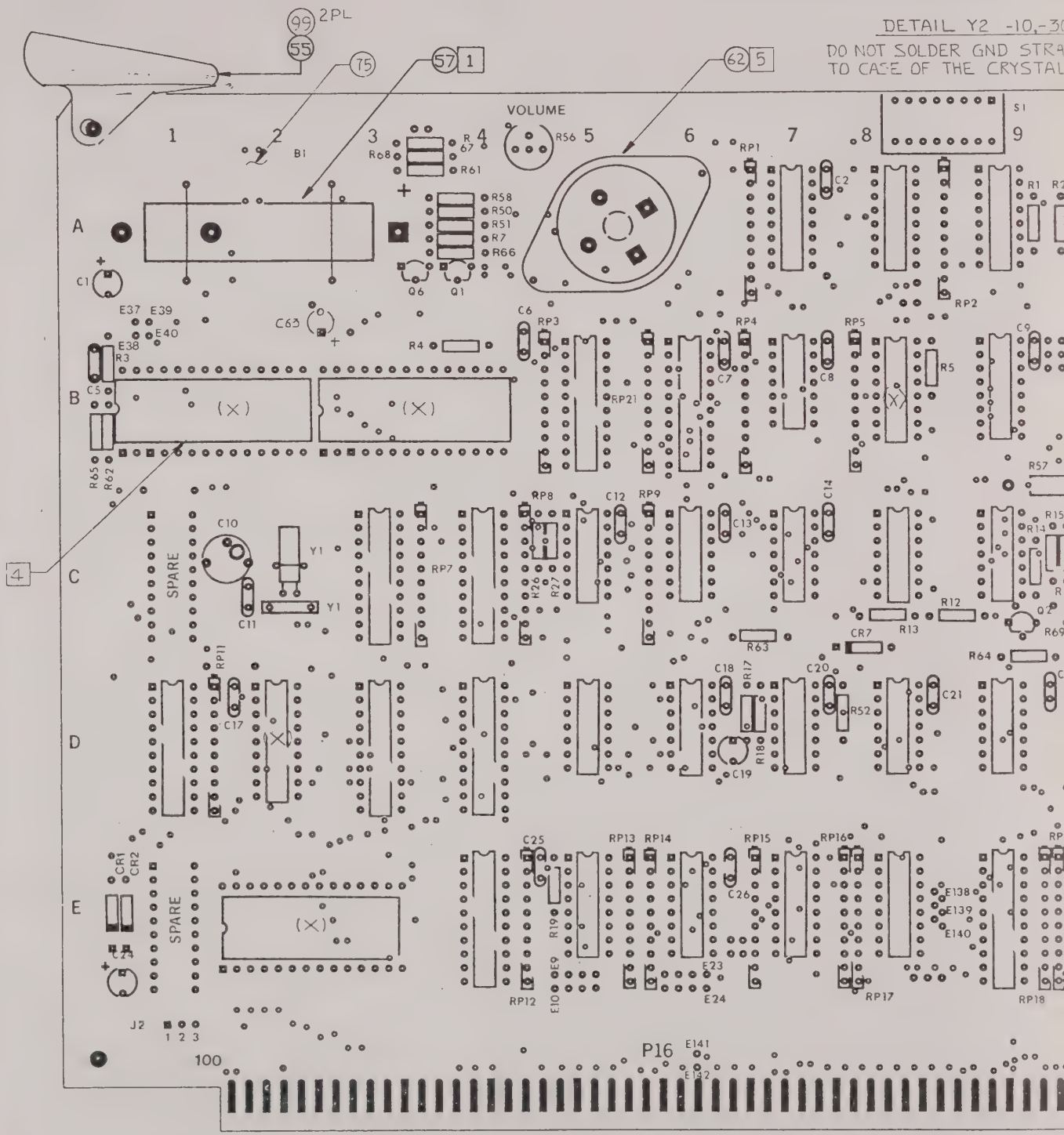
0121-0168-10 ASSY,TOP,SINGLE DISK,K450
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0168	DWG,ASSY,TOP,SINGLED DISK,K450	0	EA	
1	0117-0716-10	FAB,COVER TOP,SINGLE DISK	1	EA	
2	7500-0003-10	FLOPPY DISK DR 5" 1/2 HT	1	EA	
3	0121-0088-10	BRACKET, DISK DRIVE, K450	1	EA	
4	7085-1006-00	WSHR,INT TOOTH LOCK,#6,STZN	4	EA	
5	7000-0463-08	SCREW 3MM X 8MM	4	EA	
6	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	9	EA	
7	7071-1440-00	NUT,S-LOCK,4-40,STD,STZN	3	EA	
8	0117-0626-10	ASSY,GND HARNESS,DOS/2	1	EA	
9	0114-0482-10	ASSY,CBL,K101 TO FDC SIGNALS	1	EA	
11	0117-0717-10	FAB,DOOR HINGE ASSY,SNGL DISK	1	EA	
12	7200-0063-10	STUD ASSY,LATCH	1	EA	
13	7200-0064-10	RECEPTACLE,LATCH	1	EA	
14	7200-0065-10	NUT,RETAINING,RECEPTACLE	2	EA	
15	7082-1006-00	WSHR,FLAT,#6,LP,STZN	3	EA	
18	0121-0090-10	ASSY STORAGE CONTROLLER BOARD	1	EA	
19	0121-0037-10	ASSY,CBL,FDC TO DISK,SINGLE DR	1	EA	
20	7082-1004-00	WSHR,FLAT,#4,LP,STZN	4	EA	
21	7085-1004-00	WSHR,INT TOOTH LOCK,#4,STZN	4	EA	
22	7011-1440-10	SCR,X,PH,4-40 X 5/16,STZN	4	EA	
23	7200-0019-10	CBL CLAMP,FLAT,RIBBON	1	EA	

B-RC	5707	REVISED PER ECO	6/
C	5738	REVISED PER ECO	7/
D	5806	REVISED PER ECO	8.

DETAIL Y2 -10,-3

DO NOT SOLDER GND STR
TO CASE OF THE CRYSTAL



NOTE: UNLESS OTHERWISE SPECIFIED

1. SECURE BATTERY, B1 TO BOARD WITH ITEM 57 BEFORE SOLDERING LEADS.
2. (X) INDICATES SOCKET LOCATIONS - REF ONLY.
3. MARK WITH ASSY DASH NO. AND REV LEVEL APPROX WHERE SHOWN USING CONTRASTING INDELIBLE INK.
4. PIN 1 OF ITEM 49 LOCATES IN E N 3 OF ITEM 2 WHEN USING 24 PIN DEVICE.
5. NOTE: IN BUZZER GOES TO TOP

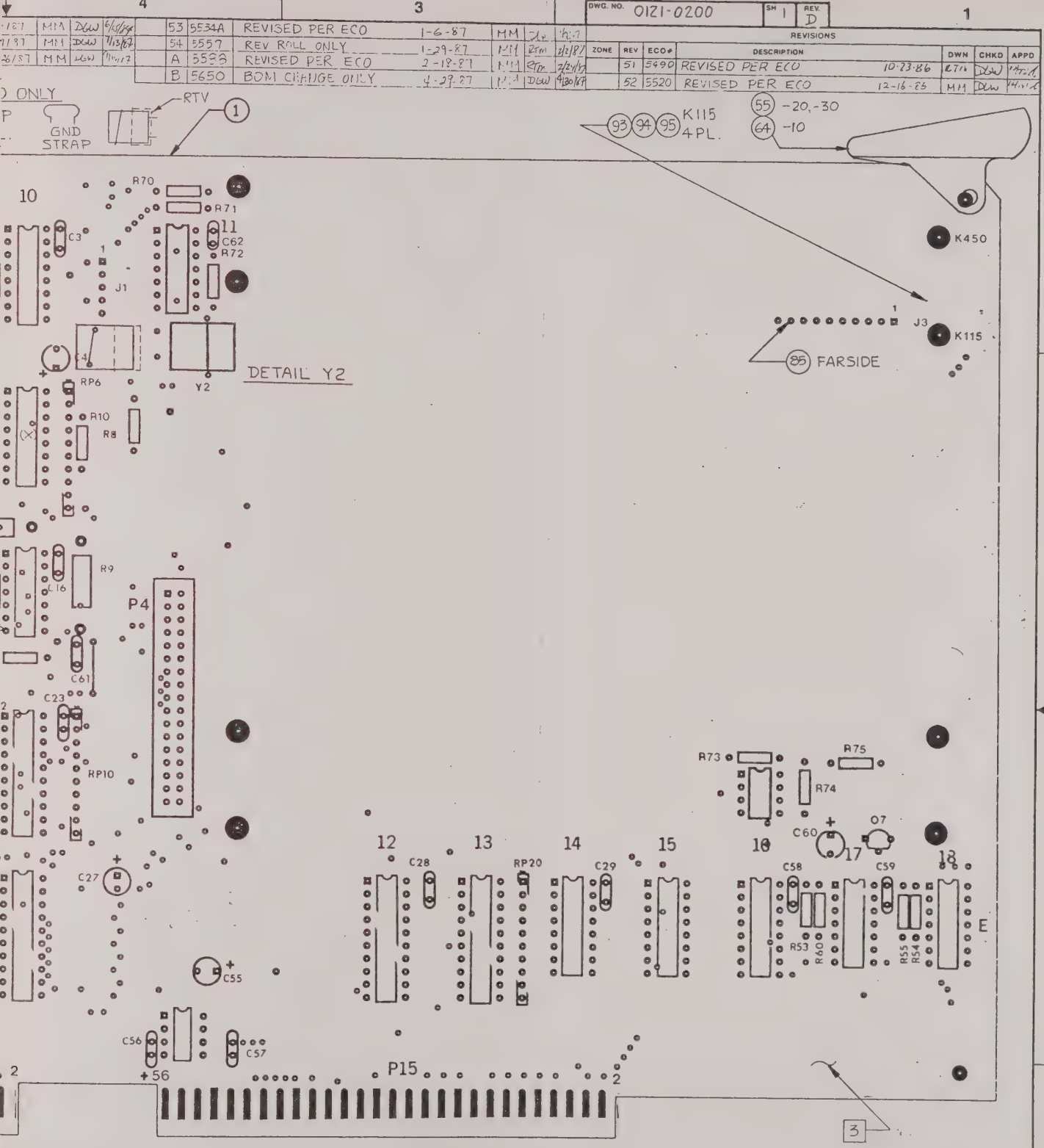
JUMPER	AS FITCHED	-10 K45
E9 TO E10	OUT	JMP
E23 TO E24	OUT	
E138 TO E139	OUT	JMP
E139 TO E140	OUT	
E141 TO E142	OUT	JMP
J2-1 TO J2-2	OUT	JMP
J2-2 TOJ2-3	OUT	

DIETRICH POST REORDER NO. 9183

DWG. NO.	SH	REV.
0121-0200	1	D

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	5490	REVISED PER ECO 10-23-86	RTM	DGW	
	52	5520	REVISED PER ECO 12-16-86	MM	DGW	
	53	5534A	REVISED PER ECO 1-6-87	MM	DGW	
	54	5557	REV RAIL ONLY 1-29-87	MM	RTM	2/2/87
	A	5598	REVISED PER ECO 2-18-87	MM	RTM	2/24/87
	B	5650	BOM CHANGE ONLY 4-29-87	MM	DGW	4/30/87



-20 K115	-30
	JMP
JMP	
	JMP
JMP	
	JMP
JMP	JMP

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					
				PARTS LIST	
			10 0121-0006-20	K450	

DASH NO. | NEXT ASSY | USED ON

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS .XX ± / .XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN DGW	9/86
CHECKED RTM	10/86
PROJ ENG	

GOULD Electronics

TITLE: ASSY, DATA DISPLAY PCB (NEW)

SIZE D | DWG NO 0121-0200 | REV D

SCALE 2/1 | MODEL K450 / K115 | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0121-0200-30 ASSY,PCB,DATA DISPLAY,K450B
MODEL: K450/K115

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0200	DWG,ASSY,DATA DISPLAY	0	EA	REF
0	D0121-0201	DWG,SCHEM,DATA DISPLAY	0	EA	REF
1	0121-0202-10	FAB,DATA DISPLAY PCB	1	EA	
2	3000-2000-10	RES,200,5%,1/4W,C	1	EA	R64
3	3000-5600-10	RES,560,5%,1/4W,C	2	EA	R70,72
4	3000-2400-10	RES,240,5%,1/4W,C	1	EA	R71
5	3050-4700-10	RES,470,5%,1/2W,C	1	EA	R8
6	3000-8206-10	RES,82,5%,1/4W,C	1	EA	R12
7	3000-4700-10	RES,470,5%,1/4W,C	1	EA	R5
8	3000-2201-10	RES,2.2K,5%,1/4W,C	14	EA	3,4,60,62 53-55,58 65,67,68 R19,1,2
9	3000-1002-10	RES,10K,5%,1/4W,C	4	EA	R17,18,52 R63
10	3050-3906-10	RES,39,5%,1/2W,C	1	EA	R57
12	3100-7506-10	RES,75,1%,1/8W,MF	1	EA	R13
13	3100-6040-10	RES,604,1%,1/8W,MF	1	EA	R14
14	3100-8250-10	RES,825,1%,1/8W,MF	1	EA	R15
15	3100-9090-10	RES,909,1%,1/8W,MF	1	EA	R16
16	4000-0009-10	CAP,0.1UF,100V,10%,CER	2	EA	C5,6
17	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	7	EA	C1,4,24,27 C19,C60 C63
18	4010-0103-10	CAP,0.01UF,50V,10%,CER	23	EA	14,16,18 20,56,57 21-23,25 26,28,29 58,59,8 7,12,17 C2,3,9,13
19	4010-0100-10	CAP,10PF,50/100V,5%,CER	1	EA	C11
20	7000-0451-10	BATTERY, N.I.C.D. 2.4V	1	EA	B1
21	3000-3900-10	RES,390,5%,1/4W,C	1	EA	R66
22	6100-0151-10	SKT 28 PIN DIP LO PROFIL	3	EA	X2E,X1B X3B
23	4600-0010-10	CAP,7-40PF,100V,CER	1	EA	C10
24	1300-0028-10	TRAN 2N3904	2	EA	Q2,6
25	1400-0019-10	TRAN 2N3906	1	EA	Q1
26	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	2	EA	X8B,X10B
27	3000-6800-10	RES,680,5%,1/4W,C	2	EA	R51,9
28	3700-0083-10	RPAK,2.2K,0.18W,2%,10/9	8	EA	12,15,20 14 RP1,5,6,9
29	3700-0085-10	RPAK,22K,0.3W,2%,10/9	5	EA	21 RP3,7,8,11

BILL OF MATERIAL
AS OF 10/30/87

0121-0200-30 ASSY,PCB,DATA DISPLAY,K450B
MODEL: K450/K115

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
30	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	7	EA	4,13 RP10,16-19
31	1800-0092-10	IC 74S04N, 14, INV, X6	1	EA	11A
32	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	7C
33	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	6C
34	1800-0110-10	IC 74LS10N TRIPLE NAND	2	EA	9D,5D
35	1800-0111-10	IC 74LS20N DUAL 4-IN	1	EA	8D
36	1800-0115-10	IC 74LS74N, 14, FF, D, X2	2	EA	7B,17E
37	1800-0254-10	IC 74LS85N 4-BIT MAG	2	EA	5E,6E
38	1800-0404-10	IC 74LS136N 14 XOR X4	1	EA	9C
39	1800-0301-10	IC 74LS156N 16	1	EA	14E
40	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	6	EA	15E,16E 7A-10A
41	1800-0121-10	IC 74LS175N QUAD D F/F	1	EA	9B
42	1800-0267-10	IC 74LS240N OCTAL LINE	3	EA	10D,4E,6B
43	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	3	EA	13E,5B,1D
44	1800-0268-10	IC 74LS245N BUS TRANS	3	EA	10E,3C,4C
45	1800-0231-10	IC 74LS273N 20 FF, D, X8	3	EA	12E,3D,4D
46	1800-0193-10	IC 74LS138N 16 DCDR, 3TO8	1	EA	8E
47	1800-0097-10	IC 7406N HEX INV BUF/DR	2	EA	10C,18E
48	1800-0038-10	IC 74S20N 14 NAND X2	1	EA	8C
49	1850-0149-10	IC HM6264P-12,8KX8 HS STAT RAM	2	EA	1B,3B
50	1800-0319-10	IC D8259A PROG INTR CNT	1	EA	2E
51	1800-0341-10	IC MSM5832 MICRO-PROC	1	EA	2D
52	1800-0311-10	IC 7438N QUAD 2-INPUT	1	EA	7D
53	5100-0041-10	CRYSTAL,10.00MHZ,FUND,HC80,AT	1	EA	Y2
54	5100-0018-10	XTAL 32.768KHZ,	1	EA	Y1
55	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
57	7200-0032-10	MOUSETAIL, 4" LONG	2	EA	
58	3000-1001-10	RES,1K,5%,1/4W,C	2	EA	R69,10 R69,10,75
59	3000-2200-10	RES,220,5%,1/4W,C	1	EA	R26
60	3000-3300-10	RES,330,5%,1/4W,C	1	EA	R27
61	3300-0096-10	POT,1K,0.5W,20% 1T,PC,STR	1	EA	R56
62	7400-0002-10	BUZZER/ALARM	1	EA	
63	4400-0045-10	CAP,33UF,25V,ELCTLT	1	EA	C55
65	1800-0351-10	IC 74LS12N 3-IN NAND	1	EA	5C
66	1800-0352-10	IC 74LS22N 4-IN NAND OPE	1	EA	6D
67	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R61
68	1000-0002-10	DIO,1N4152	1	EA	CR7
69	8300-0027-10	TAPE,FOAM,1X1X1/8"	0	FT	SS OF 3A
70	4000-0011-10	CAP,2.2UF,50V,20%,0.2LS,CER	1	EA	C61
71	6000-0389-10	CONN 34 PIN ST HDR	1	EA	P4
72	6100-0156-10	SKT 18 PIN	1	EA	2D
73	3000-2700-10	RES,270,5%,1/4W,C	1	EA	R7
74	3000-3301-10	RES,3.3K,5%,1/4W,C	1	EA	R50

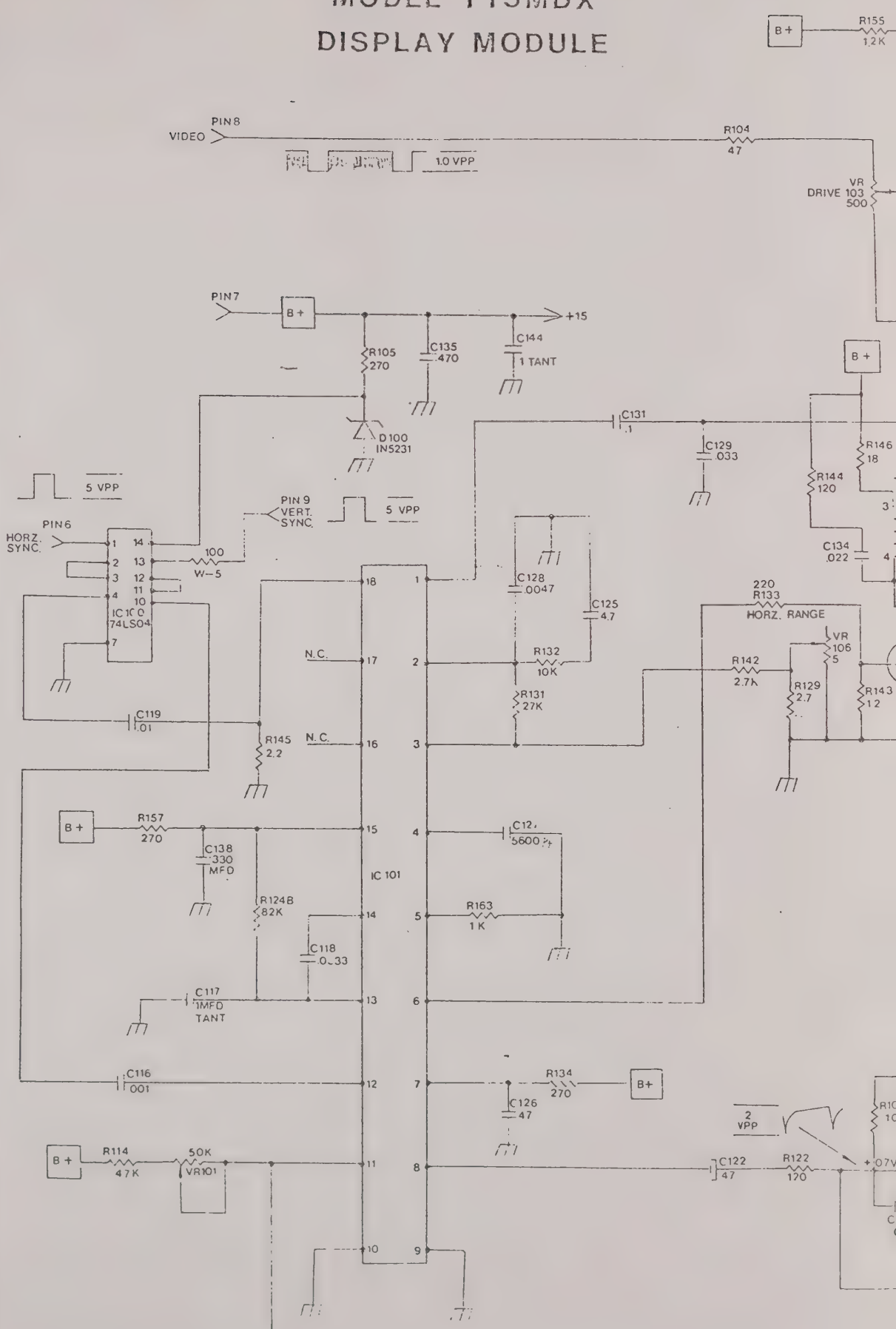
BILL OF MATERIAL

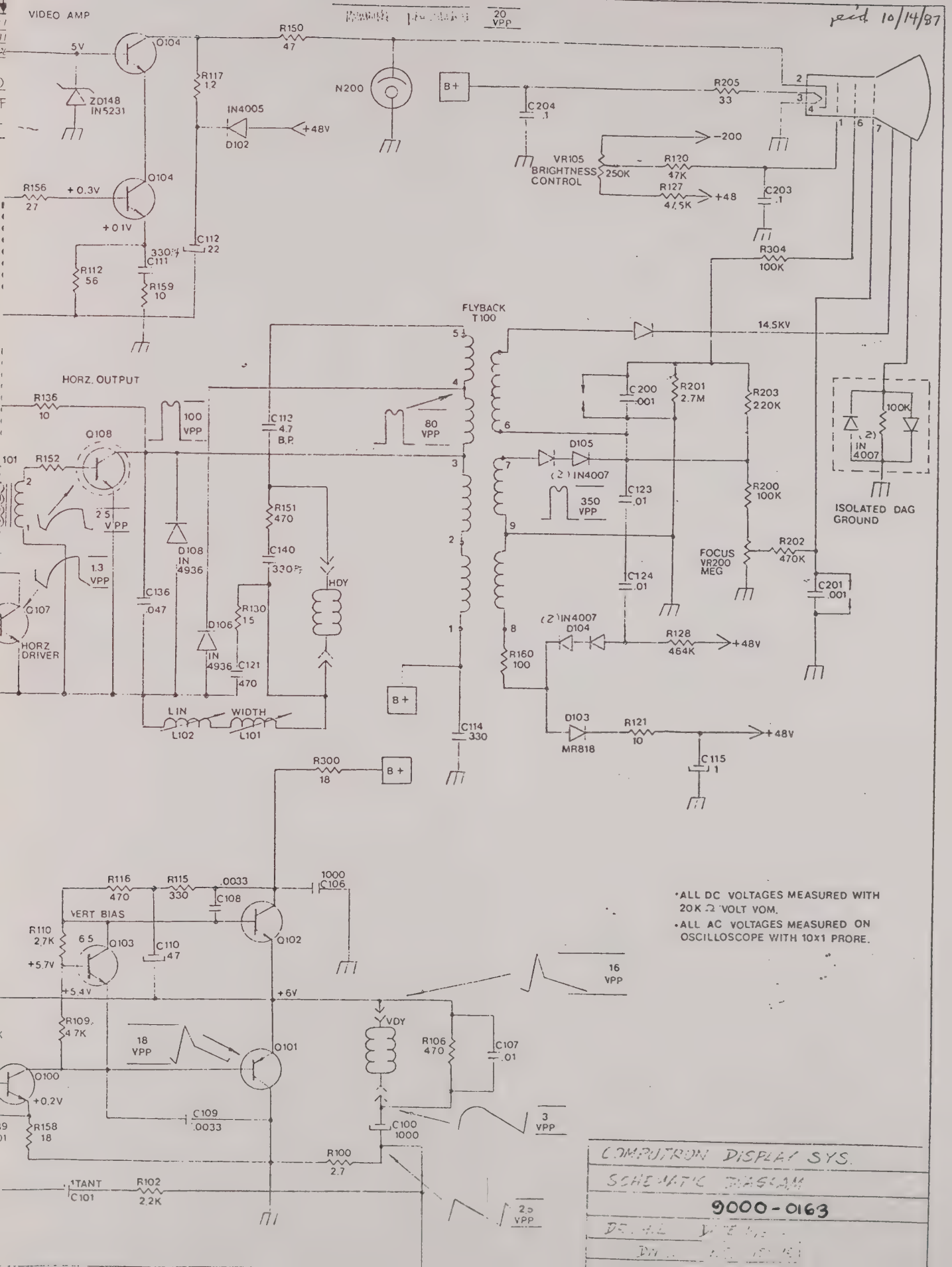
AS OF 10/30/87

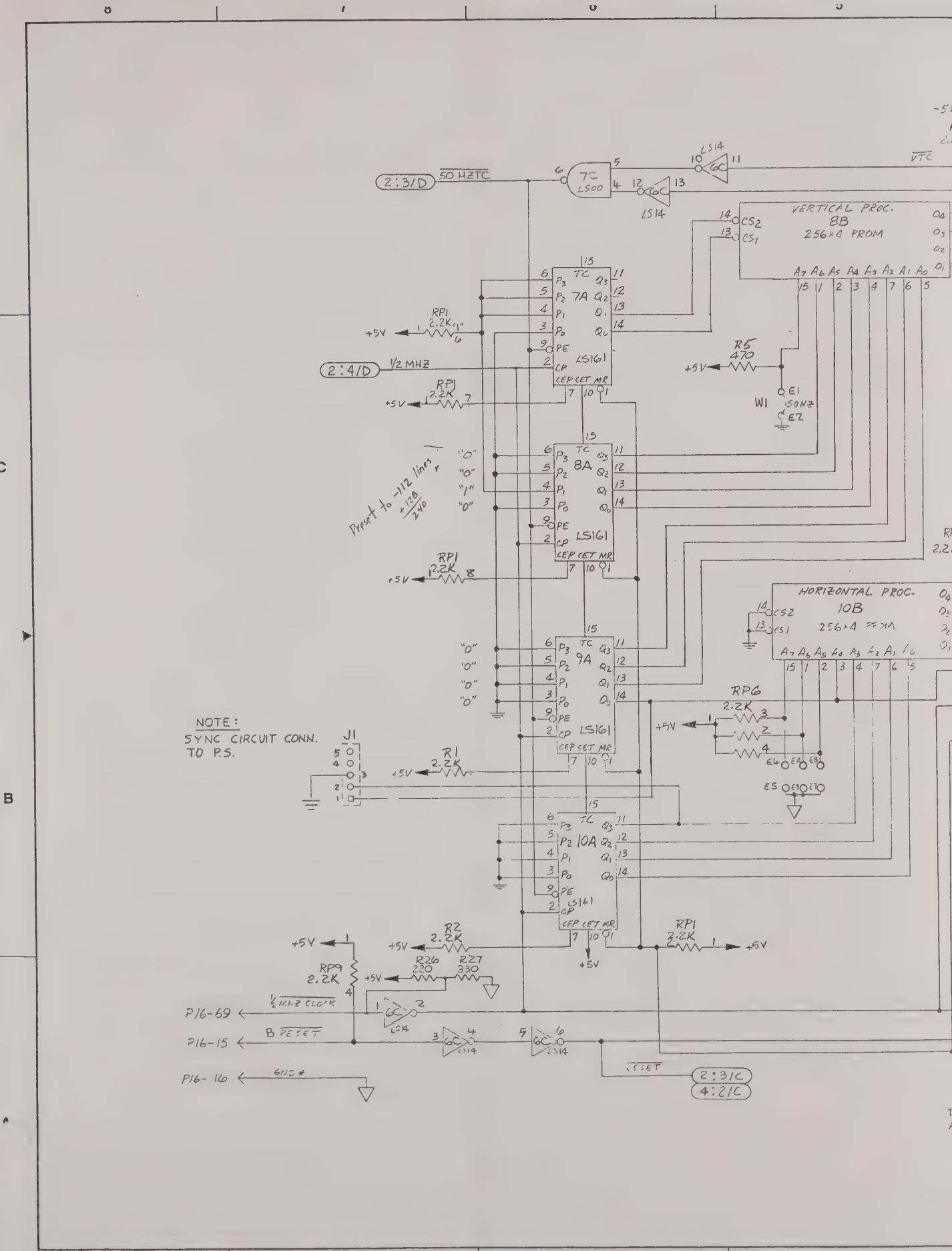
0121-0200-30 ASSY,PCB,DATA DISPLAY,K450B
MODEL: K450/K115

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
75	0114-0432-10	LABEL, CAUTION "NICD ONLY"	1	EA	
76	0117-0149-10	ASSY,PROM,VERT,K105	1	EA	8B
77	0117-0150-10	ASSY,PROM,HORIZ,K105	1	EA	10B
83	6000-0298-10	CONN 3 PIN ST HDR SGL ROW	1	EA	J2
84	6000-0571-10	CONN SHORTING PLUG	1	EA	@J2
85	6000-0613-10	CONN,10 POS RT ANG HDR,.318	1	EA	J3
86	1300-0001-10	TRAN 2N2222	1	EA	Q7
87	3000-7506-10	RES,75,5%,1/4W,C	1	EA	R73
88	3000-4301-10	RES,4.3K,5%,1/4W,C	1	EA	R74
90	0121-0205-10	ASSY,CBL,COMP115MX-7 TO DSPLY	1	EA	
91	1800-0597-10	IC,DIGITAL POT,50K, 8-PIN DIP	1	EA	16D
92	6000-0606-10	CONN 5 PIN ST HDR SGL ROW	1	EA	J1
93	1700-0071-10	IC LF356AN MONO OP AMP	1	EA	11E
94	3000-1003-10	RES,100K,5%,1/4W,C	1	EA	R75
94	3000-5102-10	RES 51K OHM,1/4W,5% CAR	1	EA	R75
99	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
100	1000-0003-10	DIO,5082-2811	2	EA	CR1,CR2
101	4010-0680-10	CAP 68PF,50/100V /10% .1	1	EA	C62

MODEL 115MDX
DISPLAY MODULE




VIDEO AMP
rec'd 10/14/87
20 VPP
5V
Q104
R150 47
R117 1.2
ZD148 IN5231
IN4005
D102
+48V
N200
B+
C204 .1
R205 33
-200
VR105 BRIGHTNESS CONTROL 250K
R120 47K
R127 47.5K
+48
C203 .1
R156 27
+0.3V
+0.1V
Q104
C112 22
330
C111
R112 56
R159 10
R304 100K
FLYBACK T100
14.5KV
HORZ. OUTPUT
R136 10
100 VPP
C113 4.7 B.P.
80 VPP
Q108
R152
2.5 VPP
D108 IN 4936
R151 470
C140 330
HDY
1.3 VPP
C136 .047
C107
HORZ DRIVER
D106 IN 4936
R130 15
C121 470
LIN
WIDTH
L102
L101
B+
C114 330
C200 .001
R201 2.7M
R203 220K
D105
(2) IN4007
C123 .01
350 VPP
R200 100K
FOCUS VR200 MEG
R202 470K
C124 .01
C201 .001
(2) IN4007 D104
R128 464K
+48V
R160 100
D103 MR818
R121 10
+48V
C115 1
100K
(2) IN 4007
ISOLATED DAG GROUND
R300 18
B+
R116 470
R115 330
.0033
C108
1000 C106
VERT BIAS
R110 2.7K
6.5
Q103
C110 .47
Q102
+5.7V
+5.4V
+6V
16 VPP
R109 4.7K
18 VPP
Q101
VDY
R106 470
C107 .01
Q100
+0.2V
C109 .0033
C100 1000
3 VPP
R158 18
R100 2.7
TANT C101
R102 2.2K
25 VPP
•ALL DC VOLTAGES MEASURED WITH 20K Ω VOLT VOM.
•ALL AC VOLTAGES MEASURED ON OSCILLOSCOPE WITH 10x1 PRORE.
COMPUTRON DISPLAY SYS.
SCHEMATIC DIAGRAM
9000-0163

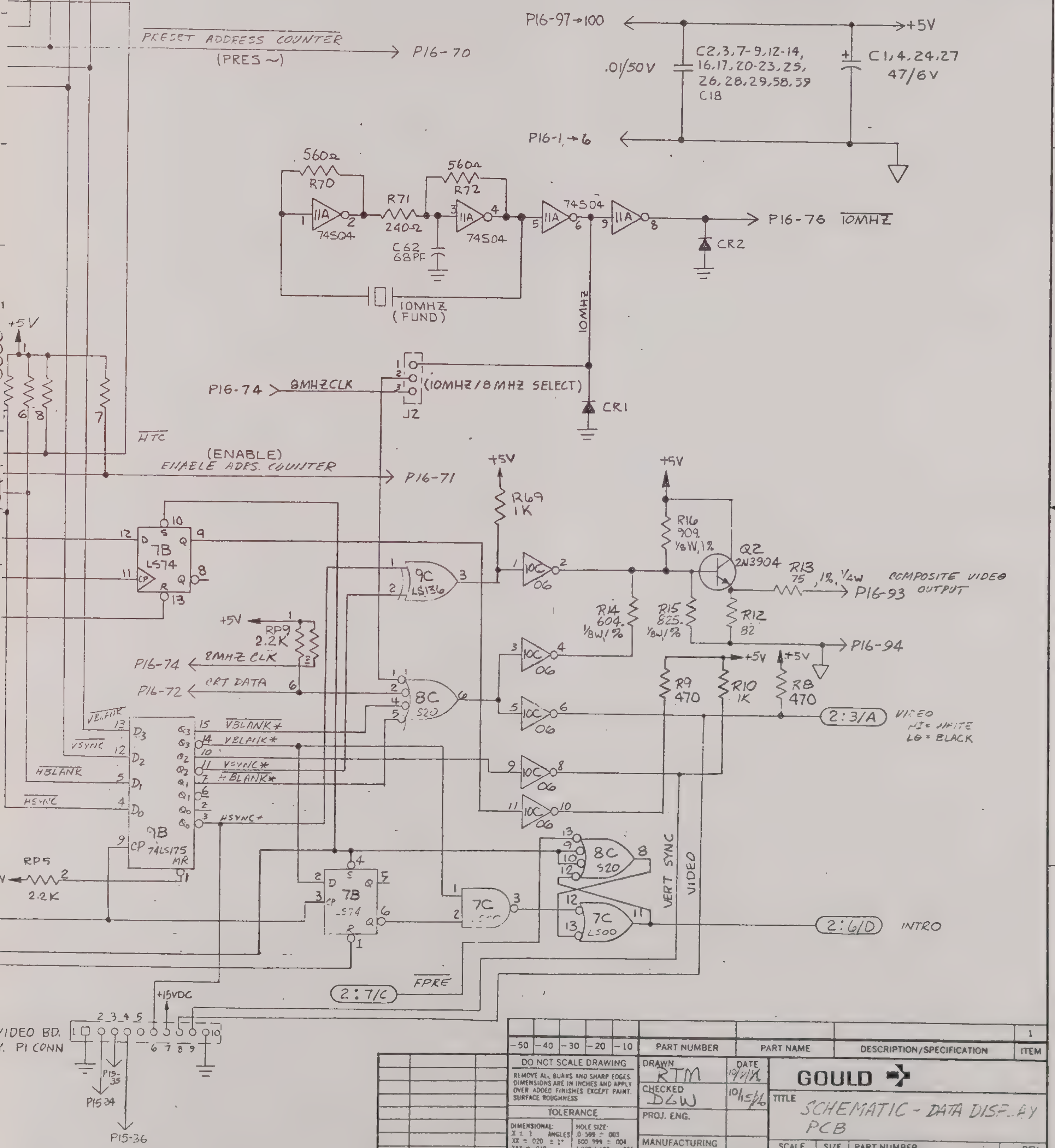

2:3/D
50 HZTC
7C
LS00
LS14
VTC
VERTICAL PROC.
8B
256×4 PROM
CS2
CS1
A7 A6 A5 A4 A3 A2 A1 A0
O4 O3 O2 O1
7A
LS161
TC
P3 P2 P1 P0
Q3 Q2 Q1 Q0
PE
CP
CEP CET MR
RP1
2.2K
+5V
2:4/D
1/2 MHZ
R5
470
E1
W1
150HZ
E2
Preset to -112 lines
+128
240
"0"
"1"
8A
HORIZONTAL PROC.
10B
256×4 PROM
9A
RP6
2.2K
E6 E4 E8
ES E5 E3 E0
NOTE:
SYNC CIRCUIT CONN.
TO P.S.
J1
R1
2.2K
10A
R2
2.2K
RP9
2.2K
R26
220
R27
330
1/2 MHZ CLOCK
P16-69
B RESET
P16-15
P16-16
GND #
RESET
2:31C
4:21C

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTOR VALUES ARE IN OHMS, 1/4W, ±5%.
2. ALL CAPACITOR VALUES ARE IN MICRO FARADS.

REVISIONS

ZONE	REV	ECO#	DESCRIPTION		DWN	CHKD	DATE
	50	5465	PILOT REL PER ECO	10/8/86	RTM	DGW	
	51	5490	REVISED PER ECO	10/22/86	RTM		
	52	5520	REV ROLL ONLY	12/16/86	MM	DGW	
	53	5534A	REV ROLL ONLY	1/6/87	MM	DGW	
	54	5557	REV ROLL ONLY	1/29/87	MM	RTM	
	A	5588	REV ROLL ONLY	2-18/87	MM	RTM	
	B	5650	REVISED PER ECO	4-29-87	MM	DGW	
	D	5806	REVISED PER ECO	8/26/87	MM	DGW	



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE: DIMENSIONAL: X ± .1, XX ± .020, XXX ± .010; ANGLES ± 1°; HOLE SIZE: 0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

ENG SERV. | DATE

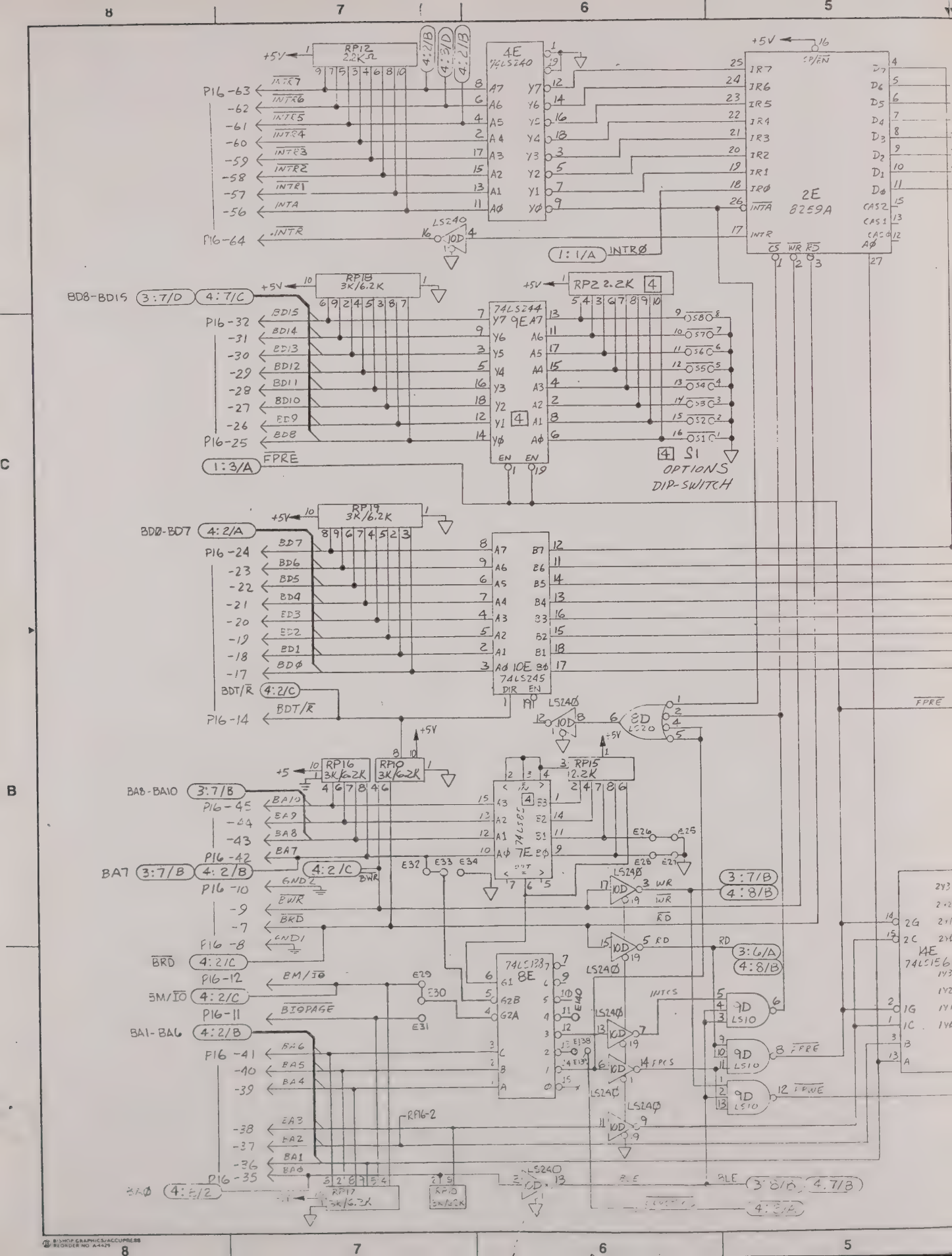
DRAWN: RTM — DATE: 10/3/86
CHECKED: DGW — 10/15/86
PROJ. ENG.
MANUFACTURING
QUALITY ASSUR

GOULD

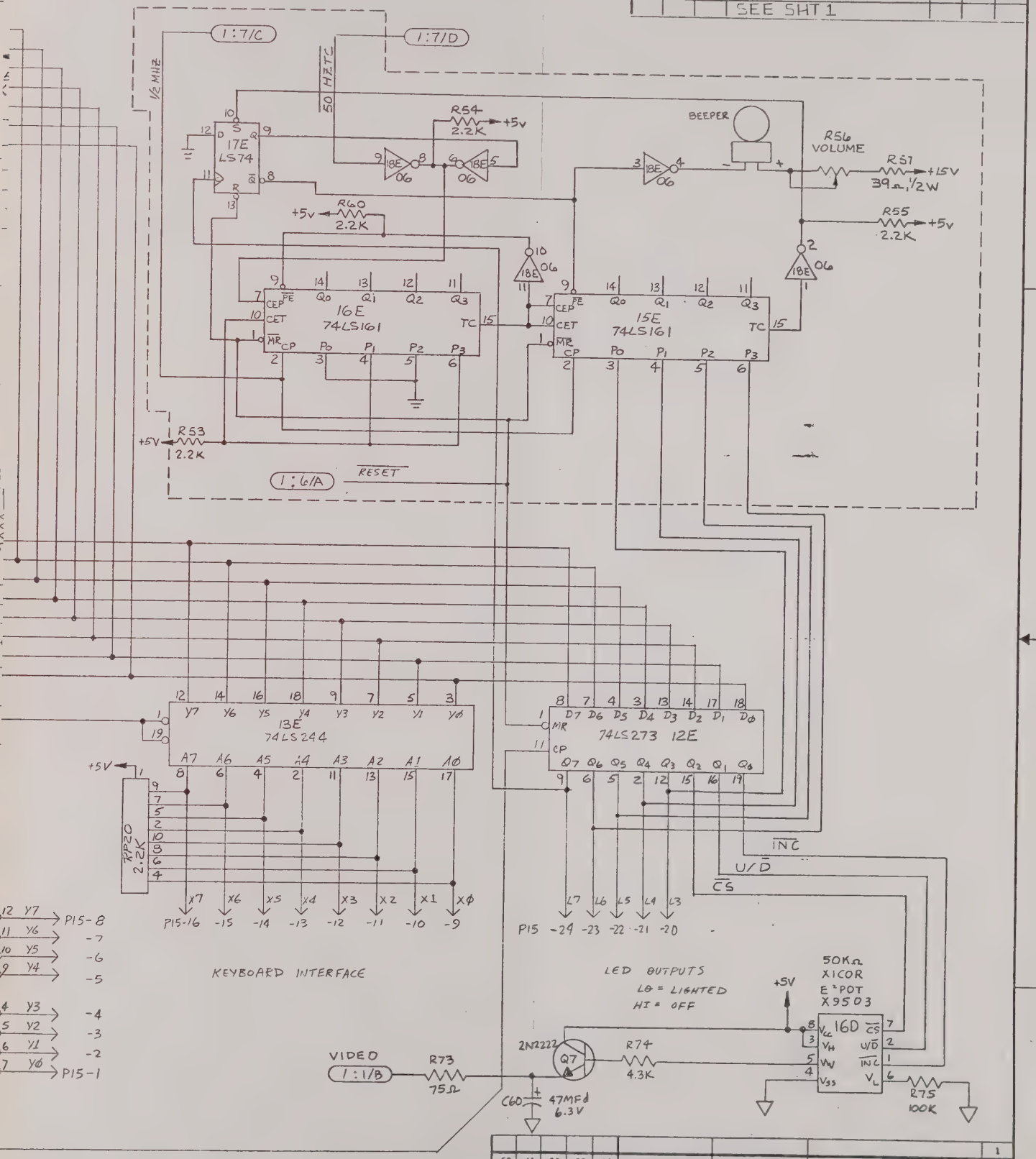
TITLE: SCHEMATIC - DATA DISPLAY PCB

SCALE | SIZE: D | PART NUMBER: 0121-0201 | REV: D

CODE | SHEET 1 OF 4


RP12 2.2K
4E 74LS240
2E 8259A
+5V
P16-63 INTR7
P16-62 INTR6
P16-61 INTR5
P16-60 INTR4
P16-59 INTR3
P16-58 INTR2
P16-57 INTR1
P16-56 INTA
P16-64 INTR
LS240
1:1/A INTRØ
RP18 3K/6.2K
RP2 2.2K
74LS244
BD8-BD15
P16-32 BD15
P16-31 BD14
P16-30 BD13
P16-29 BD12
P16-28 BD11
P16-27 BD10
P16-26 BD9
P16-25 BD8
1:3/A FPRE
4 S1 OPTIONS DIP-SWITCH
RP19 3K/6.2K
BDØ-BD7
P16-24 BD7
P16-23 BD6
P16-22 BD5
P16-21 BD4
P16-20 BD3
P16-19 BD2
P16-18 BD1
P16-17 BDØ
BDT/R
P16-14 BDT/R
74LS245
LS240
8D LS20
RP16 3K/6.2K
RP0 3K/6.2K
RP15 2.2K
BA8-BA10
P16-45 BA10
P16-44 BA9
P16-43 BA8
P16-42 BA7
BA7
P16-10 GND2
P16-9 BWR
P16-7 BRD
P16-8 GND1
BRD
P16-12 BM/IO
BM/IO
P16-11 BIOPAGE
BA1-BA6
P16-41 BA6
P16-40 BA5
P16-39 BA4
P16-38 BA3
P16-37 BA2
P16-36 BA1
P16-35 BAØ
74LS138 8E
74LS86
9D LS10
RP17 3K/6.2K
RP0 3K/6.2K
RP16-2
3:7/B 4:8/B
3:6/A 4:8/B
3:8/B 4:7/B
4:8/A
FPRE
RD
WR
IOWC
IRQS
BLE

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



−50	−40	−30	−20	−10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: .0 .599 ± .003; 600 .999 ± .004; 1.000 1.499 ± .005

DRAWN	DATE 3/6/86
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	

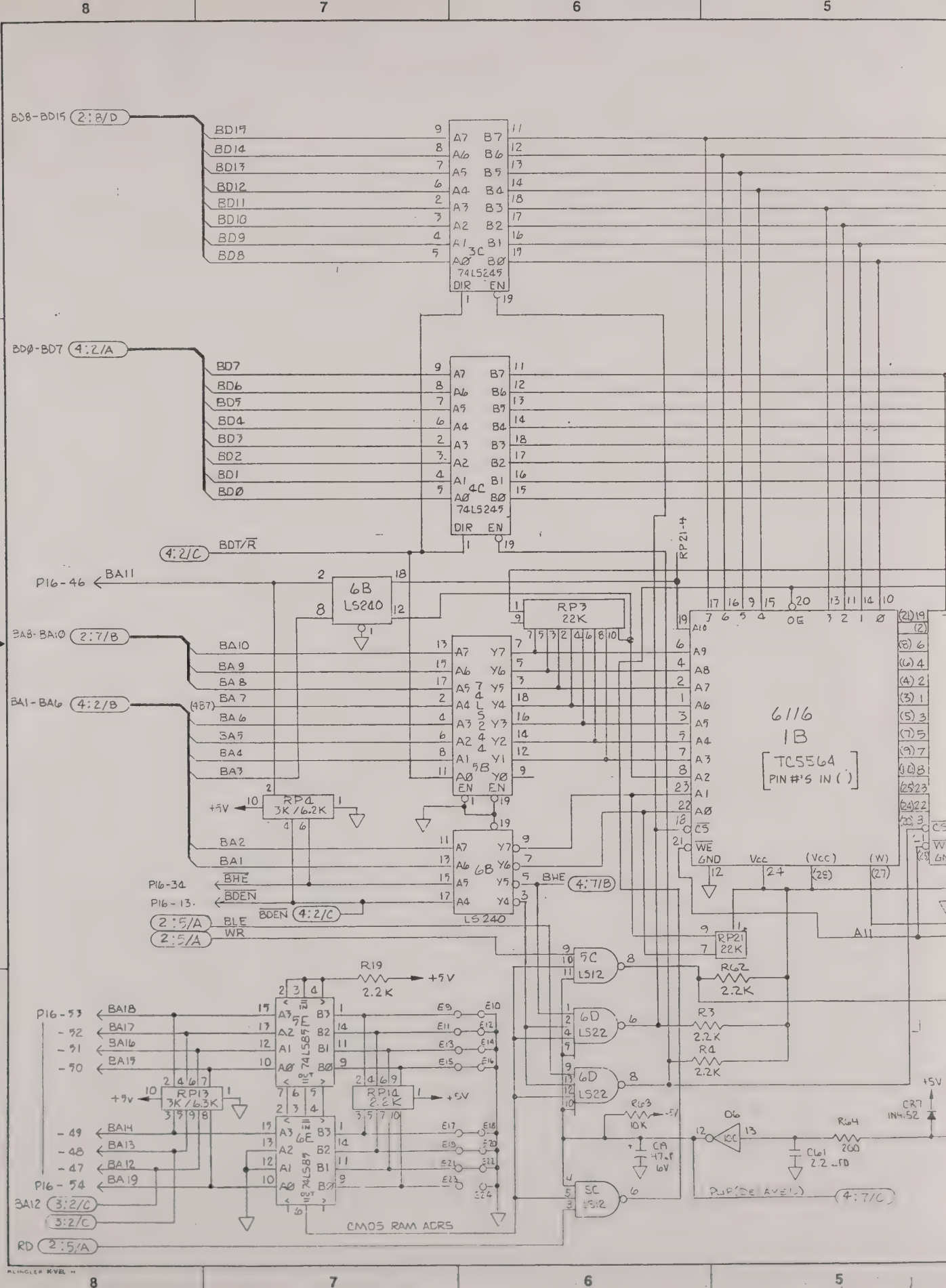
GOULD

TITLE SCHEMATIC
DATA DISPLAY PCB

SCALE	SIZE	PART NUMBER	REV
	D	0121-0201	D

CODE SHEET 2 OF 4

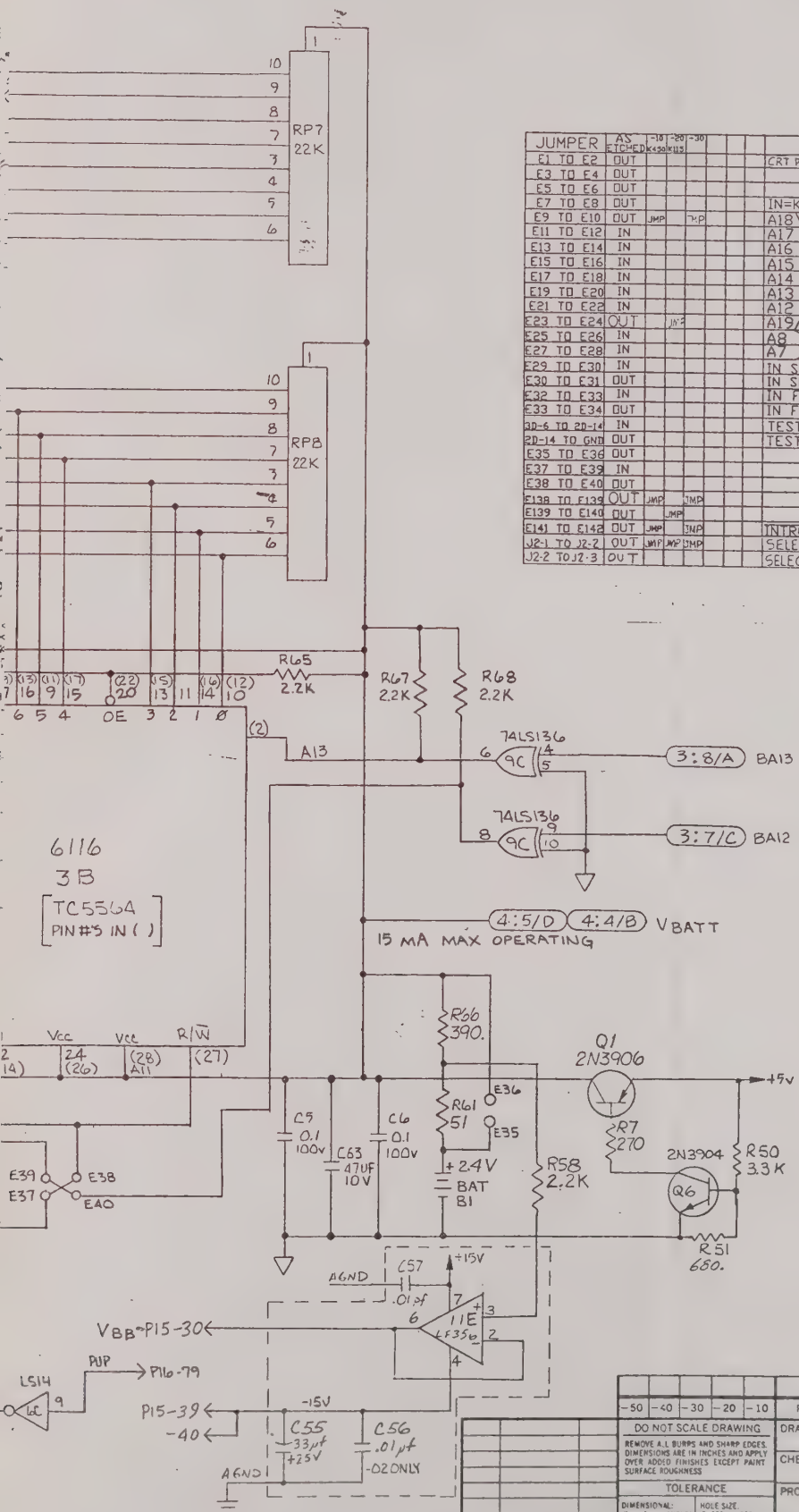
DASH NO.	NUMBER NEXT ASSEMBLY	QTY	ENG. SERV.	DATE



8
7
6
5
BD8-BD15 2:8/D
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
3C
74LS245
DIR EN
BDØ-BD7 4:2/A
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BDØ
4C
74LS245
DIR EN
4:2/C
BDT/R̄
P16-46
BA11
6B
LS240
RP3
22K
RP21-4
BA8-BA10 2:7/B
BA10
BA9
BA8
BA7
BA6
BA5
BA4
BA3
BA1-BA6 4:2/B
(487)
74LS244
5B
RP4
3K/6.2K
+5V
BA2
BA1
6B
LS240
P16-34
BHE
P16-13
BDEN
BDEN 4:2/C
2:5/A
BLE
2:5/A
WR
BHE 4:7/B
6116
1B
TC5564
PIN #'S IN ( )
OE
CS
WE
GND
Vcc
(Vcc)
(W)
A11
RP21
22K
5C
LS12
R62
2.2K
6D
LS22
R3
2.2K
R4
2.2K
R19
2.2K
+5V
P16-53
BA18
-52
BA17
-51
BA16
-50
BA15
5E
74LS85
RP13
3K/6.3K
RP14
2.2K
-49
BA14
-48
BA13
-47
BA12
P16-54
BA19
BA12 3:2/C
3:2/C
RD 2:5/A
CMOS RAM ADRS
R63
10K
-5V
C19
47.8
6V
D6
10C
R64
200
C61
2.2 µFD
CR7
1N4152
PUP (DELAYED)
4:7/C

DWG. NO. 0121-0201 SH 3 REV D

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



JUMPER	AS ETCHED	-10 K450	-20 K115	-30	DESCRIPTION	SCHEM SHT. #
E1 TO E2	OUT				CRT PROM VERT SCAN RATE IN-50HZ OUT-60HZ	1
E3 TO E4	OUT				NOT USED	1
E5 TO E6	OUT				NOT USED	1
E7 TO E8	OUT				IN=K500 HORIZ SCAN OUT=K450	1
E9 TO E10	OUT	JMP		JMP	A18	
E11 TO E12	IN				A17	
E13 TO E14	IN				A16	
E15 TO E16	IN				A15 K450 CMOS RAM ADDRESS SELECTION	3
E17 TO E18	IN				A14	
E19 TO E20	IN				A13	
E21 TO E22	IN				A12	
E23 TO E24	OUT		JMP		A19	
E25 TO E26	IN				A8 K500 MEM MAPPED I/O ADDRESS DECODE	2
E27 TO E28	IN				A7	
E29 TO E30	IN				IN SELECTS I/O MAPPED I/O K101	2
E30 TO E31	OUT				IN SELECTS MEM MAPPED I/O K500	2
E32 TO E33	IN				IN FOR K450	2
E33 TO E34	OUT				IN FOR K500	2
3D-6 TO 2D-14	IN				TEST FIX FOR K450/K115	4
2D-14 TO GND	OUT				TEST FIX FOR K450 K115	4
E35 TO E36	OUT					3
E37 TO E39	IN					3
E38 TO E40	OUT					3
E138 TO E139	OUT	JMP		JMP		2
E139 TO E140	OUT		JMP			2
E141 TO E142	OUT	JMP		JMP	INTRG CONNECTION	4
J2-1 TO J2-2	OUT	JMP	JMP	JMP	SELECTS 10MHz FOR 60Hz VERT. SCAN	1
J2-2 TO J2-3	OUT				SELECTS 8MHz FOR 50Hz VERT. SCAN	1

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

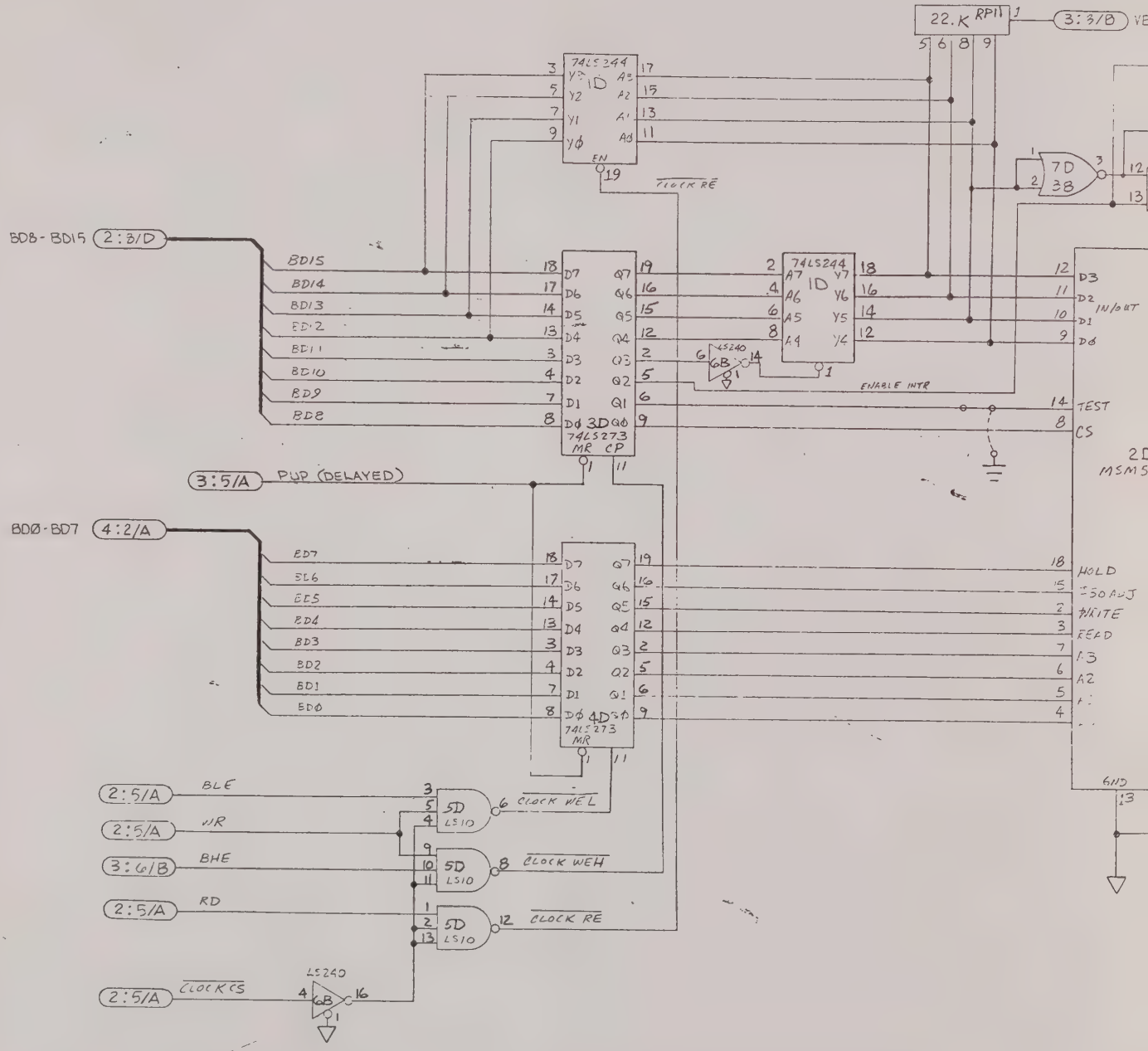
DIMENSIONAL: X = .1 ANGLES XX = .020 ± 1° XXX = .010

HOLE SIZE: 0 599 = .003 600 999 = .004 1 000 1 499 = .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

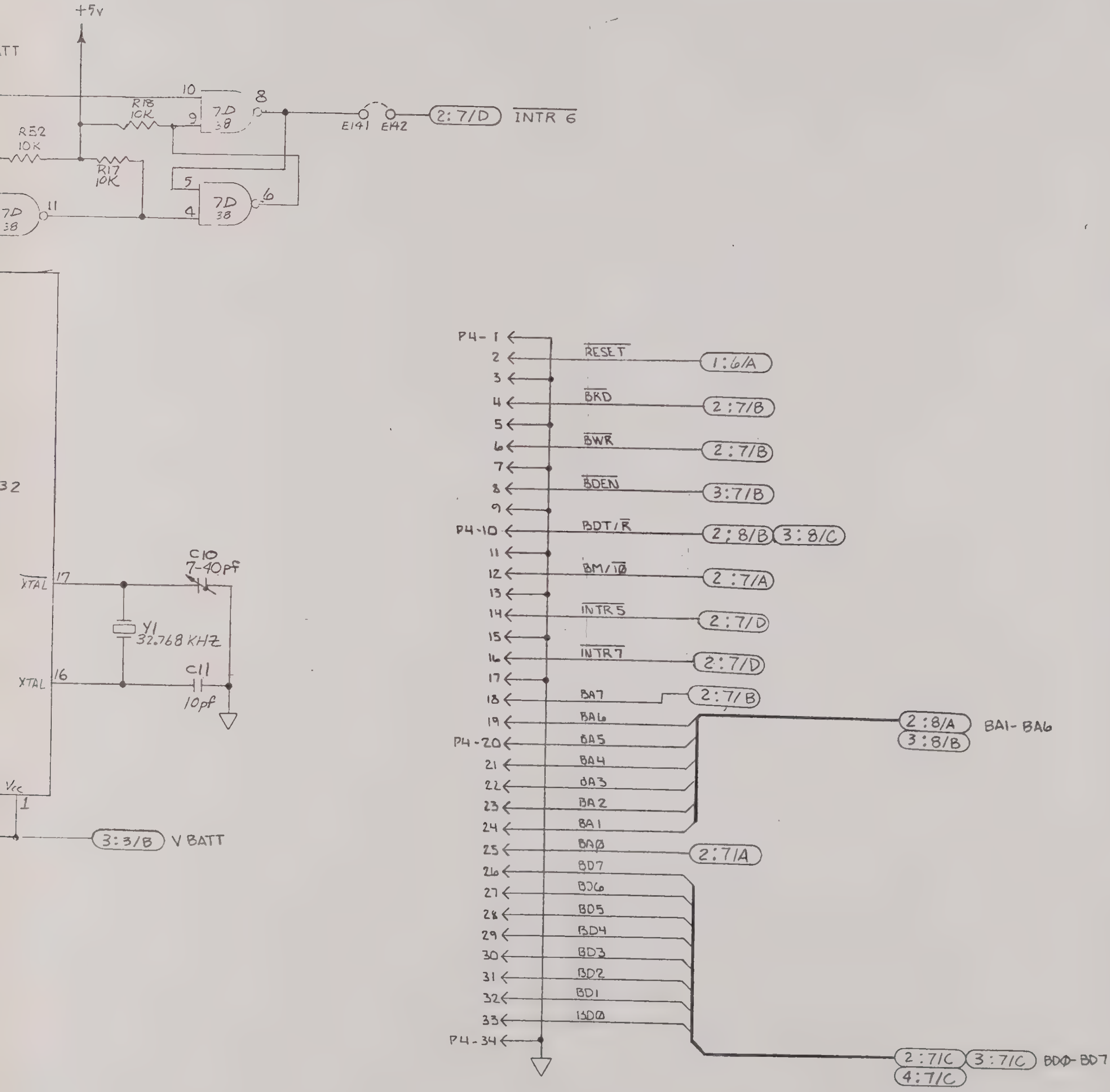
ENG. SERV. DATE

DRAWN	DATE 3/13/86	GOULD
CHECKED		TITLE SCHEMATIC DATA DISPLAY, PCB
PROJ. ENG.		
MANUFACTURING		SCALE / SIZE D / PART NUMBER 0121-0201 / REV D
QUALITY ASSUR		CODE / SHEET 3 OF 4



© SHOP GRAPHICS/ACCUPRESS
REORDER NO A-4429

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
			SEE SHT 1			



-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X = .1 .XX = .020 .XXX = .010 ANGLES ± 1°

HOLE SIZE: 0 .599 = .003; .600 .999 = .004; 1.000-1.499 = .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

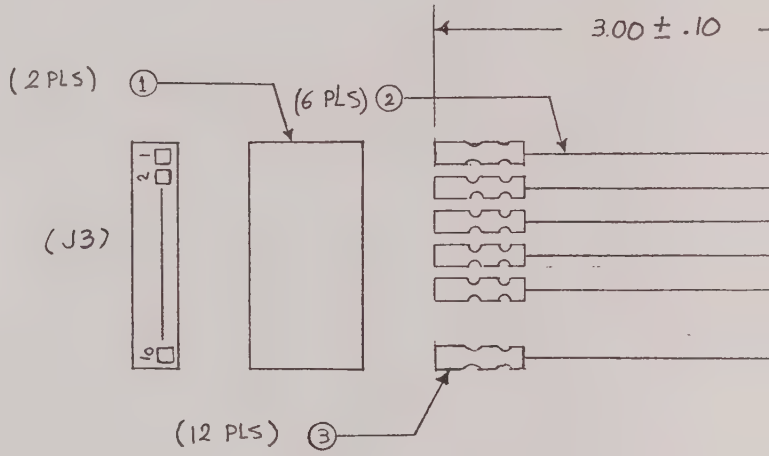
		DATE
DRAWN		3/10/86
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		
ENG. SERV.		DATE

GOULD

TITLE SCHEMATIC - DATADISPLAY PCB

SCALE	SIZE	PART NUMBER	REV
	D	0121-0201	D

CODE - SHEET 4 OF 4



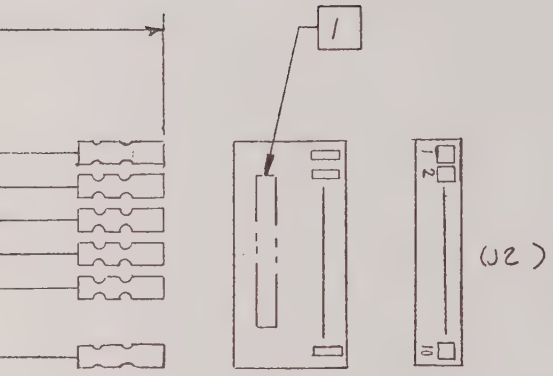
WIRE CHART	
FROM	TO
J3-1	J2-1
-2	-2
-3	-3
-4	-4
-5	-5
J3-10	J2-10

-10	0121-0200-20	K115
-10	0121-0200-10	K450
DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

-03
QT
UNLES
DIMEN
TOLE
FRACT
MATE
FINISH

DIETERICH POST REORDER NO. 84490

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5465	PILOT REL PER ECO 10-7-86	RTM	DGW	10/8/86
	A	5650	REVISED PER ECO 4/29/87	MM	DGW	4/30/87



NOTES: UNLESS OTHERWISE SPECIFIED

1. STAMP PART NO. 0121-0205, DASH NO, AND REV. LEVEL WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. MANUFACTURE PER GOULD WORKMANSHIP STANDARD 87000012.

0121-0205

-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
PER ASSY				

PARTS LIST

OTHERWISE SPECIFIED
IONS ARE IN INCHES
NCES ARE:
ONS DECIMALS ANGLES
XX ± ±
XXX ±

AL

O NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN H-Sheyer	10/6/86
CHECKED DGWRIGHT	10/8/86
PROJ ENG	

GOULD Electronics

TITLE: ASSY. CBL, COMP 115 DMX-7 TO DISPLAY PCB

SIZE	DWG. NO.	REV.
C	0121-0205	A

SCALE NONE | MODEL K115, K450 | SHEET 1 OF 1

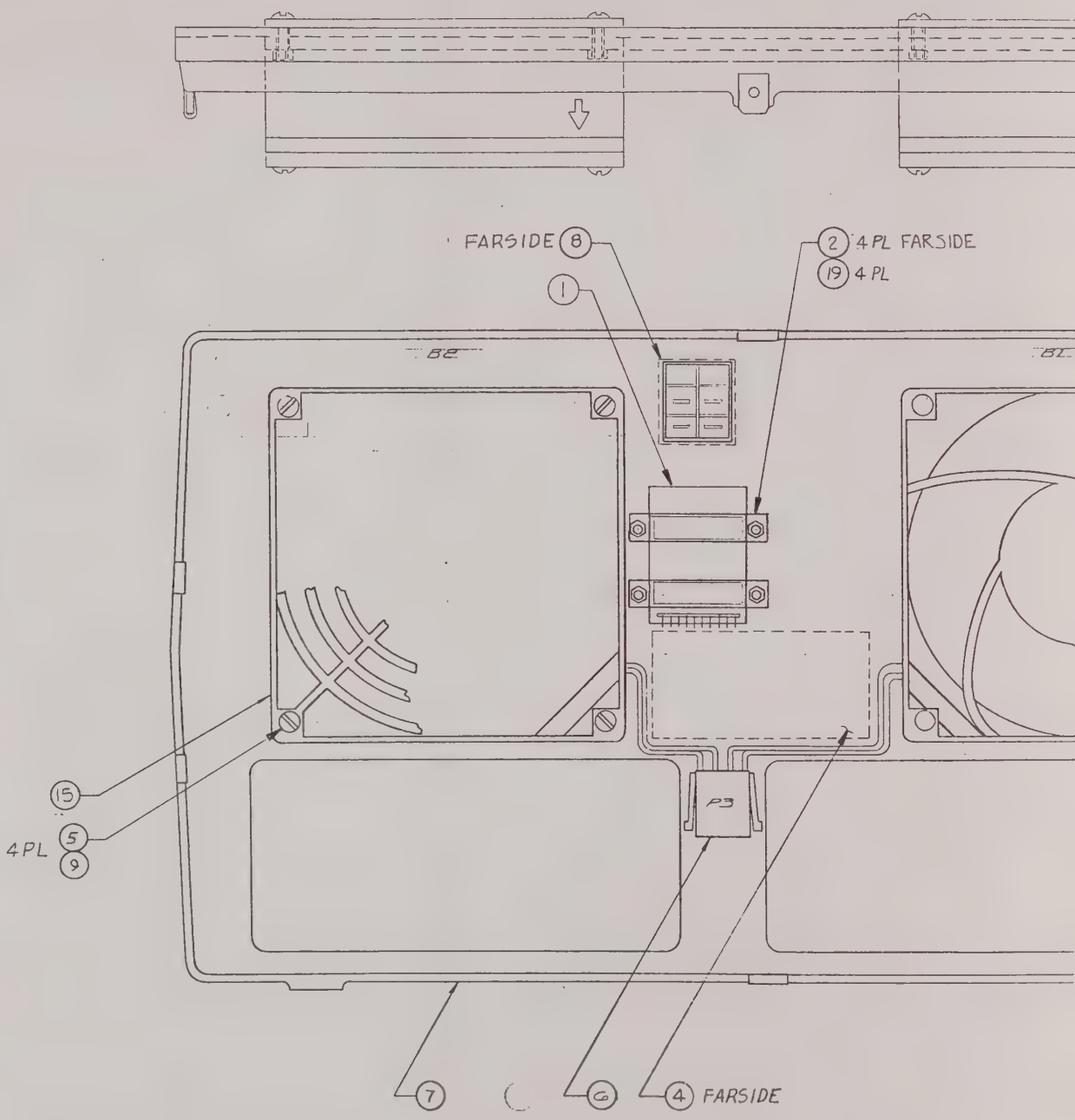
2 1

BILL OF MATERIAL

AS OF 10/30/87

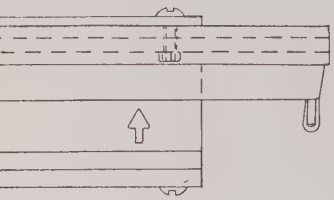
0121-0205-10 ASSY,CBL,COMP115MX-7 TO DSPLY
MODEL: K450/K115

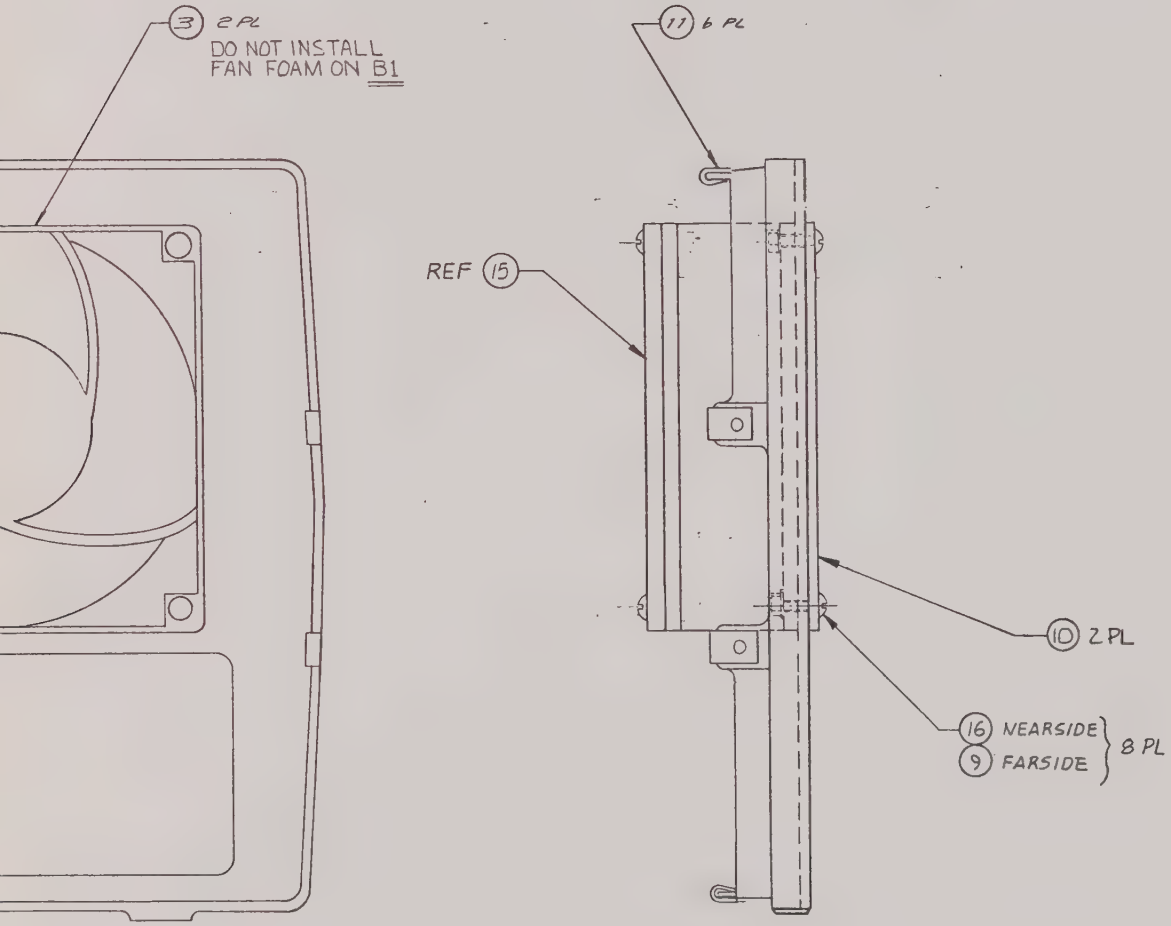
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
1	6000-0605-10	CONN, 10 PIN HOUSING, SGL. ROW	2	EA	
2	7150-0024-10	WIRE,PVC,24 AWG,BLK	2	FT	
3	6000-0188-10	CONN TERMINAL 22-30 AWG	12	EA	


FARSIDE 8
1
2 4 PL FARSIDE
19 4 PL
B2
B1
P3
15
4 PL 5
9
7
6
4 FARSIDE

0121-0405

REVISIONS						
ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	DATE
	50	5648	PILOT RELEASE 4/29/87	MM	DW	9/04/87





-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER AGREED FINISHES EXCEPT PAINT SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; XX ± .020 ± 1°; XXX ± .010

HOLE SIZE: 0 599 ± .003; 600 999 ± .004; 1.000 1.499 ± .005

DRAWN REVISED	DATE
RTM	1/26/87
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	

GOULD biomation

TITLE: ASSEMBLY- REAR CASTING K450B

SCALE	SIZE	PART NUMBER	REV
FULL	D	0121-0405	50

CODE K450B SHEET 1 OF 1

-10		1
DASH NO	NUMBER NEXT ASSEMBLY	QTY

ENG. SERV. DATE

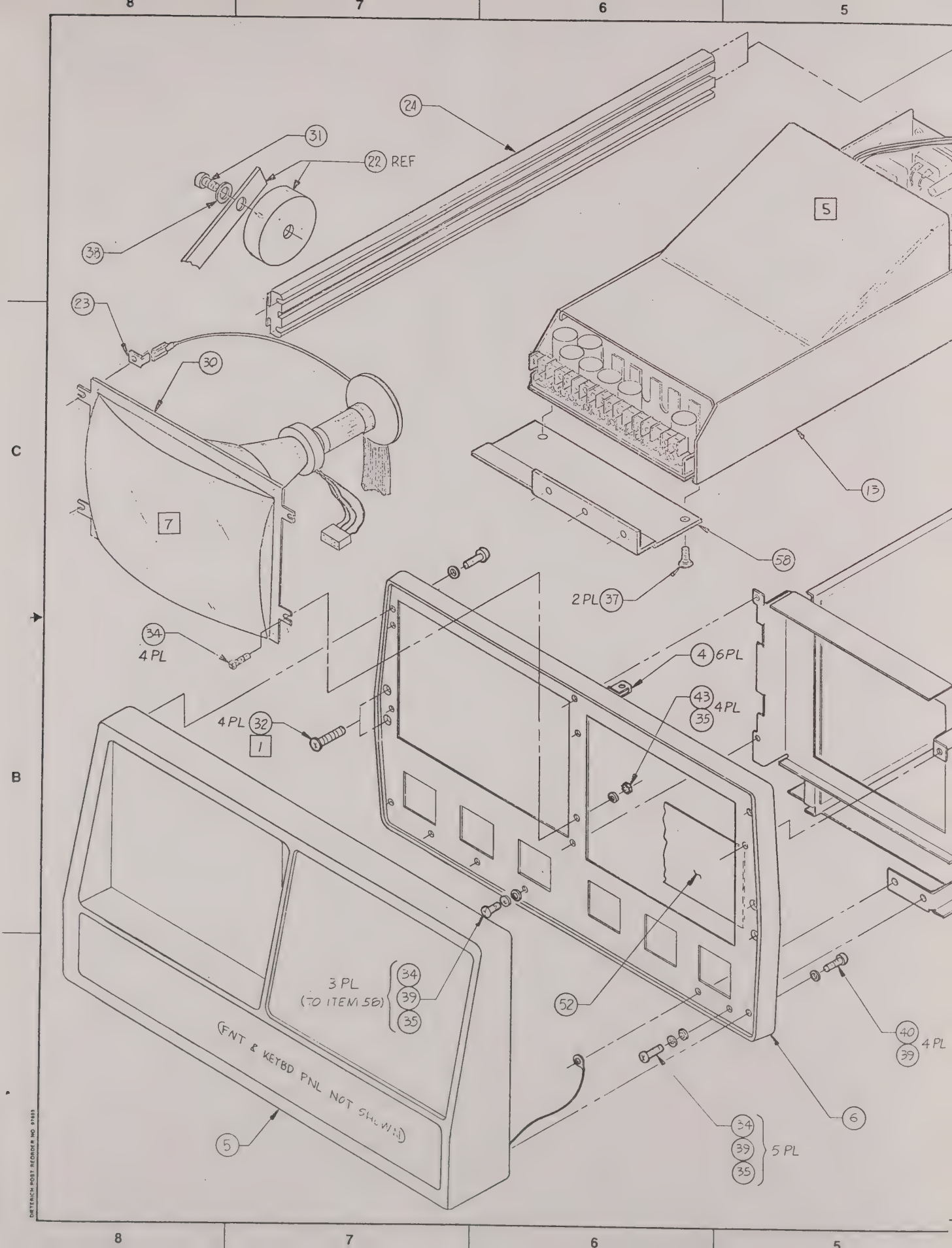
4 3 2 1

BILL OF MATERIAL

AS OF 10/30/87

0121-0405-10 ASSY,REAR,CASTING,K450B
MODEL: K450B

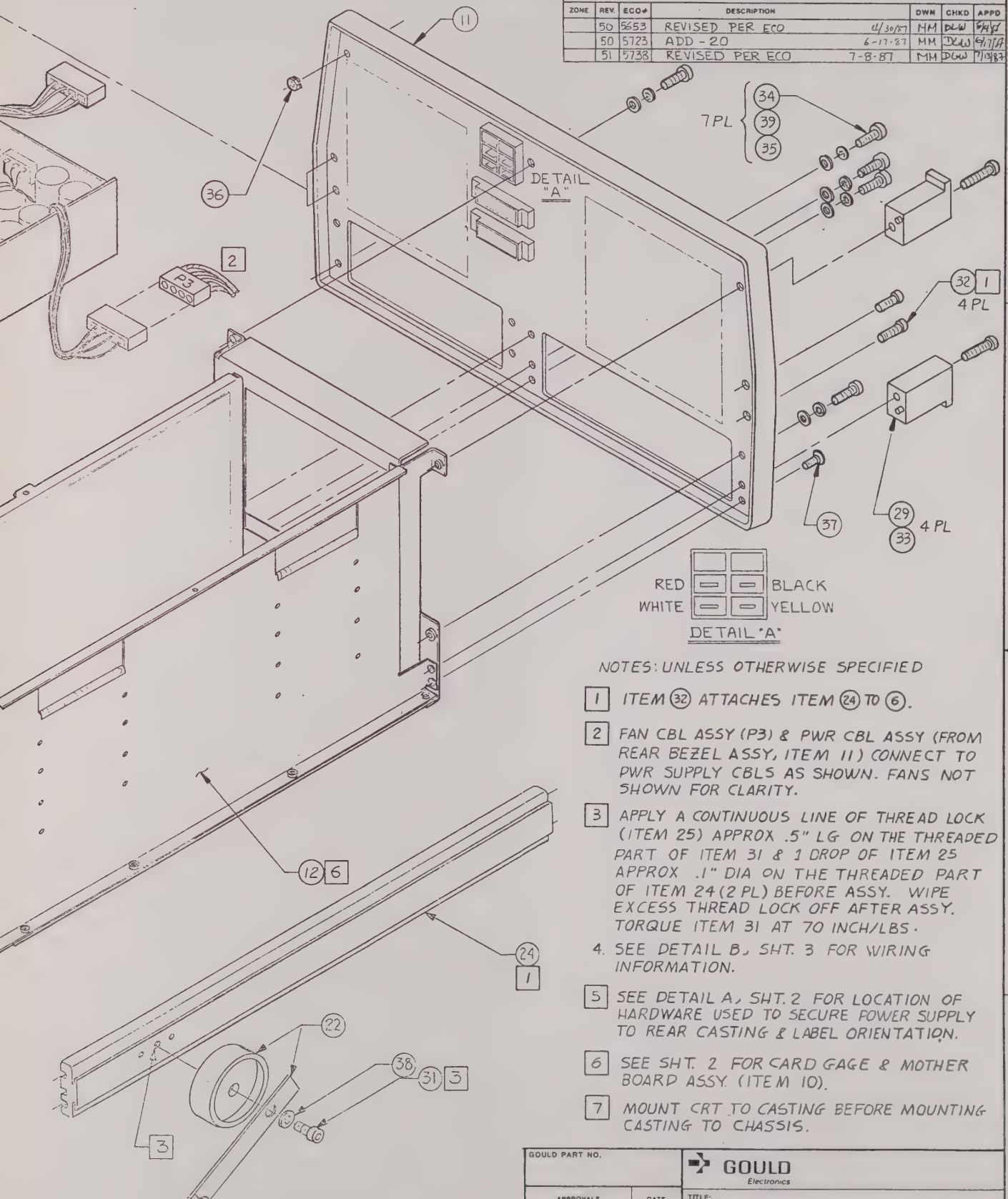
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0405	DWG,ASSY,REAR,CASTING,K450B	0	EA	REF
1	0121-0475-10	ASSY,PCB,PROBE TEST,K450B	1	EA	
2	7011-1440-20	SCR,X,PH,4-40 X 5/8,STZN	4	EA	
3	2900-0003-10	FAN 115V 50/60HZ 4600X	2	EA	B1,B2
4	0121-0433-10	LABEL,WARNING/FCC,K450B	1	EA	
5	7011-1632-24	SCR,X,PH,6-32 X 3/4,STZN	4	EA	
6	0121-0082-10	ASSY CABLE, FAN K450	1	EA	
7	0285-0009-30	BEZEL,CASTING,REAR K450B	1	EA	
8	6600-0163-10	SWITCH,RKR,DPST,AC PWR,10 A	1	EA	
9	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	12	EA	
10	7000-0080-10	HDWR FAN GUARD	3	EA	
10	7000-0624-10	HDWR,FAN GUARD,RETAINER,MEDIA	2	EA	
11	7000-0334-10	HDWR "U" SPEED NUT FSTNR	6	EA	
15	7000-0625-10	HDWR,FAN GUARD WIRE FORM,4 1/2	1	EA	
16	7011-1632-28	SCR,X,PH,6-32 X 7/8,STZN	8	EA	
19	7071-1440-00	NUT,S-LOCK,4-40,STD,STZN	4	EA	


24
31
22 REF
38
23
30
5
7
13
58
2 PL 37
34
4 PL
4 6 PL
43
35
4 PL
4 PL 32
1
3 PL
(TO ITEM 58)
34
39
35
52
40
39
4 PL
6
34
39
35
5 PL
(FNT & KEYBD PNL NOT SHOWN)
5

DWG. NO.	SH.	REV.
0121-0406	1	51

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5653	REVISED PER ECO 4/30/87	MM	DLW	5/4/87
	50	5723	ADD - 20 6-17-87	MM	DLW	6/17/87
	51	5738	REVISED PER ECO 7-8-87	MM	DLW	7/13/87



RED BLACK
WHITE YELLOW
DETAIL "A"

NOTES: UNLESS OTHERWISE SPECIFIED

1. ITEM (32) ATTACHES ITEM (24) TO (6).
2. FAN CBL ASSY (P3) & PWR CBL ASSY (FROM REAR BEZEL ASSY, ITEM 11) CONNECT TO PWR SUPPLY CBLS AS SHOWN. FANS NOT SHOWN FOR CLARITY.
3. APPLY A CONTINUOUS LINE OF THREAD LOCK (ITEM 25) APPROX .5" LG ON THE THREADED PART OF ITEM 31 & 1 DROP OF ITEM 25 APPROX .1" DIA ON THE THREADED PART OF ITEM 24 (2 PL) BEFORE ASSY. WIPE EXCESS THREAD LOCK OFF AFTER ASSY. TORQUE ITEM 31 AT 70 INCH/LBS.
4. SEE DETAIL B, SHT. 3 FOR WIRING INFORMATION.
5. SEE DETAIL A, SHT. 2 FOR LOCATION OF HARDWARE USED TO SECURE POWER SUPPLY TO REAR CASTING & LABEL ORIENTATION.
6. SEE SHT. 2 FOR CARD GAGE & MOTHER BOARD ASSY. (ITEM 10).
7. MOUNT CRT TO CASTING BEFORE MOUNTING CASTING TO CHASSIS.

DASH NO.	NEXT ASSY	USED ON
10		K450P

FIRST APPLICATION

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

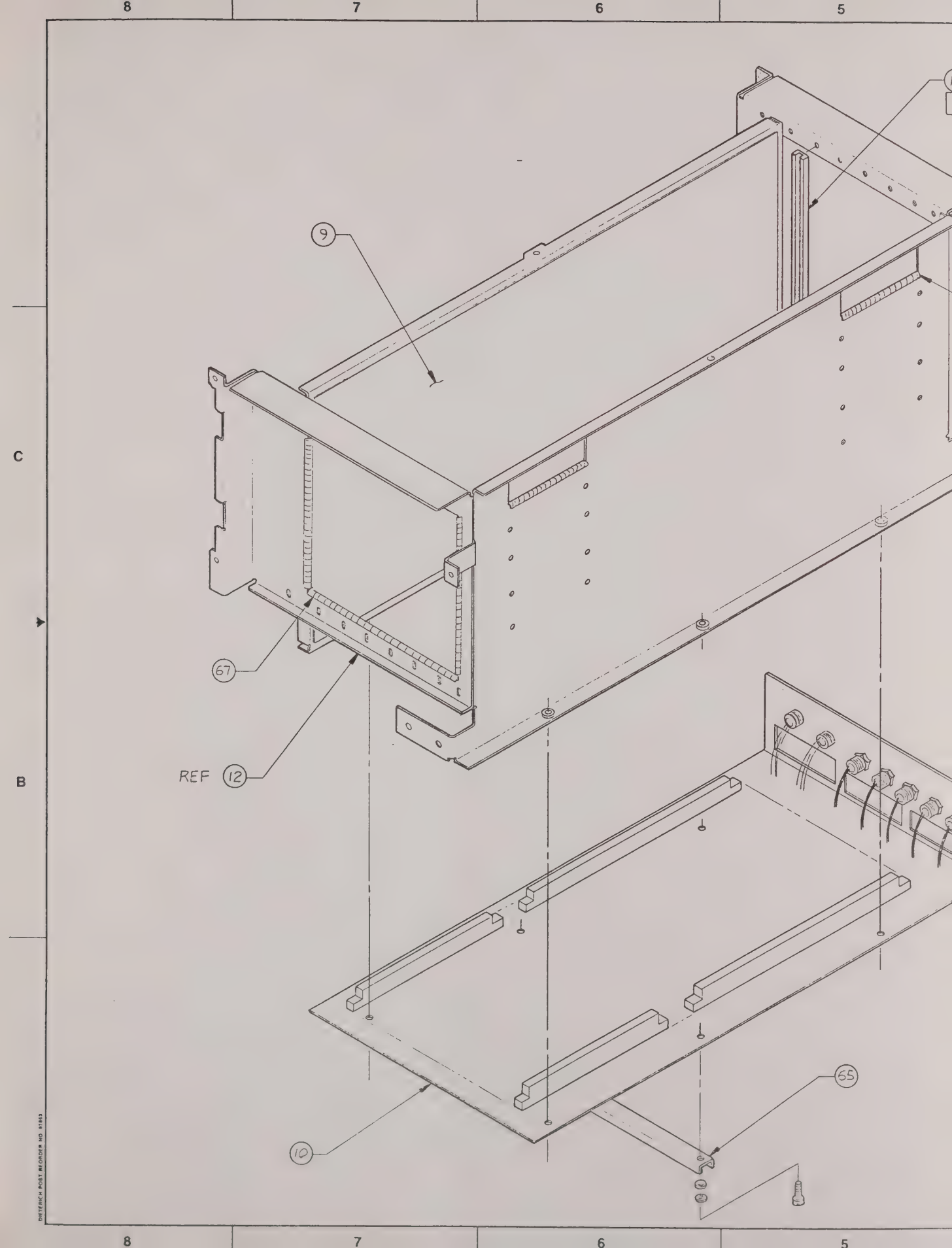
APPROVALS	DATE
DRAWN RTm	1/28/87
CHECKED DLW	5/4/87
PROJ ENG	

GOULD Electronics

TITLE: CHASSIS, TOP ASSEMBLY K450B

SIZE	DWG. NO.	REV
D	0121-0406	51

SCALE — MODEL K450B SHEET 1 OF 4


9
67
REF 12
10
65

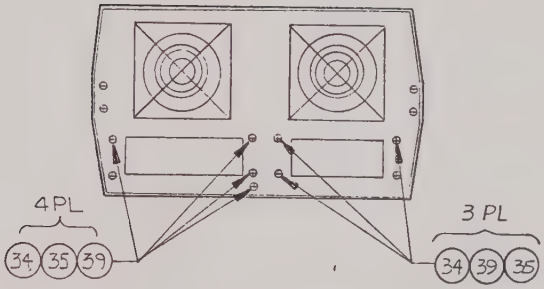
DWG. NO.	SH	REV
0121-0406	2	51

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD

16 PL

67



DETAIL A
REAR VIEW OF UNIT
(FROM SHT. 1)

NOTES: UNLESS OTHERWISE SPECIFIED

[1] HARDWARE SPECIFIED IS APPLICABLE TO OPPOSIDE END.

40
39
35
7 PL

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

DASH NO.	NEXT ASSY	USED ON
FIRST APPLICATION		

GOULD PART NO.

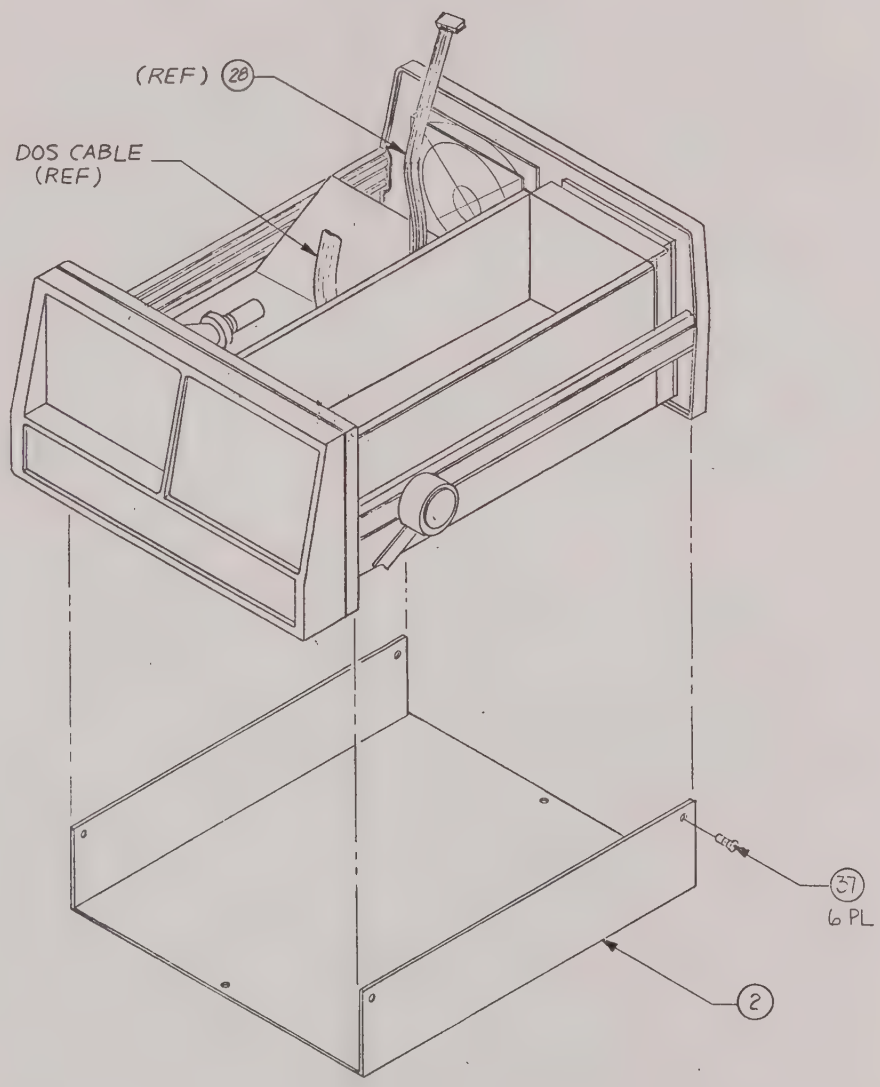
APPROVALS	DATE
DRAWN RTM	1/26/87
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: CHASSIS, TOP ASSEMBLY K450B

SIZE	DWG. NO.	REV
D	0121-0406	51

SCALE / MODEL K450B SHEET 2 OF 4



NOTES: UNLESS OTHERWISE SPECIFIED

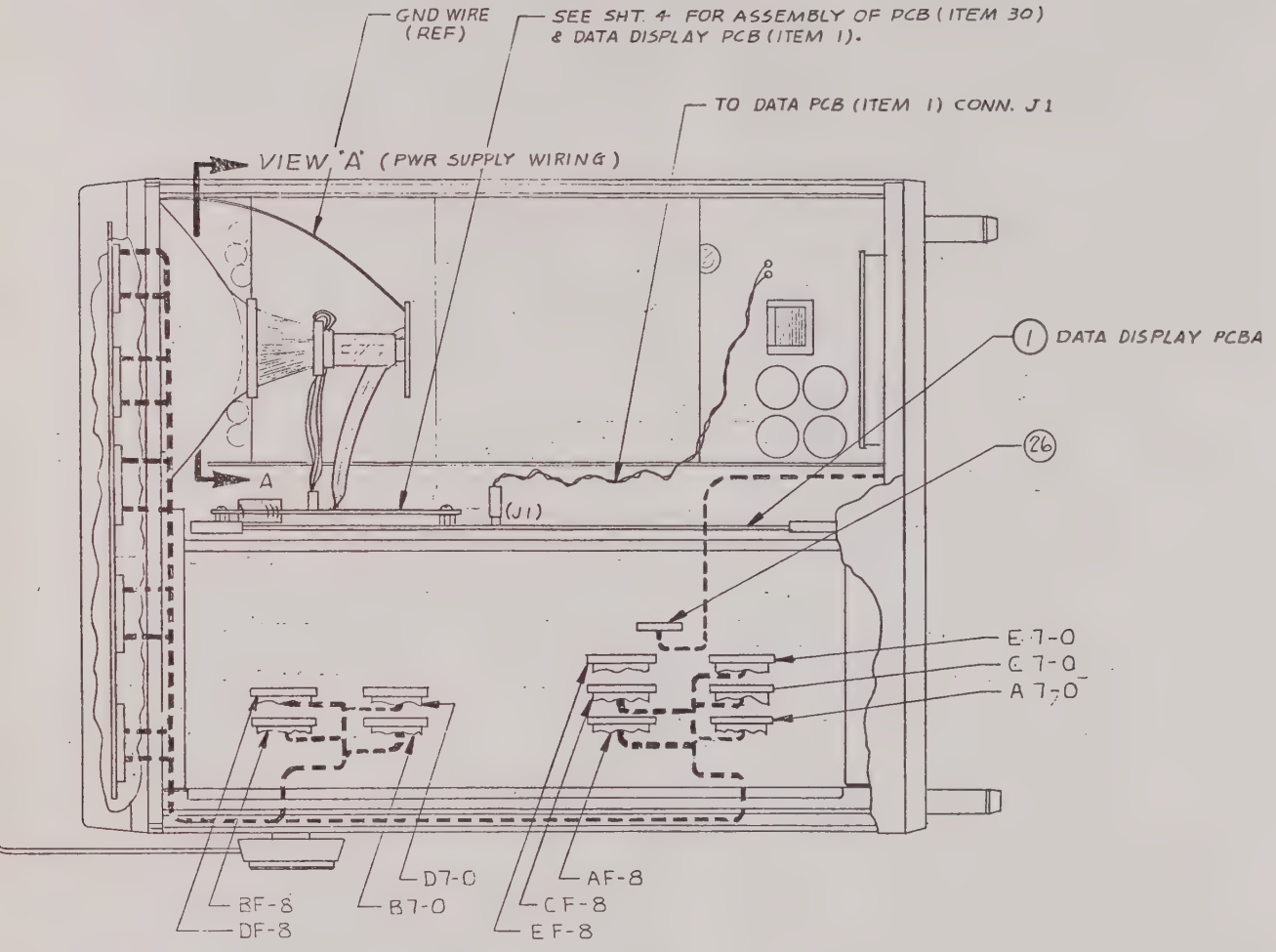
[1] NUMBER BESIDE "▷" INDICATES WIRE NO. FROM HARNESS 0121-0167-10 WHICH IS SOLDERED INTO CARD CAGE ASSEMBLY ITEM (12).

[2]

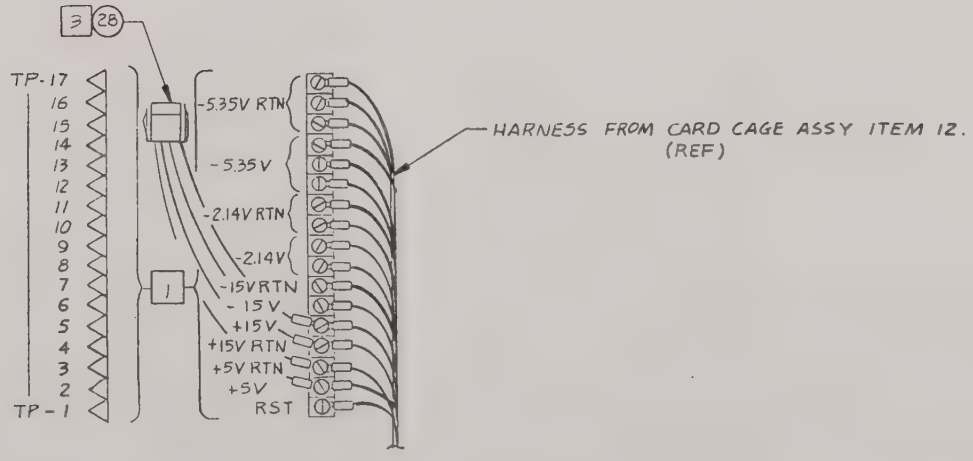
[3] WIRING CHART :

ITEM 28	
PIN NO	TP-
1	5
2	4
3	3
4	2

} LUGS OF ITEMS 28 TO BE UNDER HARNESS LUGS



DETAIL 'B' WIRING INFORMATION

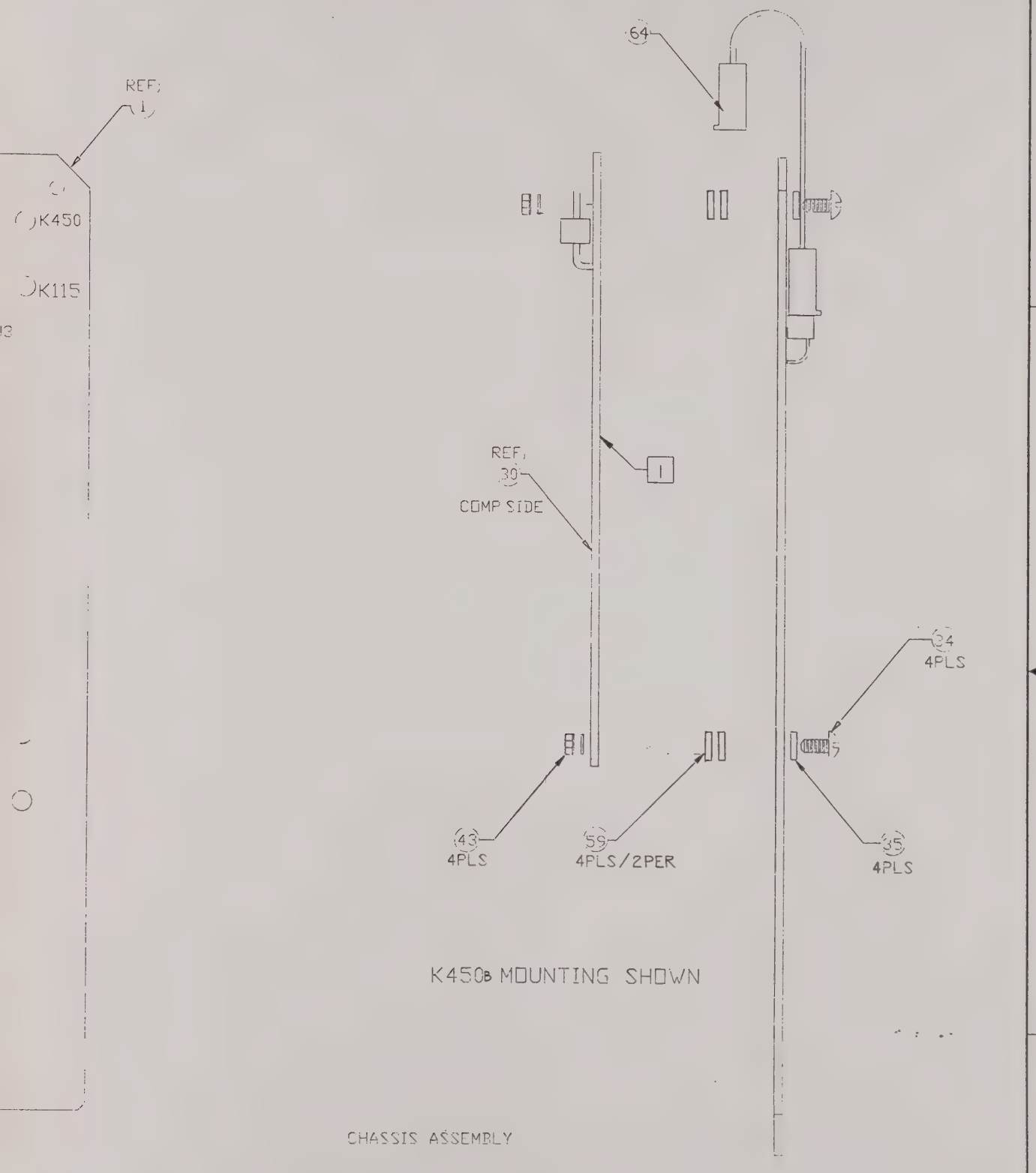


VIEW "A"
PWR SUPPLY WIRING

SIZE		DWG NO	REV
D	GOULD	0121-0406	51
		SHEET 3 OF 4	

4 3 2 1

REF; COMPONENT SIDE



K450B MOUNTING SHOWN

CHASSIS ASSEMBLY

VIDEO BOARD TO DATA DISPLAY BOARD

MOUNTING AND INTERCONNECT CABLE.

1 NOTE: BE SURE THE SOLDER SIDE LEADS OF THE COMPUTRON VIDEO BOARD DO NOT TOUCH THE SURFACE OF THE DATA DISPLAY BOARD.

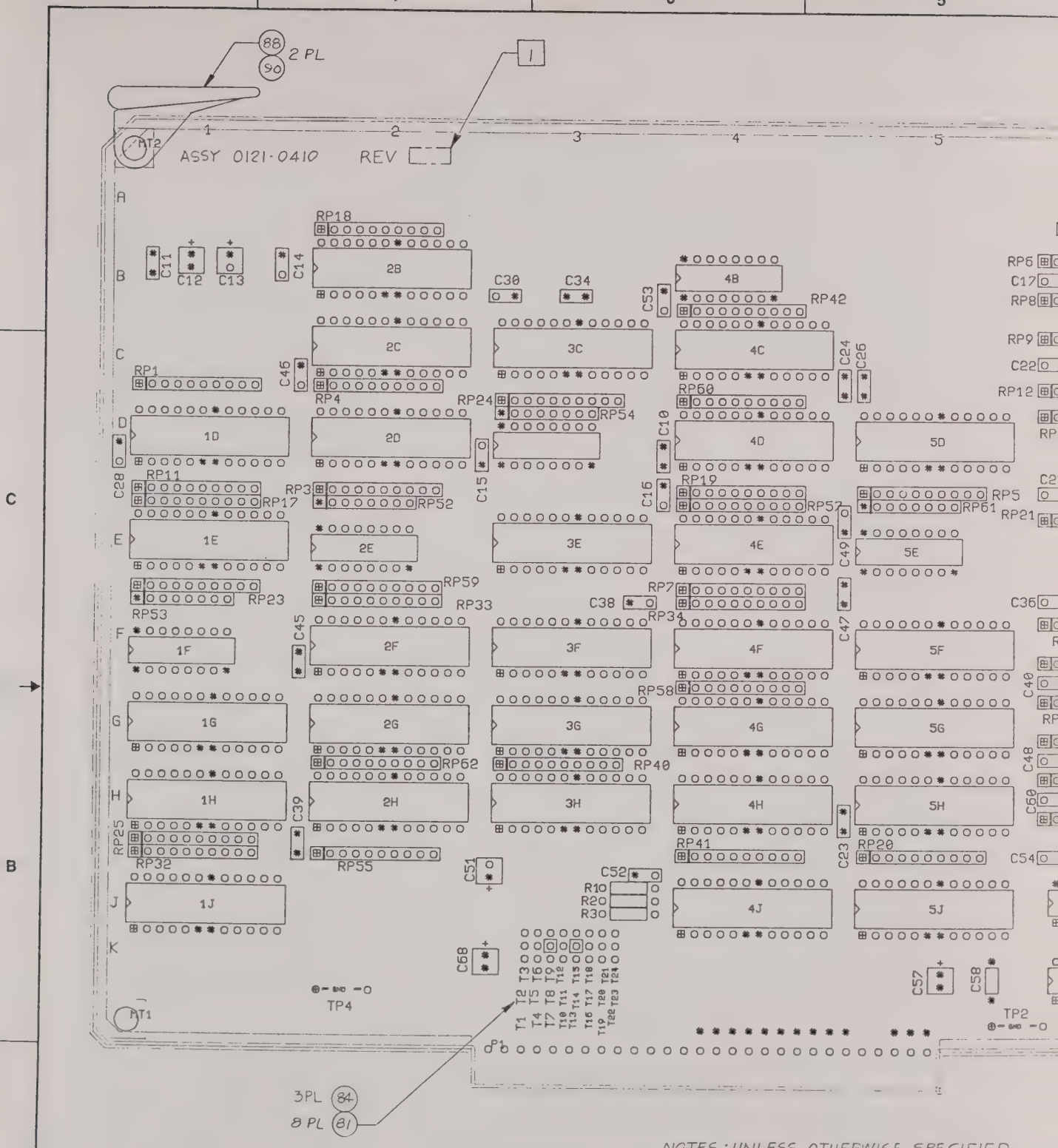
SIZE		DWG. NO.	REV.
D	GOULD Electronics	0121-0406	51
		SHEET 4 OF 4	

BILL OF MATERIAL

AS OF 10/30/87

0121-0406-10 ASSY,CHASSIS,K450B
MODEL. K205

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0406	DWG,ASSY,CHASSIS,K450B	0	EA	REF
1	0121-0200-30	ASSY,PCB,DATA DISPLAY,K450B	1	EA	
2	0121-0490-10	COVER,BOTTOM,K450B	1	EA	
4	7000-0334-10	HDWR "U" SPEED NUT FSTNR	6	EA	
5	0121-0007-30	ASSY,FRONT BEZEL,K450B	1	EA	
6	0117-0023-30	CASTING,FRONT,MACHINED,K450B	1	EA	
9	0285-0281-10	INSULATOR,SHIELD,4500	1	EA	
10	0121-0480-10	ASSY,PCB,MOTHERBOARD,K450B	1	EA	
11	0121-0405-10	ASSY,REAR,CASTING,K450B	1	EA	
12	0121-0407-10	FAB,CARD CAGE, K450B	1	EA	
13	9000-0225-40	ASSY PWR SPLY TESTED K450B	1	EA	
15	7000-0404-10	HDWR CARD GUIDE NYL 6.00L	16	EA	
22	0111-0016-10	ASSY,HANDLE	1	EA	
23	7000-0577-10	LUG SLIP-ON MALE TAB #6	1	EA	
24	0285-0117-30	SIDE RAIL,WHT,4500	2	EA	
25	8200-0032-10	ADHESIVE,THREAD LOCK 262	0	EA	
26	0120-0043-01	ASY CBL PROBE TEST TO CLK,K205	1	EA	
28	0120-0145-20	ASSY,HARNESS,DOS-PWR,K450,1 DD	1	EA	
29	0950-0099-10	REAR FOOT,K500	4	EA	
30	9000-0163-10	ASSY, VIDEO MONITOR, 7" CRT	1	EA	
31	7000-0376-10	SCR,HD,CAP,3/4 X 1/4-20	2	EA	
32	7000-0328-10	SCR,PHH,8-32 X 5/8	8	EA	
33	7011-1832-60	SCR,X,PH,8-32 X 1-7/8,STZN	4	EA	
34	7011-1632-16	SCR,X,PH,6-32 X 1/2,STZN	23	EA	
35	7080-1006-00	WSHR,FLAT,#6,STZN	37	EA	
36	7071-1008-00	NUT,KEP,#8,STD,STZN	2	EA	
37	7021-2632-12	SCR,X,FH 100,6-32 X 3/8,SS	9	EA	
38	7094-0001-10	WSHR,SPRG,1/4	2	EA	
39	7085-1006-00	WSHR,INT TOOTH LOCK,#6,STZN	33	EA	
40	7011-1632-12	SCR,X,PH,6-32 X 3/8,STZN	11	EA	
43	7071-1632-00	NUT,S-LOCK,6-32,STD,STZN	8	EA	
44	7200-0019-10	CBL CLAMP,FLAT,RIBBON	2	EA	
52	0112-0308-10	INSULATOR, KEYBOARD	1	EA	
58	0121-0166-10	BRACKET,MTG,PS,K450	1	EA	
59	7000-0073-10	WSHR FLT #6 FIBER	8	EA	
64	0121-0205-10	ASSY,CBL,COMP115MX-7 TO DSPLY	1	EA	
65	0121-0426-10	CONNECTOR SUPPORT, K450B	1	EA	
67	7200-0044-10	GROMMET,FLEX,SPGS-2,ROLL	2	FT	



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSY. REVISION LEVEL WHERE SHO CONTRASTING INDELIBLE INK.
2. ASSEMBLY REFLECTS SCHEMATIC DWG. O & FAB DWG. 0121-0412 .
3. MANUFACTURE PER GOULD WORKMANSHIP 87000012.
4. R42 & C3 NOT LOADED.

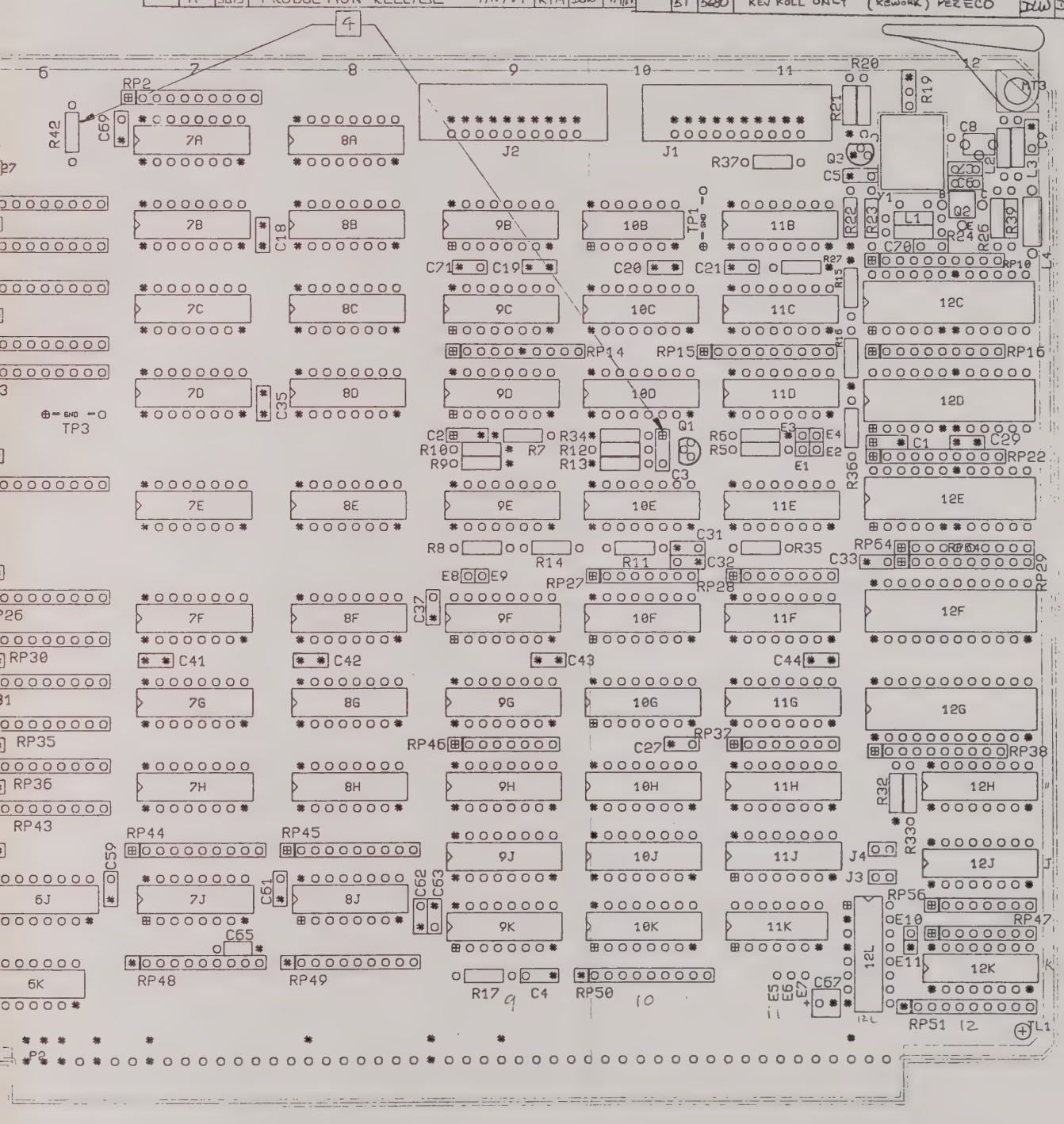
DIETERICH POST RECORDER NO. 87000

DWG. NO. 0121-0410 SH 1 REV A

	52	5697	REVISED PER ECO	5/27/87	MM	DLW
	53	5719	REV ROLL ONLY	6/12/87	MM	
	54	5750	REV ROLL ONLY	7/11/87	MM	DLW
	A	5815	PRODUCTION RELEASE	9/10/87	RTM	DLW

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5664	PILOT RELEASE	RTM	DLW	5/4/87
	51	5680	REV ROLL ONLY (REWORK) PER ECO	DLW	DLW	5/29/87



-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

GOULD PART NO.

APPROVALS	DATE
DRAWN	4/30/86
CHECKED	5/4/87
PROJ ENG	

GOULD Electronics

TITLE: ASSY, PCB CLOCK K450B

DASH NO.	NEXT ASSY	USED ON
10	K450B-XXX	K450B

FIRST APPLICATION

DO NOT SCALE DRAWING

SIZE D | DWG NO 0121-0410 | REV A

SCALE 2/1 | MODEL K450B | SHEET 1 OF 1

WN USING

21-0411

STD.

BILL OF MATERIAL

AS OF 10/30/87

0121-0410-10 ASSY,PCB,CLOCK,K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	0121-0411	DWG.SCHEM.CLOCK PCB. K450B	0	EA	
0	D0121-0410	DWG,ASSY,PCB,CLOCK,K450B	0	EA	
1	0121-0412-10	FAB,PCB,CLOCK,K450B	1	EA	
3	1400-0019-10	TRAN 2N3906	2	EA	Q1,3
4	3000-1200-10	RES,120,5%,1/4W,C	2	EA	R34,37
5	1300-0038-10	TRAN BFR-91	1	EA	Q2
7	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	11K
8	1800-0254-10	IC 74LS85N 4-BIT MAG	1	EA	12L
9	1800-0349-10	IC 74368AN HEX BUS DR	1	EA	9F
10	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	6K
11	1820-0028-10	IC 4028 1 OF 10 DEC	1	EA	9B
12	1820-0065-10	IC F4069B HEX INVERTER	1	EA	10B
13	1820-0063-10	IC MC14518B DUAL UP CNT	2	EA	9C,9D
15	1850-0077-10	IC F100101DC TPL 5OR/NOR	6	EA	1E,2F,4E, 4F,4H,12E
17	6100-0119-10	SKT 14 PIN DIP LO-PROFIL	1	EA	X6K
19	1850-0078-10	IC F100102DC 2IN OR/NOR	25	EA	12D 1D,G,H,J, 2B,C,D,G, G,H,4C,D, G,H,J,12C, G,J,5D,F, H,3C,E,F,
21	1850-0147-10	IC 10474	2	EA	12F,12G
22	1850-0125-10	IC MC10H116P TPL LINE RCVR	4	EA	1F,2E,3D, 5E
23	1850-0097-10	IC MC10231L DUAL D F/F	2	EA	4B,11D
24	1850-0098-10	IC MC10176L HEX D F/F	22	EA	11E,9H,10J 11F 7A-7H,9G 8A-8H,10H
26	1850-0105-10	IC MC10173L QUAD 2-IN	2	EA	10G,11J
27	1850-0099-10	IC MC10164L 8-INPUT MULT	1	EA	10C
28	1850-0100-10	IC MC10161L 1 OF 8 DEC	1	EA	9J
29	1850-0101-10	IC MC10137L DECADE CNTR	2	EA	9E,10E
30	1850-0103-10	IC MC10125L QUAD ECL-TT	1	EA	10F
31	1850-0104-10	IC MC10124L QUAD TTL	5	EA	6J,7J,8J 9K,10K
32	1850-0108-10	IC F10109DC DUAL 4-5 INP	1	EA	10D
33	1850-0113-10	IC MC10101L QUAD OR/GAT	2	EA	11H,11C
35	6100-0137-10	SKT 24 PIN DIP LOW PRO	2	EA	X12F,X12G
36	2100-0014-10	IND 1025-94 MOLDED CHOKE	2	EA	L2,L3
37	2100-0012-10	IND 1025-12 FERRITE CORE	1	EA	L1
38	2100-0036-10	IND 2743002121 SHLD BEAD	1	EA	L4
40	2950-5106-10	RES,51,5%,1/8W,C	1	EA	R24
41	3000-1000-10	RES,100,5%,1/4W,C	2	EA	R35,36

BILL OF MATERIAL
AS OF 10/30/87

0121-0410-10 ASSY,PCB,CLOCK,K450B
MODEL: K450B

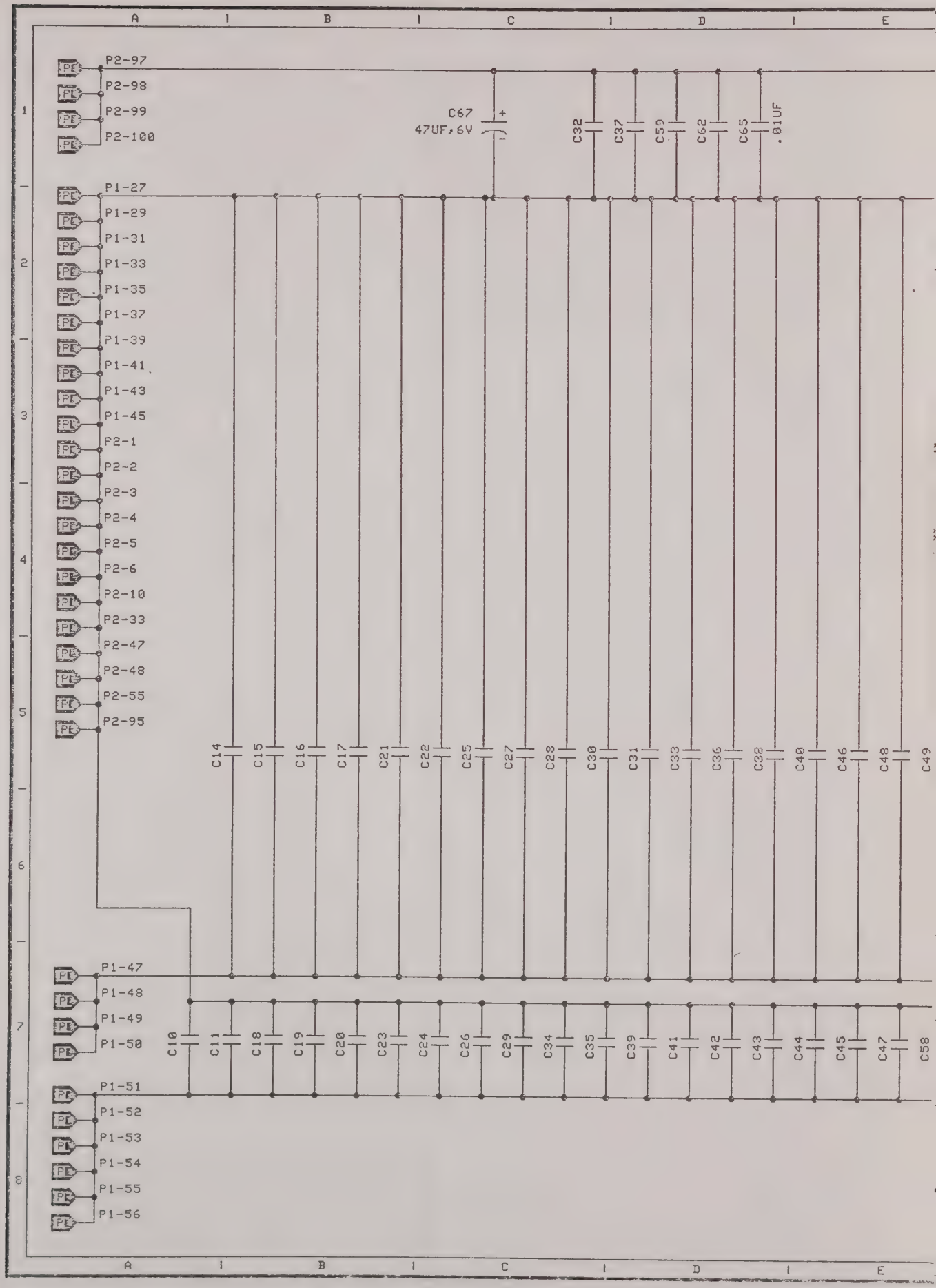
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
42	3000-8200-10	RES,820,5%,1/4W,C	1	EA	R21
43	3000-1006-10	RES,10,5%,1/4W,C	1	EA	R9
44	3000-1501-10	RES,1.5K,5%,1/4W,C	1	EA	R26
45	3000-1600-10	RES,160,5%,1/4W,C	1	EA	R15
46	3000-1800-10	RES,180,5%,1/4W,C	1	EA	R16
48	3000-2001-10	RES,2K,5%,1/4W,C	3	EA	R8,7,32
49	3000-2200-10	RES,220,5%,1/4W,C	4	EA	23 R10,12,20,
51	3000-3006-10	RES,30,5%,1/4W,C	2	EA	R5,R39
52	3000-4700-10	RES,470,5%,1/4W,C	1	EA	R13
53	3000-5100-10	RES,510,5%,1/4W,C	1	EA	R27
54	3000-5600-10	RES,560,5%,1/4W,C	1	EA	R22
55	3000-3001-10	RES,3K,5%,1/4W,C	1	EA	R33
56	3000-6800-10	RES,680,5%,1/4W,C	1	EA	R6
57	3000-6806-10	RES,68,5%,1/4W,C	3	EA	R11,14,17
59	3300-0067-10	POT,200,0.5W,10% 20T,PC,RTANG	1	EA	R19
60	3700-0051-10	RPAK,10K,0.2W,2%,8/4	1	EA	RP14
61	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	4	EA	RP48-51
62	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	5	EA	54,61 RP47,52,53
63	3700-0039-10	RPAK,56,0.18W,2%,10/9	4	EA	24 RP3,5,23
64	3700-0091-10	RPAK,68,0.2W,2%,8/7	5	EA	37,46,56 RP27,28
66	3700-0092-10	RPAK,68,0.2W,2%,10/9	42	EA	17,18-22, 25,26,29-36,38,40-45,57,58, 59,60,62, 6-13,15,16 64 RP1,2,4,
68	5100-0004-10	XTAL 100MHZ .39UH	1	EA	Y1
69	3700-0096-10	RPAK,100,0.2W,2%,8/7	1	EA	RP55
70	4010-0330-10	CAP,33PF,50/100V,5%,CER	2	EA	C70,71
71	4010-0560-10	CAP,56PF,50/100V,5%,CER	1	EA	C1
73	4010-5606-10	CAP,5.6PF,100V,5%,CER	1	EA	C7
76	4010-0103-10	CAP,0.01UF,50V,10%,CER	55	EA	52-54 58-63,65 69 9-11,14-49 C2,4-6
79	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	6	EA	57,67,68 C12,13,51
80	4600-0009-10	CAP 1.2-3PF,100V	1	EA	C8
81	6000-0571-10	CONN SHORTING PLUG	10	EA	T1-T2

BILL OF MATERIAL

AS OF 10/30/87

0121-0410-10 ASSY,PCB,CLOCK,K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
81	6000-0571-10	CONN SHORTING PLUG	10	EA	T10-T11 T13-T14 T16-T17 T19-T20 T22-T23 T4-T5 T7-T8 XJ3,XJ4
83	6000-0384-10	CONN 20 POS RT ANGLE HDR	2	EA	J1,2
84	6000-0293-08	CONN 8 POS HDR ST SGL ROW	3	EA	3K(3)
88	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
90	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
91	1850-0131-10	IC MC10H016L B/N COUNTER	4	EA	11G,12H 12J,11B
92	1850-0124-10	IC 10H105 TRIPLE 2-3-2 OR/NOR	1	EA	12K
93	6000-0293-02	CONN 2 POS HDR ST SGL ROW	2	EA	J3,J4


A
B
C
D
E
1
2
3
4
5
6
7
8
P2-97
P2-98
P2-99
P2-100
P1-27
P1-29
P1-31
P1-33
P1-35
P1-37
P1-39
P1-41
P1-43
P1-45
P2-1
P2-2
P2-3
P2-4
P2-5
P2-6
P2-10
P2-33
P2-47
P2-48
P2-55
P2-95
P1-47
P1-48
P1-49
P1-50
P1-51
P1-52
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P1-54
P1-55
P1-56
C67
47UF,6V
+
C32
C37
C59
C62
C65
.01UF
C14
C15
C16
C17
C21
C22
C25
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C38
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C20
C23
C24
C26
C29
C34
C35
C39
C41
C42
C43
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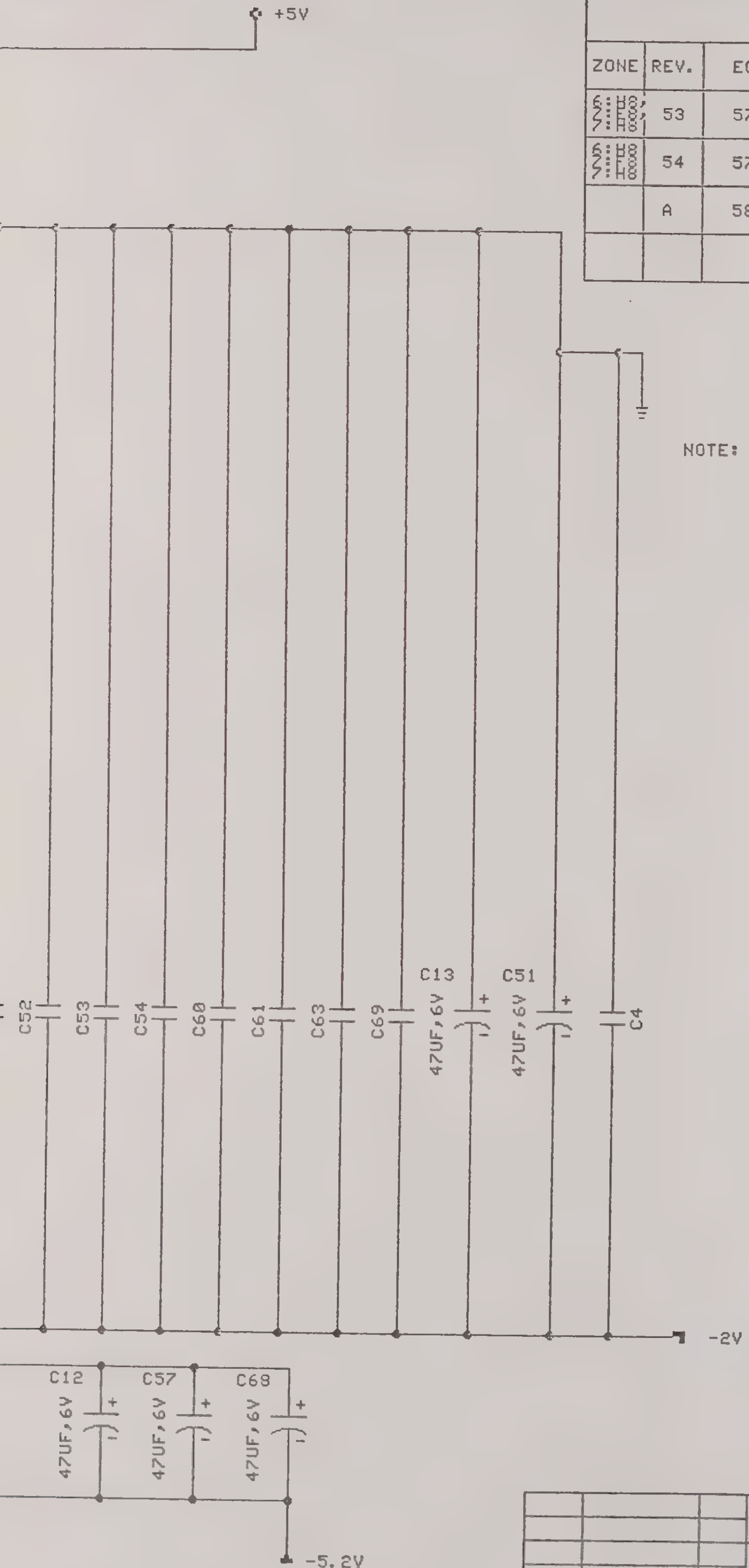
C45
C47
C58



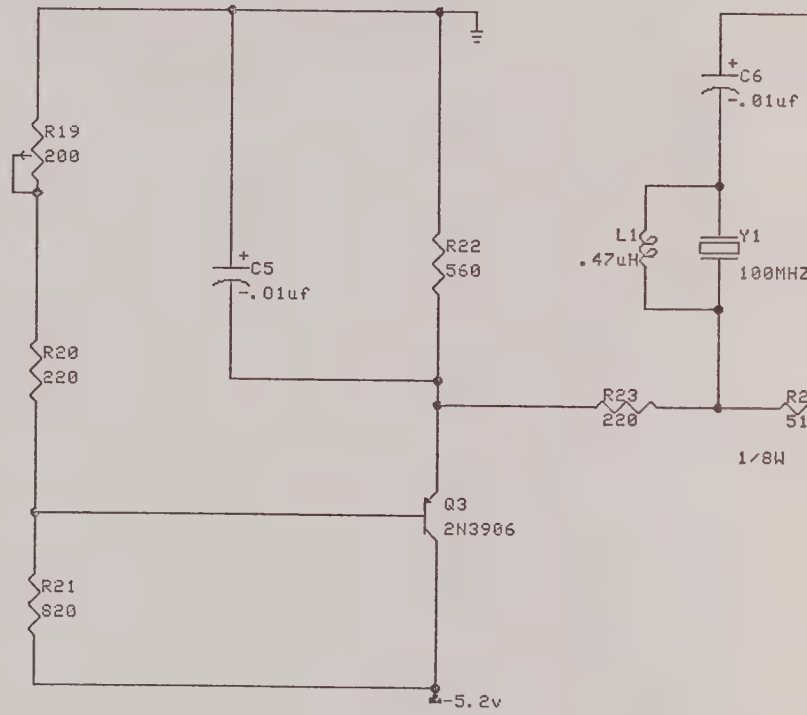
REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE
6:H8, 5:E8, 7:H8	53	5719	SAMPLE CLOCK BUFFER MOD.				6/87
6:H8 5:E8 7:H8	54	5750	ADD 6" DELAY TO SAMPLE CLKS	S.M.			9/87
	A	5815	REVISION ROLL ONLY	S.M.	[illegible]		SEPT 9,87

NOTE: THE FOLLOWING EDGE CONNECTOR PINS ARE NOT USED:

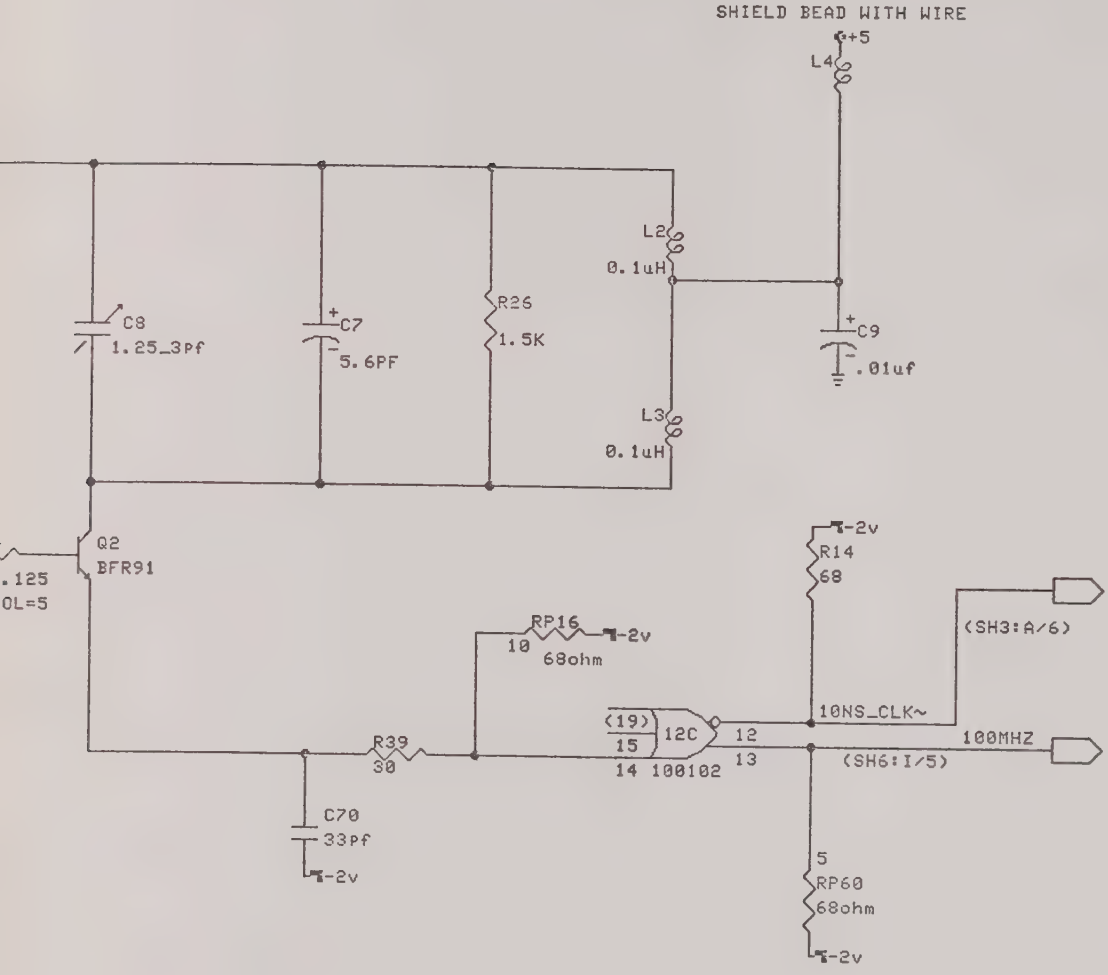
P1-25 & 26; P2-8,13,14,16,34,35,43,45,49,51,53, 44 THRU 84(EVEN) & 57 THRU 91(ODD).

DASH NO.	NUMBER NEXT ASSEMBLY	QTY		
DRAWN H. SHEGARFI	DATE 5/87	GOULD DESIGN & TEST		
PROJ. ENGR J. STAGER	5/87	TITLE SCHEMATIC, CLOCK BOARD, K450B		
MANUFACTURING				
QUALITY ASSUR		MODEL K450B	PART NUMBER B8121-0411	REV A
ECO NO.		SEPT 9,1987	SHEET 1 OF 11	

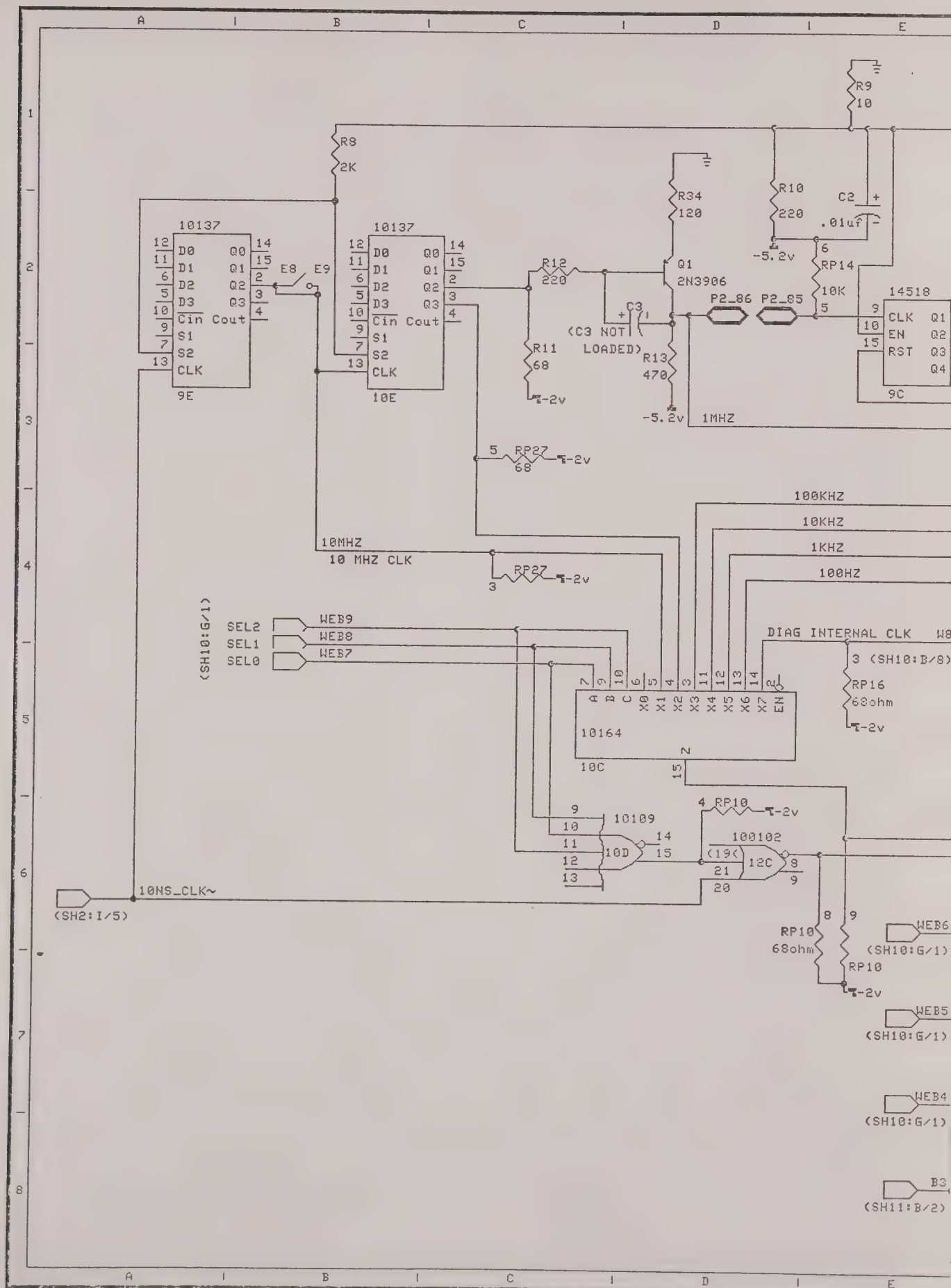
09 SEP 87 10:46 /USER/STEVE/CLOCK 1.DRAW

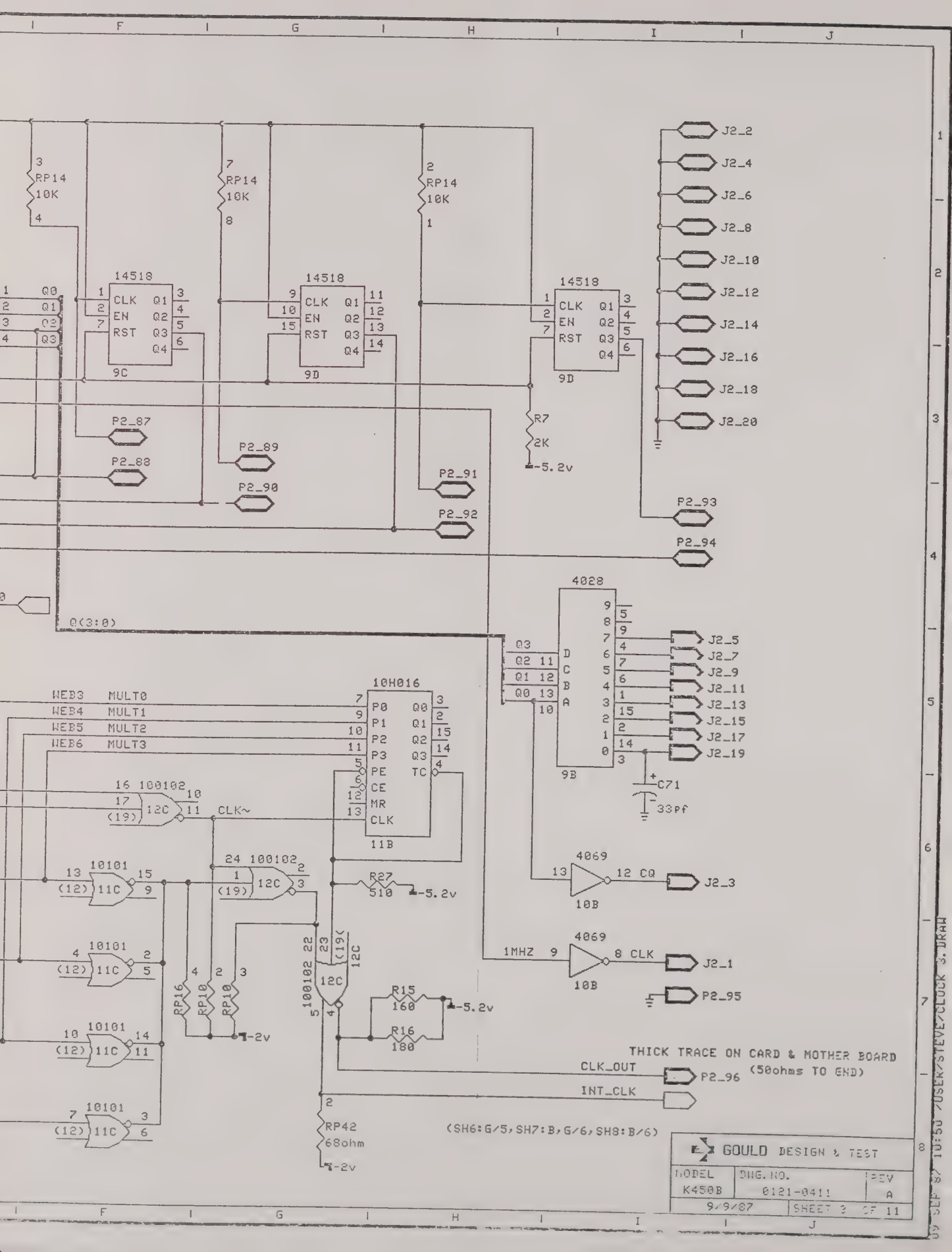


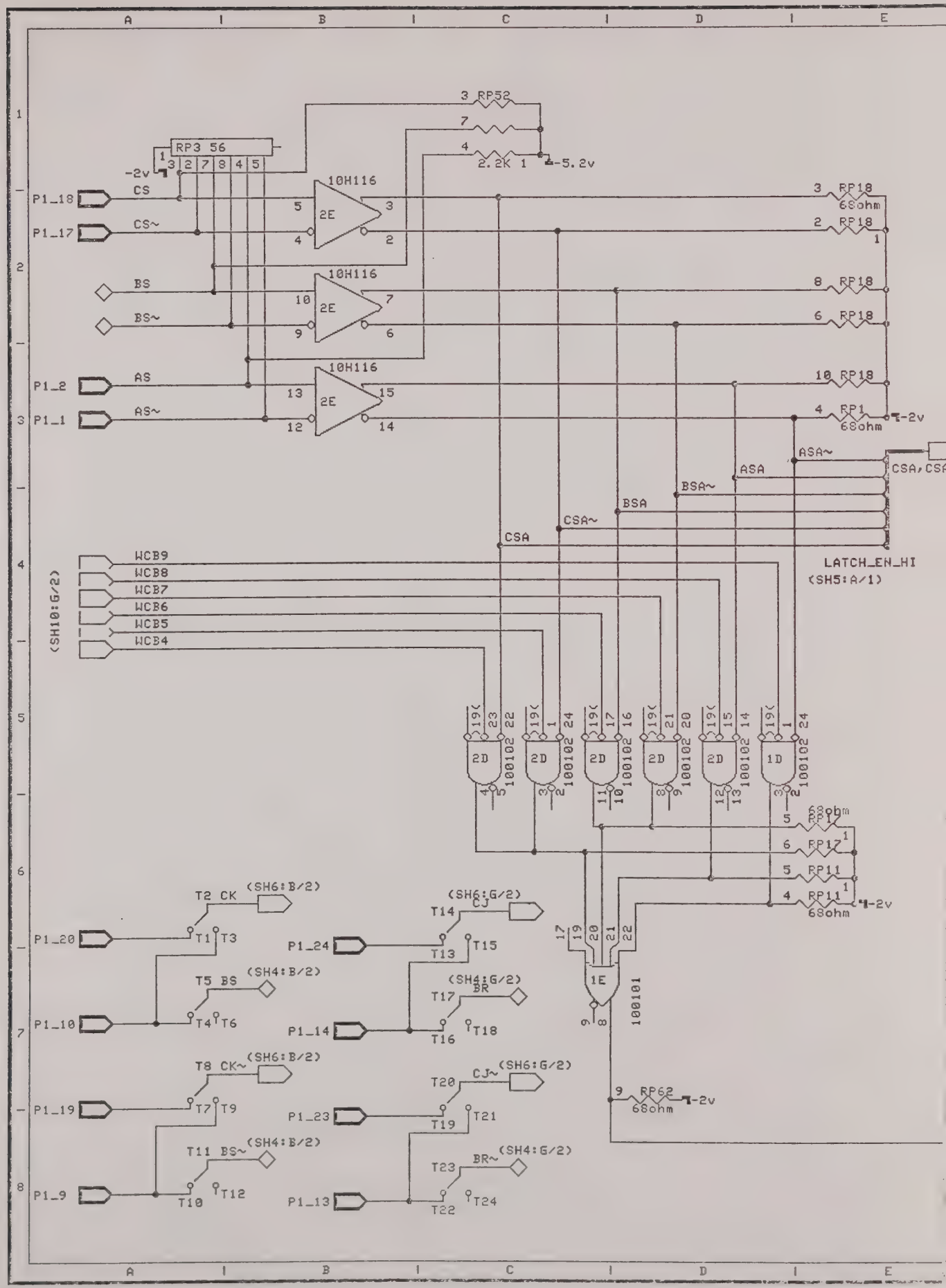
1. MPU GENERATED DIAGNOSTIC INTERNAL CLOCK
   PRODUCEDS A SHORT LOW PERIOD CLK PULSE,
   OF THE SAME DURATION AS WR~ BUS PULSE.
   THE SAME IS TRUE OF THE DIAGNOSTIC LATCH CLOCK (W8B1).
2. ALL DISCRETE RESISTORS ARE 1/4W (POWER PARAM),
   5% TOLORANCE (TOL PARAM), UNLESS OTHERWISE NOTED.

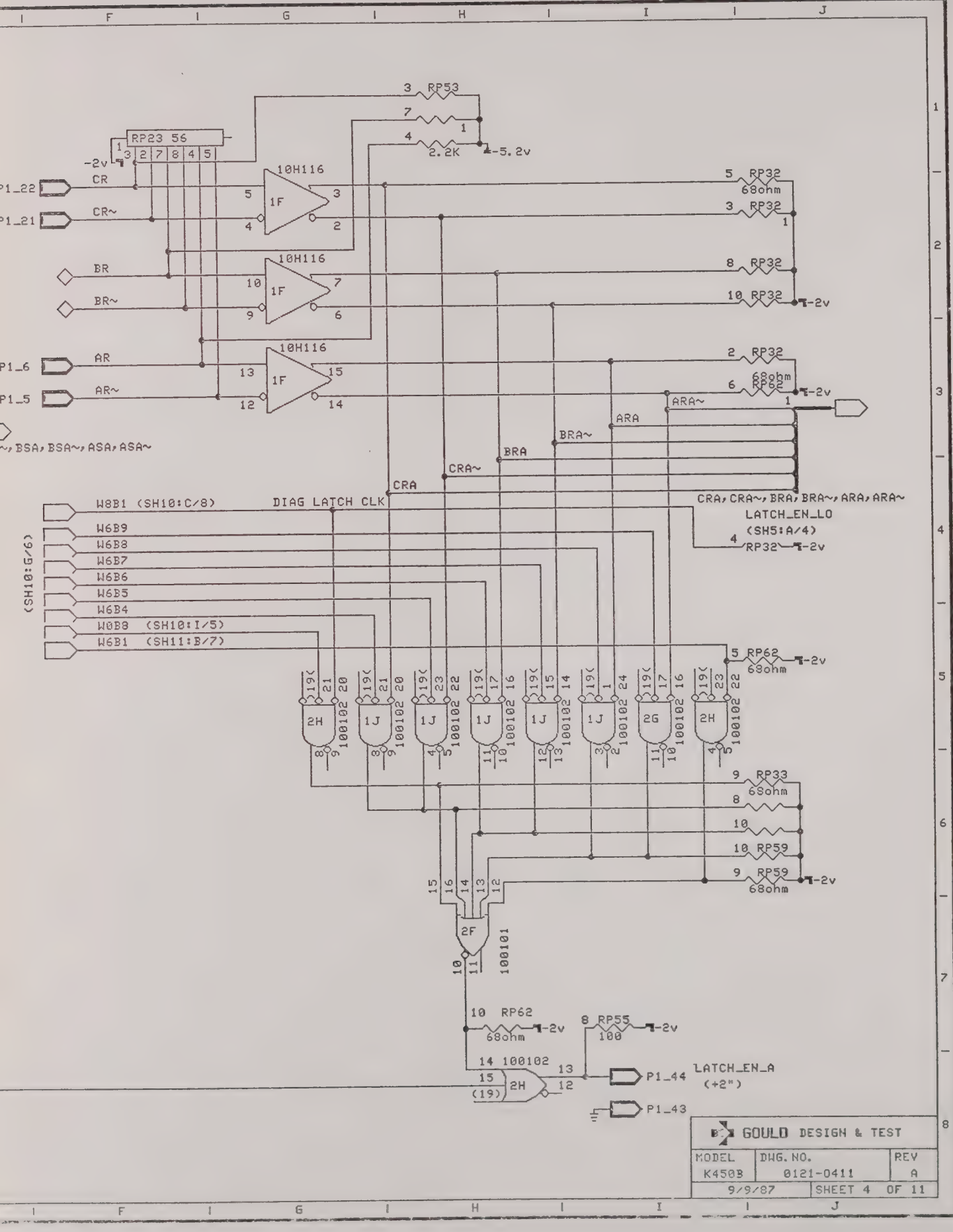


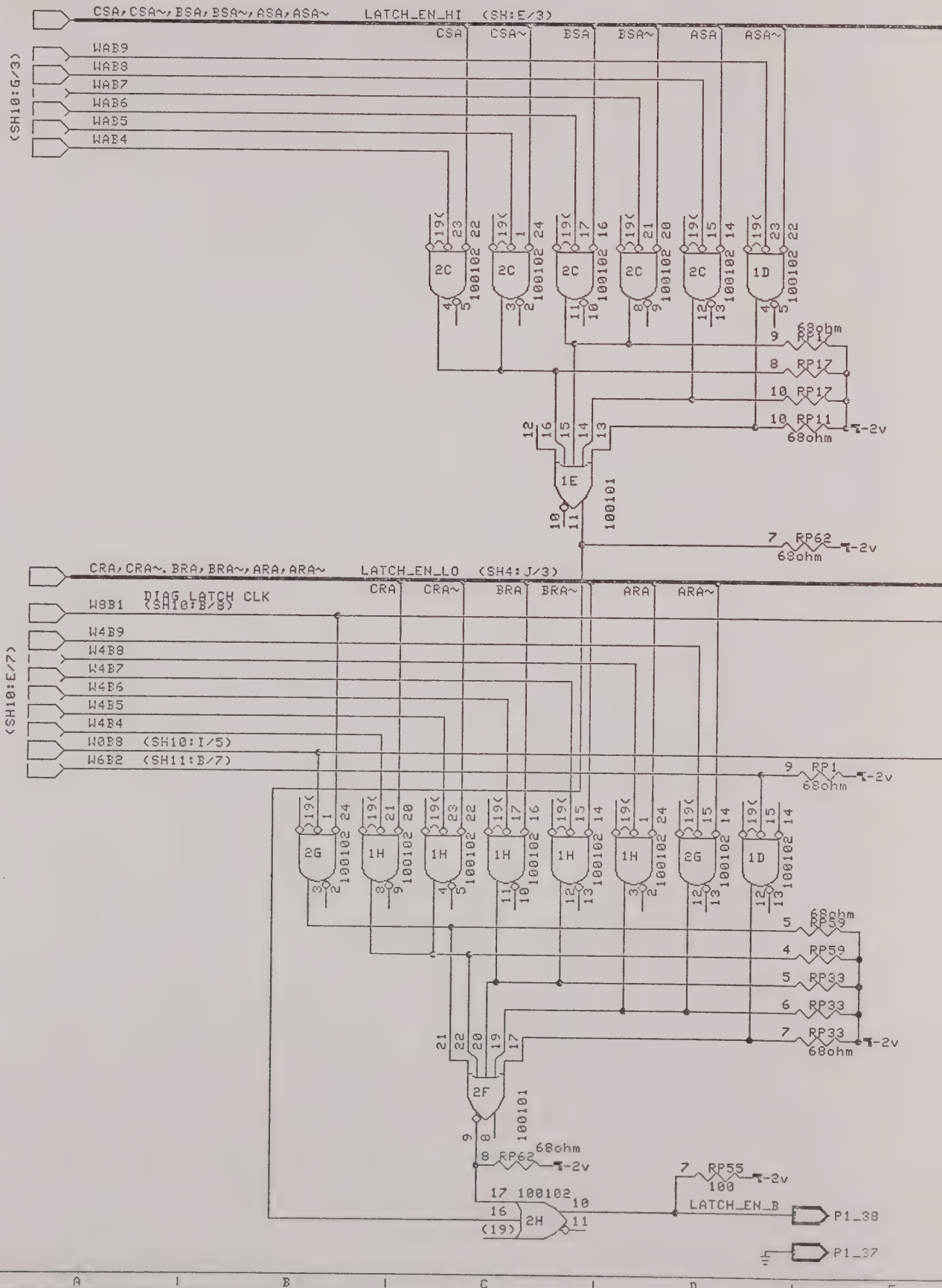
GOULD DESIGN & TEST		
MODEL	DWG. NO.	REV
K450B	0121-0411	A
9/9/87	SHEET 2	OF 11

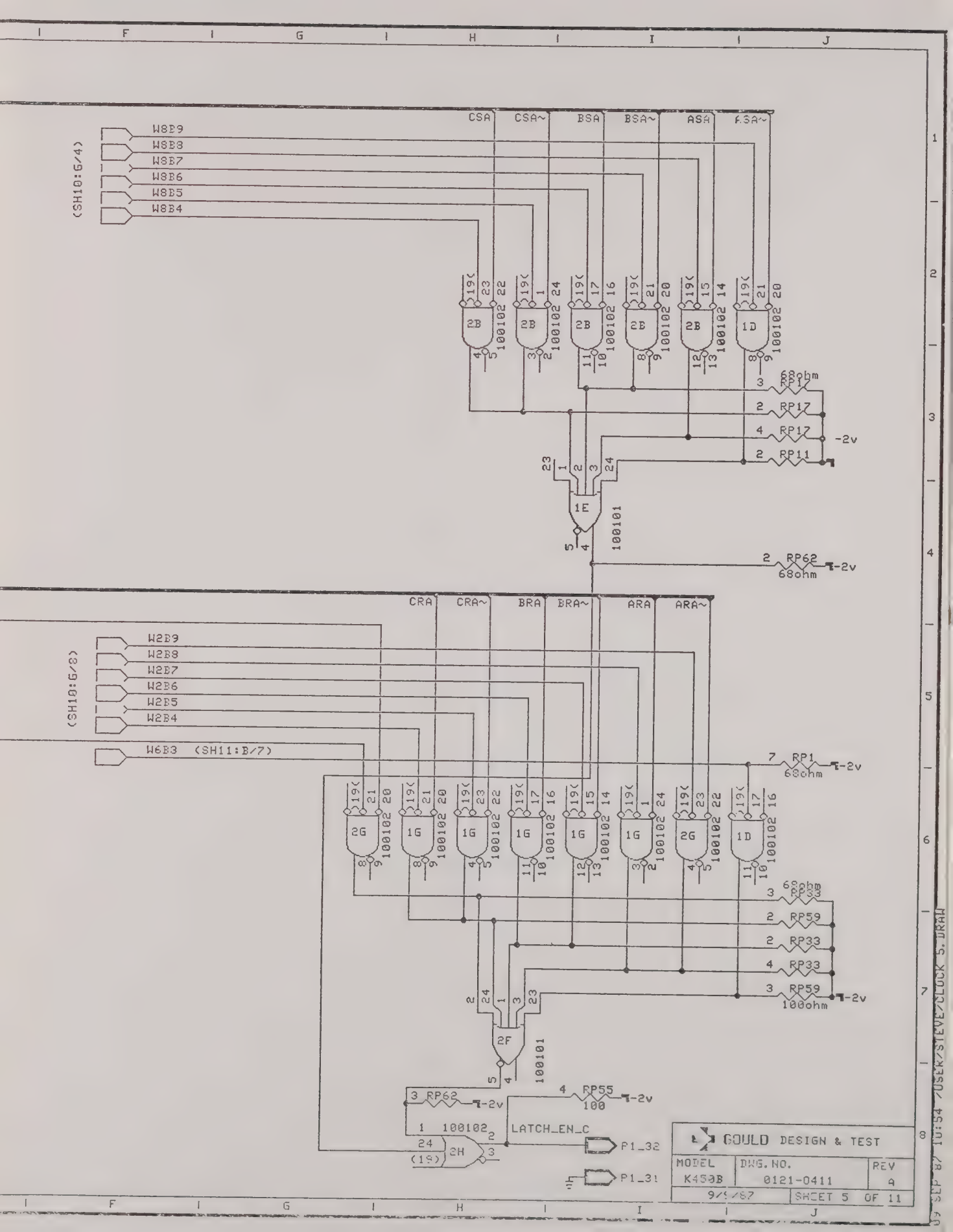

R9
10
R8
2K
R34
120
R10
220
C2
.01uf
-5.2v
RP14
10K
14518
CLK Q1
EN Q2
RST Q3
Q4
9C
10137
D0 Q0
D1 Q1
D2 Q2
D3 Q3
Cin Cout
S1
S2
CLK
9E
10E
E8
E9
R12
220
Q1
2N3906
C3
(C3 NOT LOADED)
R11
68
R13
470
-2v
P2_86
P2_85
1MHZ
RP27
68
100KHZ
10KHZ
1KHZ
100HZ
10MHZ
10 MHZ CLK
DIAG INTERNAL CLK
3 (SH10:B/8)
RP16
68ohm
SEL2
SEL1
SEL0
WEB9
WEB8
WEB7
(SH10:G/1)
10164
10C
RP10
10109
10D
100102
12C
10NS_CLK~
(SH2:I/5)
WEB6
WEB5
WEB4
B3
(SH11:B/2)

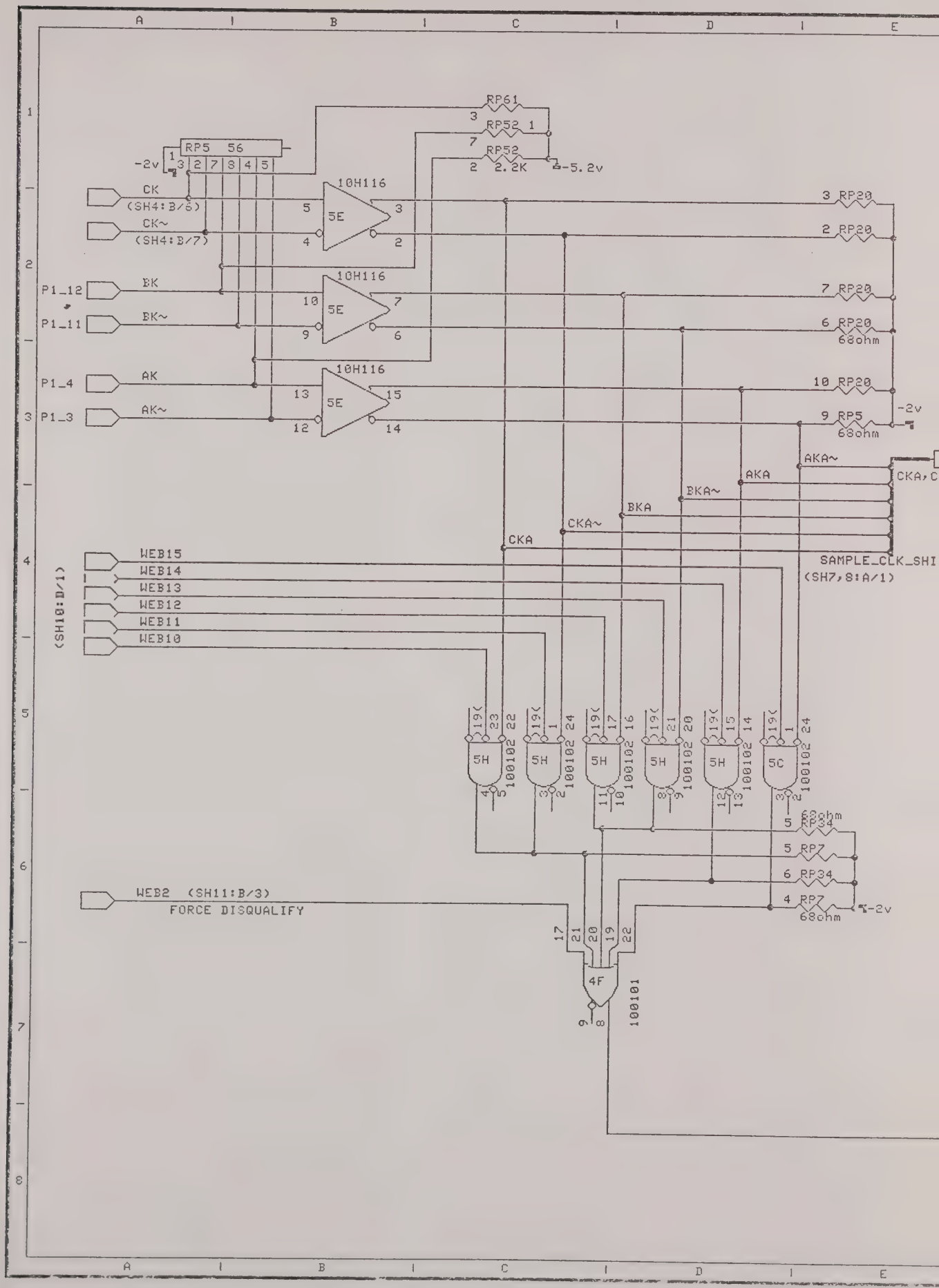

RP14 10K
14518
CLK
EN
RST
Q1
Q2
Q3
Q4
9C
9D
R7 2K
-5.2v
P2_87
P2_88
P2_89
P2_90
P2_91
P2_92
P2_93
P2_94
J2_2
J2_4
J2_6
J2_8
J2_10
J2_12
J2_14
J2_16
J2_18
J2_20
Q(3:0)
4028
9B
J2_5
J2_7
J2_9
J2_11
J2_13
J2_15
J2_17
J2_19
C71
33pf
WEB3 MULT0
WEB4 MULT1
WEB5 MULT2
WEB6 MULT3
10H016
P0
P1
P2
P3
PE
CE
MR
CLK
TC
11B
100102
12C
CLK~
10101
11C
R27 510
4069
10B
J2_3
1MHZ
8 CLK
J2_1
P2_95
R15 160
R16 180
RP16
RP10
-2v
THICK TRACE ON CARD & MOTHER BOARD
(50ohms TO END)
CLK_OUT
P2_96
INT_CLK
RP42 68ohm
(SH6:G/5, SH7:B,G/6, SH8:B/6)
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0411
REV A
9/9/87
SHEET 3 OF 11

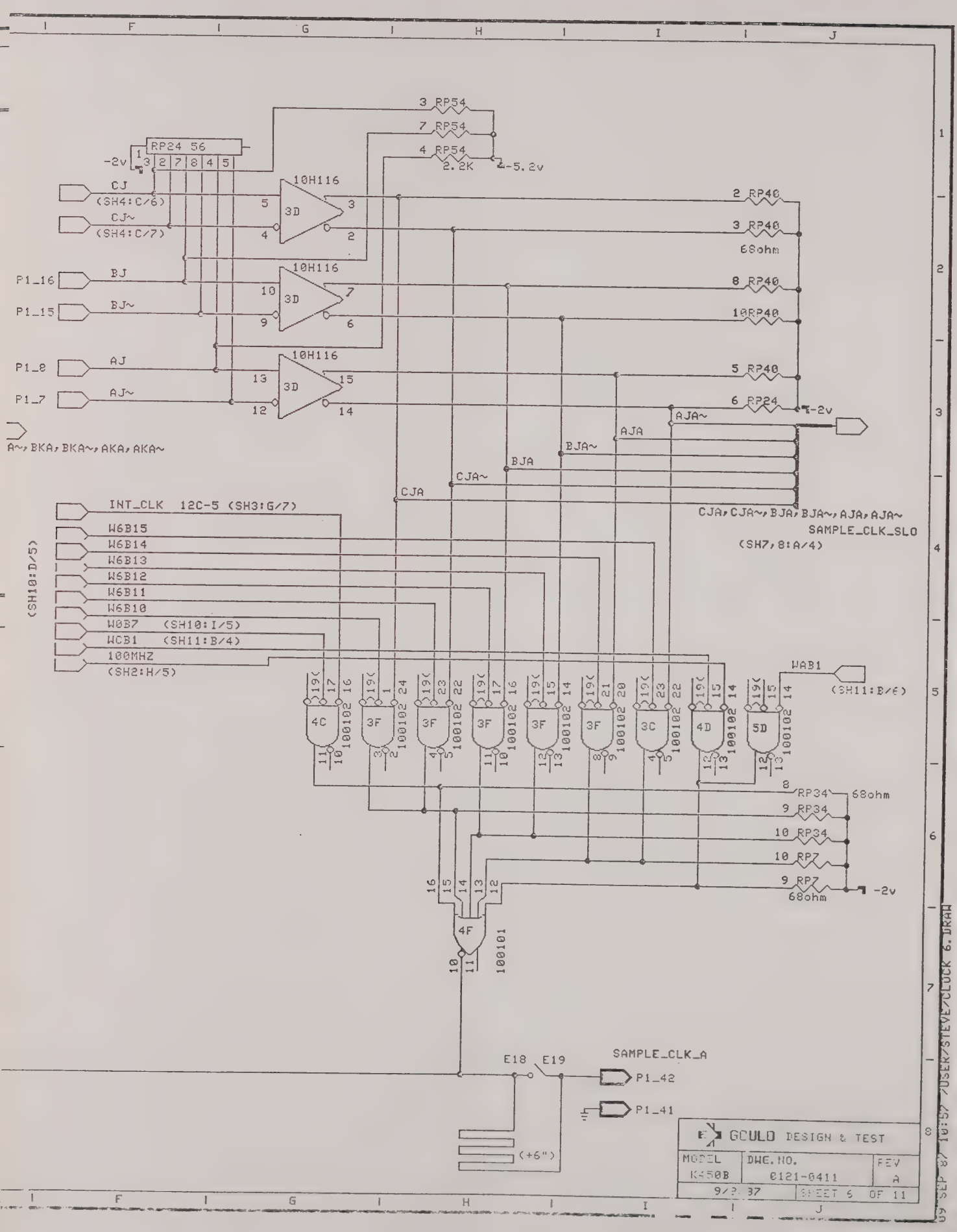

RP3 56
-2v
3 RP52
7
4
2.2K 1
-5.2v
P1_18
CS
P1_17
CS~
10H116
2E
BS
BS~
P1_2
AS
P1_1
AS~
3 RP18
68ohm
2 RP18
8 RP18
6 RP18
10 RP18
4 RP1
-2v
ASA~
ASA
CSA, CSA
BSA~
BSA
CSA~
CSA
LATCH_EN_HI
(SH5:A/1)
(SH10:G/2)
WCB9
WCB8
WCB7
WCB6
WCB5
WCB4
2D
1D
100102
5 RP17
6 RP17
5 RP11
4 RP11
1E
100101
9 RP62
T2 CK
(SH6:B/2)
P1_20
T1
T3
T5 BS
(SH4:B/2)
P1_10
T4
T6
T8 CK~
P1_19
T7
T9
T11 BS~
P1_9
T10
T12
CJ
T14
P1_24
T13
T15
BR
T17
P1_14
T16
T18
CJ~
T20
P1_23
T19
T21
BR~
T23
P1_13
T22
T24

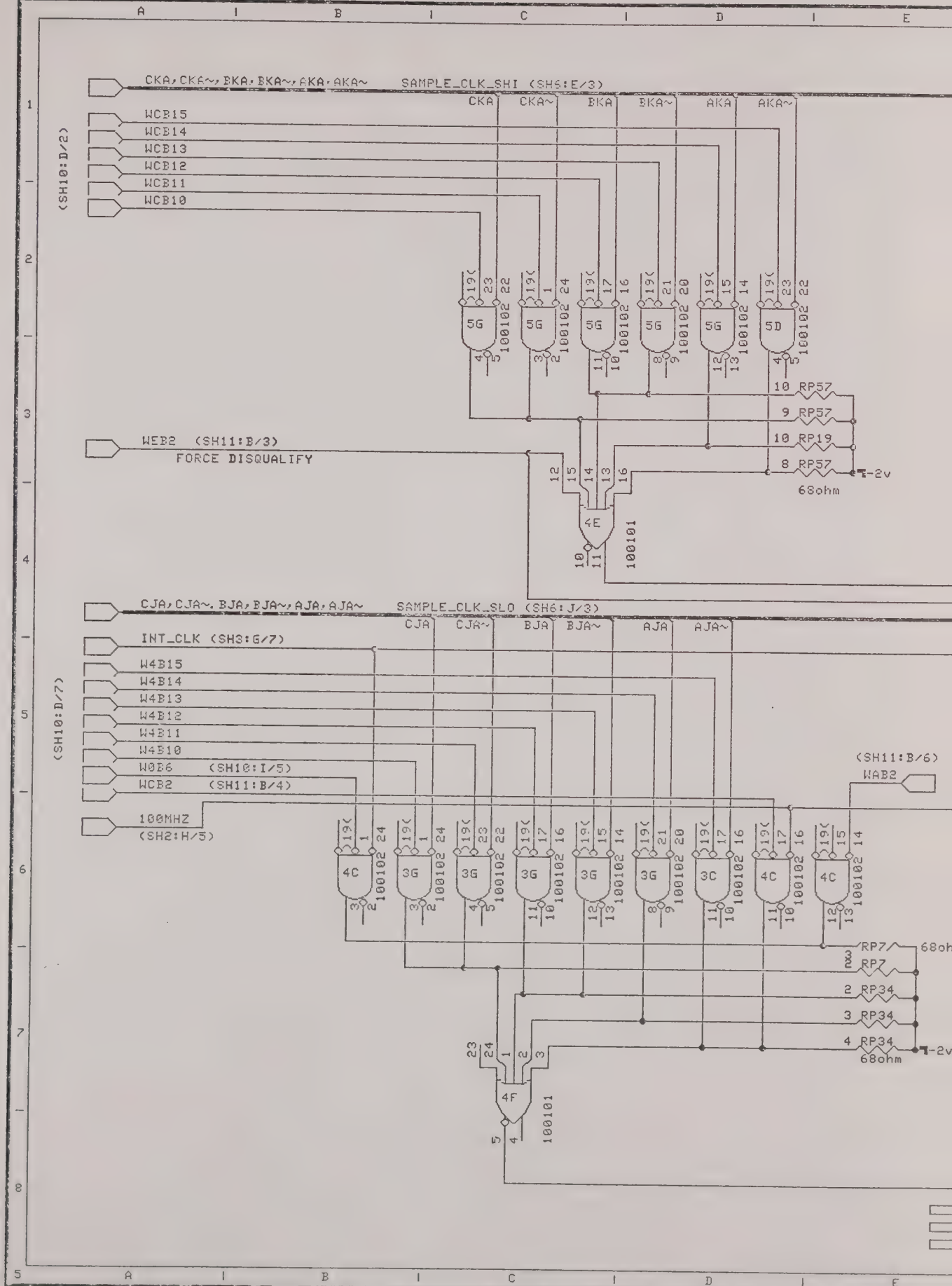

RP53
RP23 56
-2v
-5.2v
2.2K
10H116
1F
CR
CR~
BR
BR~
AR
AR~
P1_22
P1_21
P1_6
P1_5
RP32
68ohm
RP62
ARA~
ARA
BRA~
BRA
CRA~
CRA
CRA, CRA~, BRA, BRA~, ARA, ARA~
LATCH_EN_LO
(SH5:A/4)
W8B1 (SH10:C/8)
DIAG LATCH CLK
W6B9
W6B8
W6B7
W6B6
W6B5
W6B4
W0B8 (SH10:I/5)
W6B1 (SH11:B/7)
(SH10:G/6)
2H
1J
2G
100102
RP33
RP59
2F
100101
RP55
100
P1_44
LATCH_EN_A
(+2")
P1_43
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0411
REV A
9/9/87
SHEET 4 OF 11
09 SEP 87 10:52 /USER/STEVE/CLOCK 4.DRAW

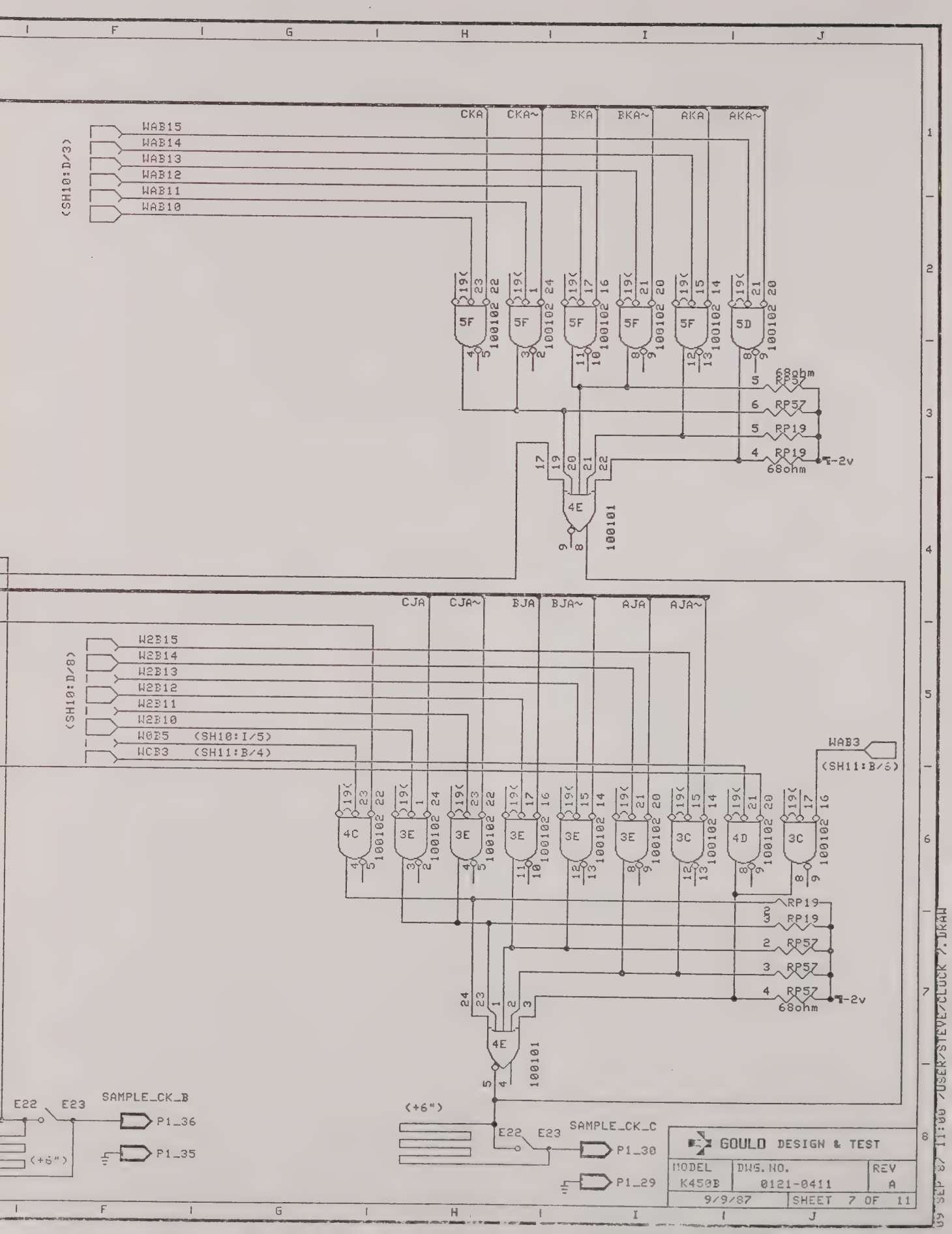

CSA,CSA~,BSA,BSA~,ASA,ASA~ LATCH_EN_HI (SH:E/3)
CSA
CSA~
BSA
BSA~
ASA
ASA~
(SH10:G/3)
WAB9
WAB8
WAB7
WAB6
WAB5
WAB4
2C
2C
2C
2C
2C
1D
100102
68ohm
RP1
RP17
RP17
RP11
-2v
1E
100101
RP62
CRA,CRA~,BRA,BRA~,ARA,ARA~ LATCH_EN_LO (SH4:J/3)
CRA
CRA~
BRA
BRA~
ARA
ARA~
DIAG LATCH CLK
W8B1 (SH10:B/8)
(SH10:E/7)
W4B9
W4B8
W4B7
W4B6
W4B5
W4B4
W0B8 (SH10:I/5)
W6B2 (SH11:B/7)
2G
1H
1H
1H
1H
1H
2G
1D
RP59
RP59
RP33
RP33
RP33
2F
100101
RP62
RP55
100
LATCH_EN_B
2H
(19)
P1_38
P1_37

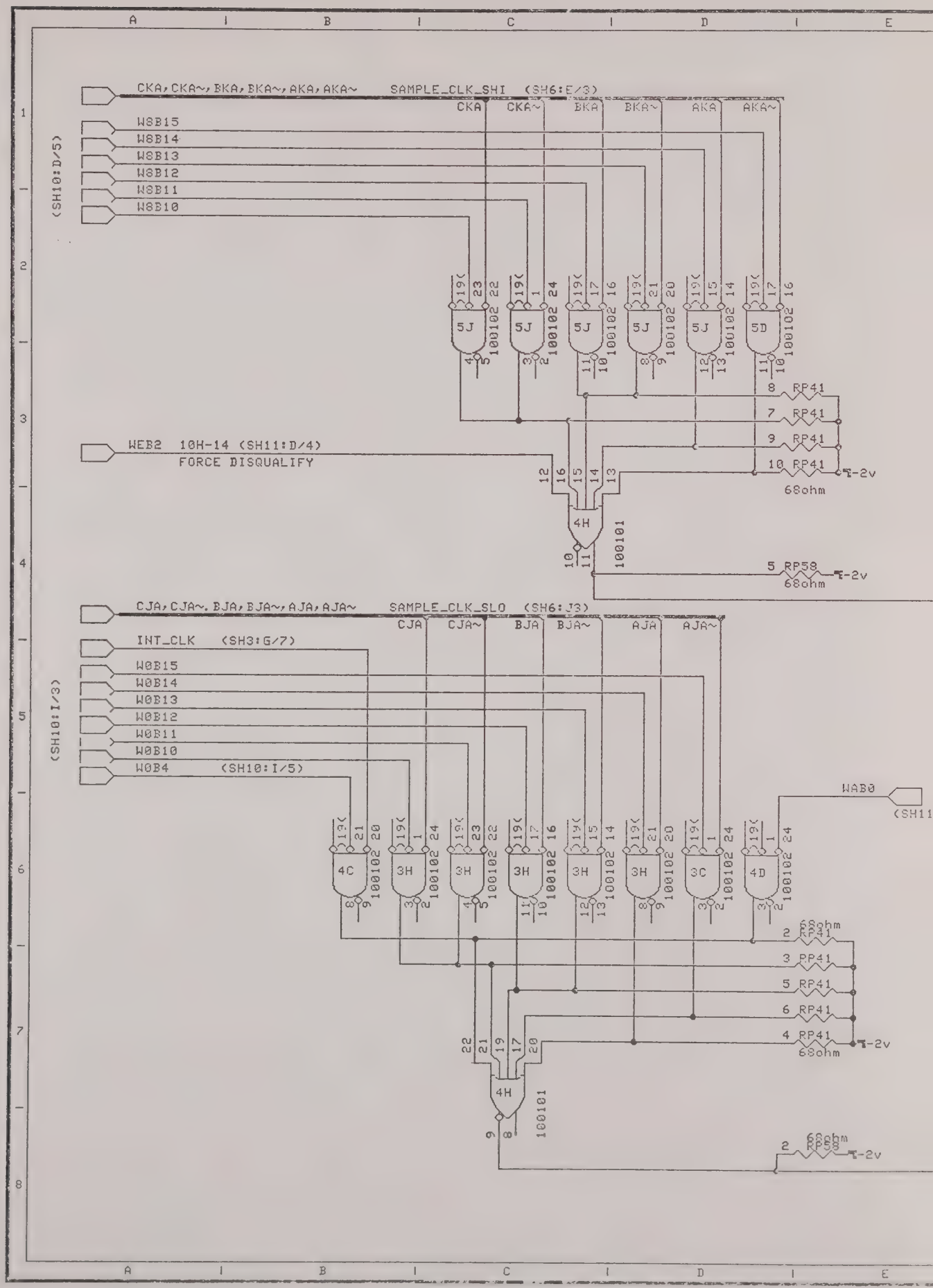

CSA
CSA~
BSA
BSA~
ASA
ASA~
W8B9
W8B8
W8B7
W8B6
W8B5
W8B4
(SH10:G/4)
2B
1D
100102
68ohm
RP17
RP11
-2v
1E
100101
RP62
CRA
CRA~
BRA
BRA~
ARA
ARA~
W2B9
W2B8
W2B7
W2B6
W2B5
W2B4
W6B3 (SH11:B/7)
(SH10:G/8)
2G
1G
1D
RP1
RP33
RP59
100ohm
2F
RP55
100
LATCH_EN_C
2H
P1_32
P1_31
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0411
REV 9
SHEET 5 OF 11
09 SEP 87 10:54 /USER/STEVE/CLOCK 5.DRAW

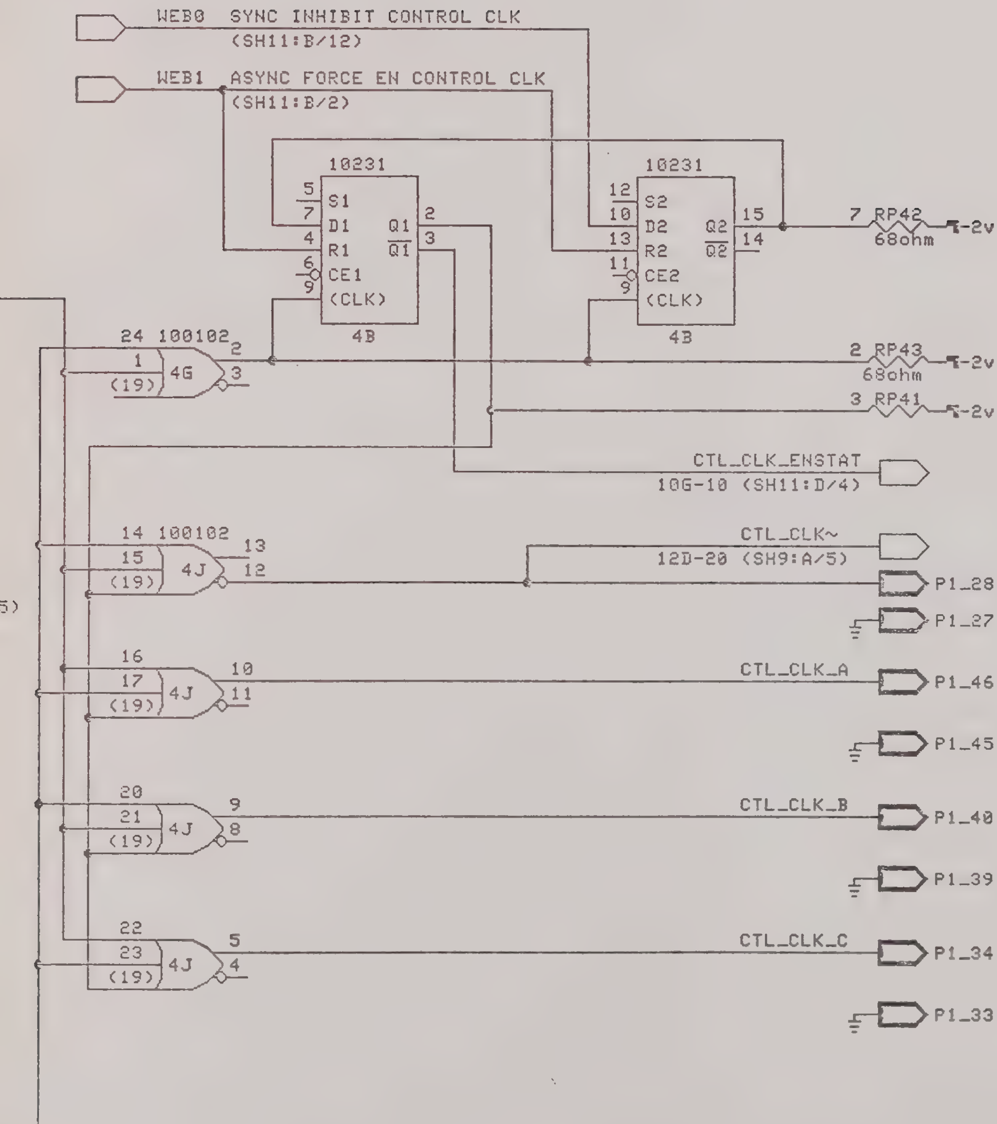

RP61
RP52
RP52
2.2K
-5.2v
RP5 56
-2v
CK
(SH4:B/6)
CK~
(SH4:B/7)
10H116
5E
BK
BK~
P1_12
P1_11
AK
AK~
P1_4
P1_3
3 RP20
2 RP20
7 RP20
6 RP20
68ohm
10 RP20
9 RP5
68ohm
-2v
AKA~
AKA
BKA~
BKA
CKA~
CKA
CKA,C
SAMPLE_CLK_SHI
(SH7,8:A/1)
WEB15
WEB14
WEB13
WEB12
WEB11
WEB10
(SH10:B/1)
5H
5C
100102
RP34
RP7
68ohm
WEB2 (SH11:B/3)
FORCE DISQUALIFY
4F
100101


3 RP54
7 RP54
4 RP54
2.2K
-5.2v
RP24 56
-2v
CJ
(SH4:C/6)
CJ~
(SH4:C/7)
10H116
3D
2 RP40
3 RP40
680hm
P1_16
BJ
P1_15
BJ~
8 RP40
10RP40
P1_8
AJ
P1_7
AJ~
5 RP40
6 RP24
-2v
AJA~
AJA
BJA~
BJA
CJA~
CJA
A~, BKA, BKA~, AKA, AKA~
CJA, CJA~, BJA, BJA~, AJA, AJA~
SAMPLE_CLK_SLO
(SH7,8:A/4)
INT_CLK 12C-5 (SH3:G/7)
W6B15
W6B14
W6B13
W6B12
W6B11
W6B10
W0B7 (SH10:I/5)
WCB1 (SH11:B/4)
100MHZ
(SH2:H/5)
(SH10:D/5)
WAB1
(SH11:B/6)
4C
3F
3C
4D
5D
100102
RP34
680hm
RP7
4F
100101
E18
E19
SAMPLE_CLK_A
P1_42
P1_41
(+6")
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0411
REV A
SHEET 6 OF 11
09-SEP-87 10:57 /USER/STEVE/CLOCK 6.DRW


CKA,CK6~,BKA,BKA~,AKA,AKA~
SAMPLE_CLK_SHI (SH5:E/3)
CKA
CKA~
BKA
BKA~
AKA
AKA~
(SH10:D/2)
WCB15
WCB14
WCB13
WCB12
WCB11
WCB10
5G
5D
RP57
RP19
WEB2 (SH11:B/3)
FORCE DISQUALIFY
-2v
68ohm
4E
100101
CJA,CJA~,BJA,BJA~,AJA,AJA~
SAMPLE_CLK_SLO (SH6:J/3)
CJA
CJA~
BJA
BJA~
AJA
AJA~
INT_CLK (SH3:G/7)
(SH10:D/7)
W4B15
W4B14
W4B13
W4B12
W4B11
W4B10
W0B6 (SH10:I/5)
WCB2 (SH11:B/4)
100MHZ
(SH2:H/5)
(SH11:B/6)
WAB2
4C
3G
3C
RP7
RP34
4F


CKA
CKA~
BKA
BKA~
AKA
AKA~
WAB15
WAB14
WAB13
WAB12
WAB11
WAB10
(SH10:D/3)
5F
5F
5F
5F
5F
5D
100102
68ohm
RP57
RP19
-2v
4E
100101
CJA
CJA~
BJA
BJA~
AJA
AJA~
W2B15
W2B14
W2B13
W2B12
W2B11
W2B10
W0B5 (SH10:I/5)
WCB3 (SH11:B/4)
(SH10:D/8)
WAB3
(SH11:B/6)
4C
3E
3C
4D
SAMPLE_CK_B
SAMPLE_CK_C
E22
E23
P1_36
P1_35
P1_30
P1_29
(+6")
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0411
REV A
9/9/87
SHEET 7 OF 11
09 SEP 87 11:00 /USER/STEVE/CLOCK 7.DRAW

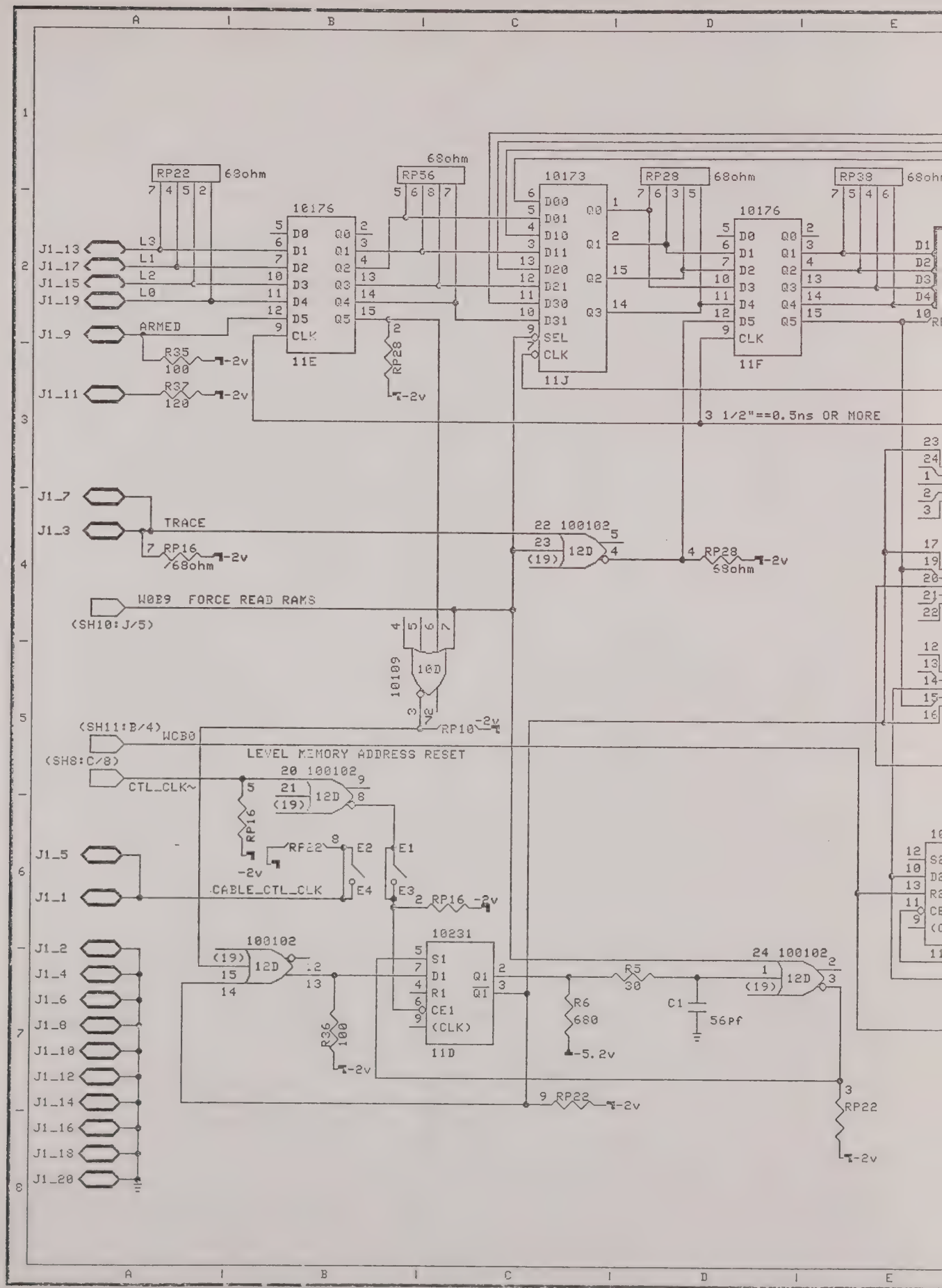

CKA, CKA~, BKA, BKA~, AKA, AKA~
SAMPLE_CLK_SHI (SH6:E/3)
CKA
CKA~
BKA
BKA~
AKA
AKA~
W8B15
W8B14
W8B13
W8B12
W8B11
W8B10
(SH10:D/5)
5J
5J
5J
5J
5J
5D
100102
8 RP41
7 RP41
9 RP41
10 RP41
-2v
68ohm
WEB2 10H-14 (SH11:D/4)
FORCE DISQUALIFY
4H
100101
5 RP58
68ohm
CJA, CJA~, BJA, BJA~, AJA, AJA~
SAMPLE_CLK_SLO (SH6:J3)
CJA
CJA~
BJA
BJA~
AJA
AJA~
INT_CLK (SH3:G/7)
W0B15
W0B14
W0B13
W0B12
W0B11
W0B10
W0B4 (SH10:I/5)
(SH10:I/3)
WAB0
(SH11
4C
3H
3H
3H
3H
3H
3C
4D
100102
2 RP41
3 RP41
5 RP41
6 RP41
4 RP41
68ohm
-2v
4H
100101
2 RP58
68ohm
-2v

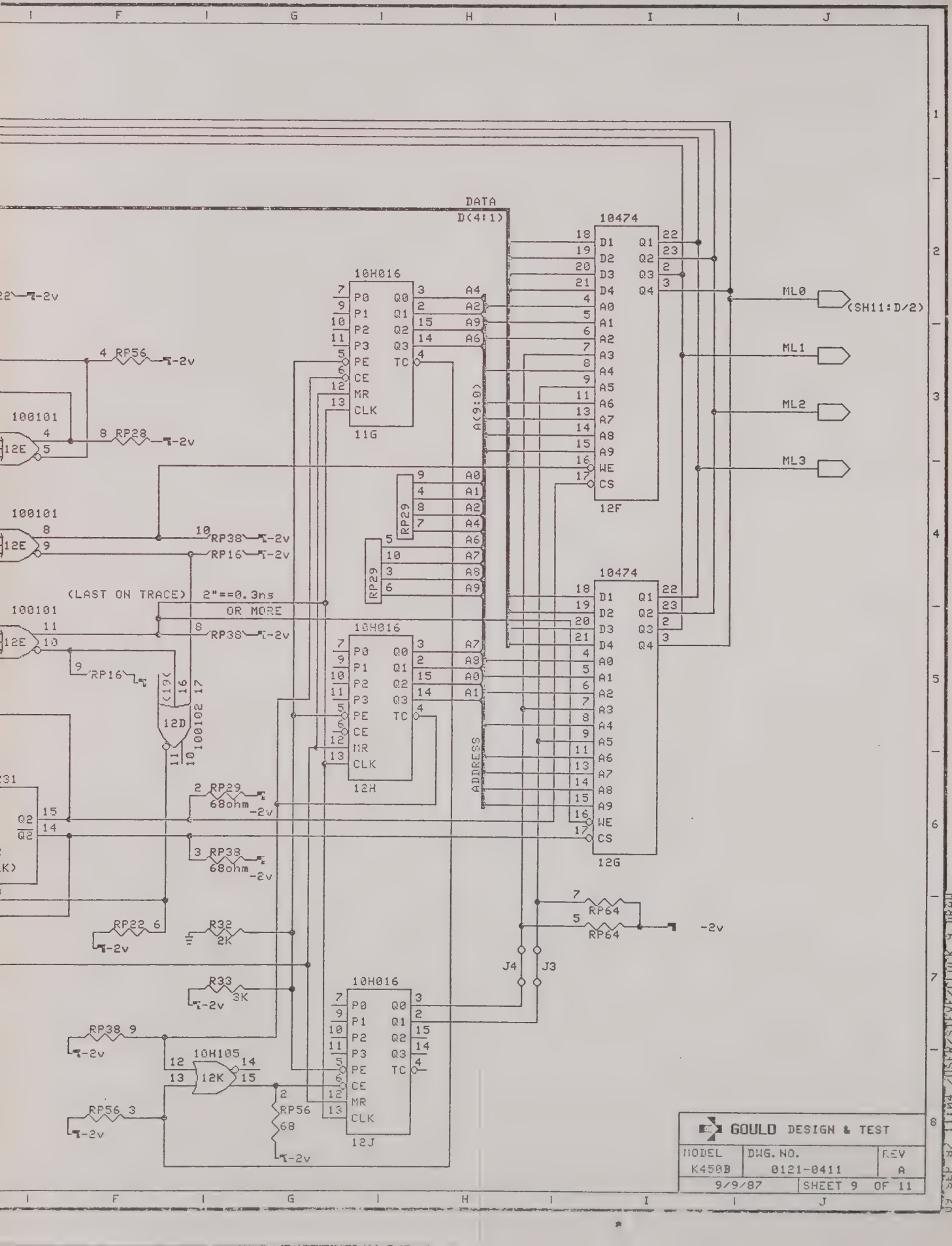


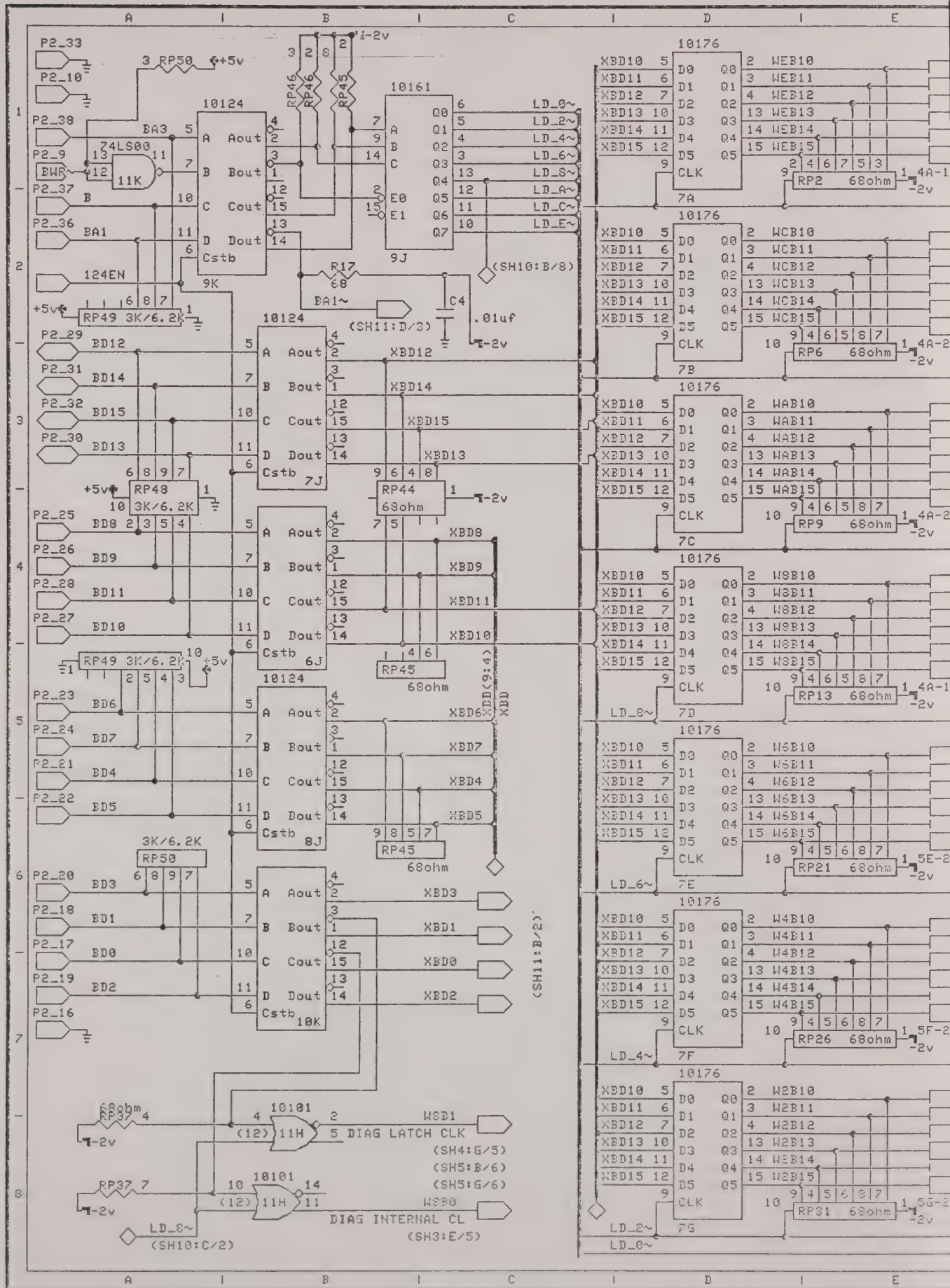
GOULD DESIGN & TEST

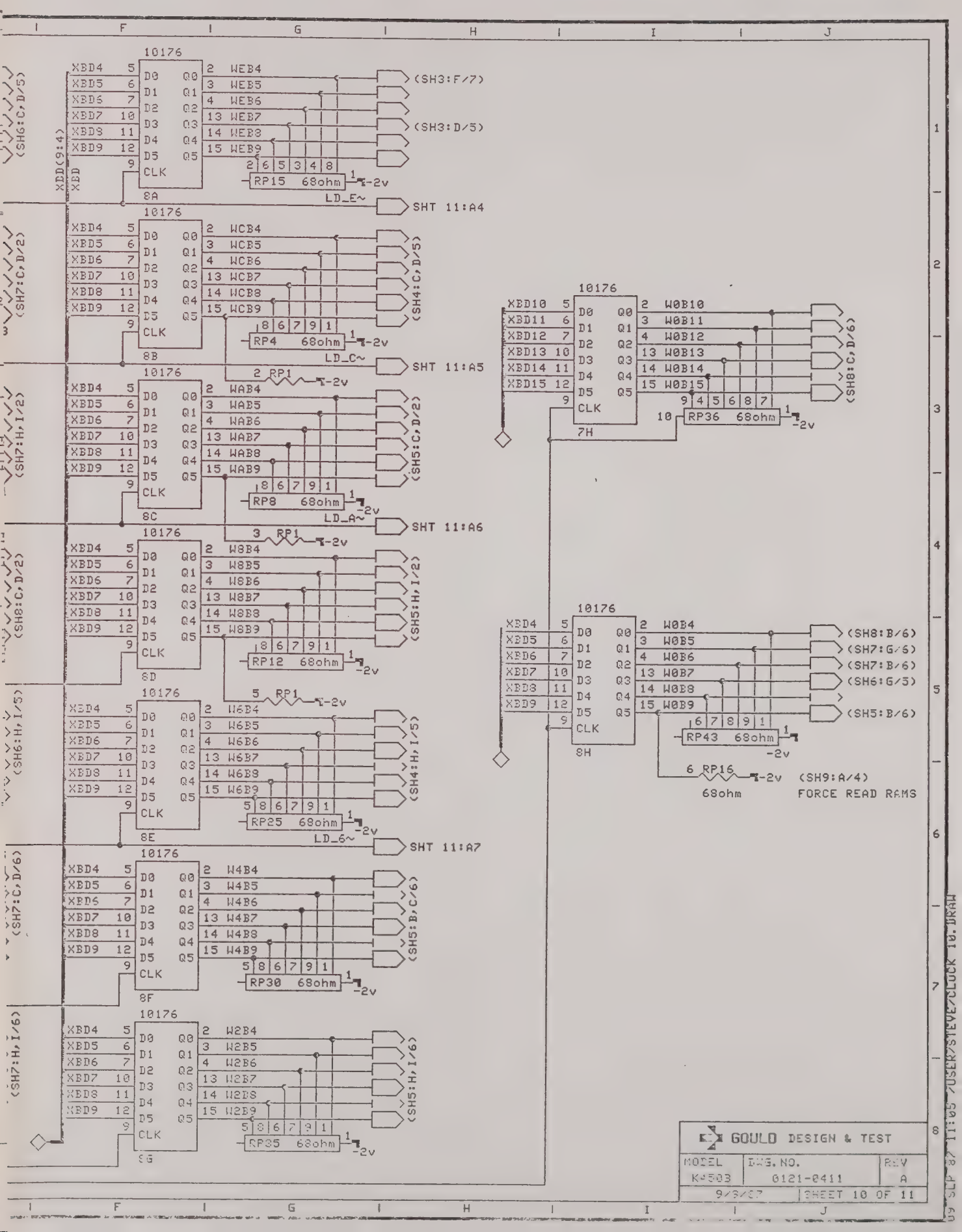
MODEL	DWG. NO.	REV
K4503	0121-0411	A
9/9/'87	SHEET 8 OF 11	

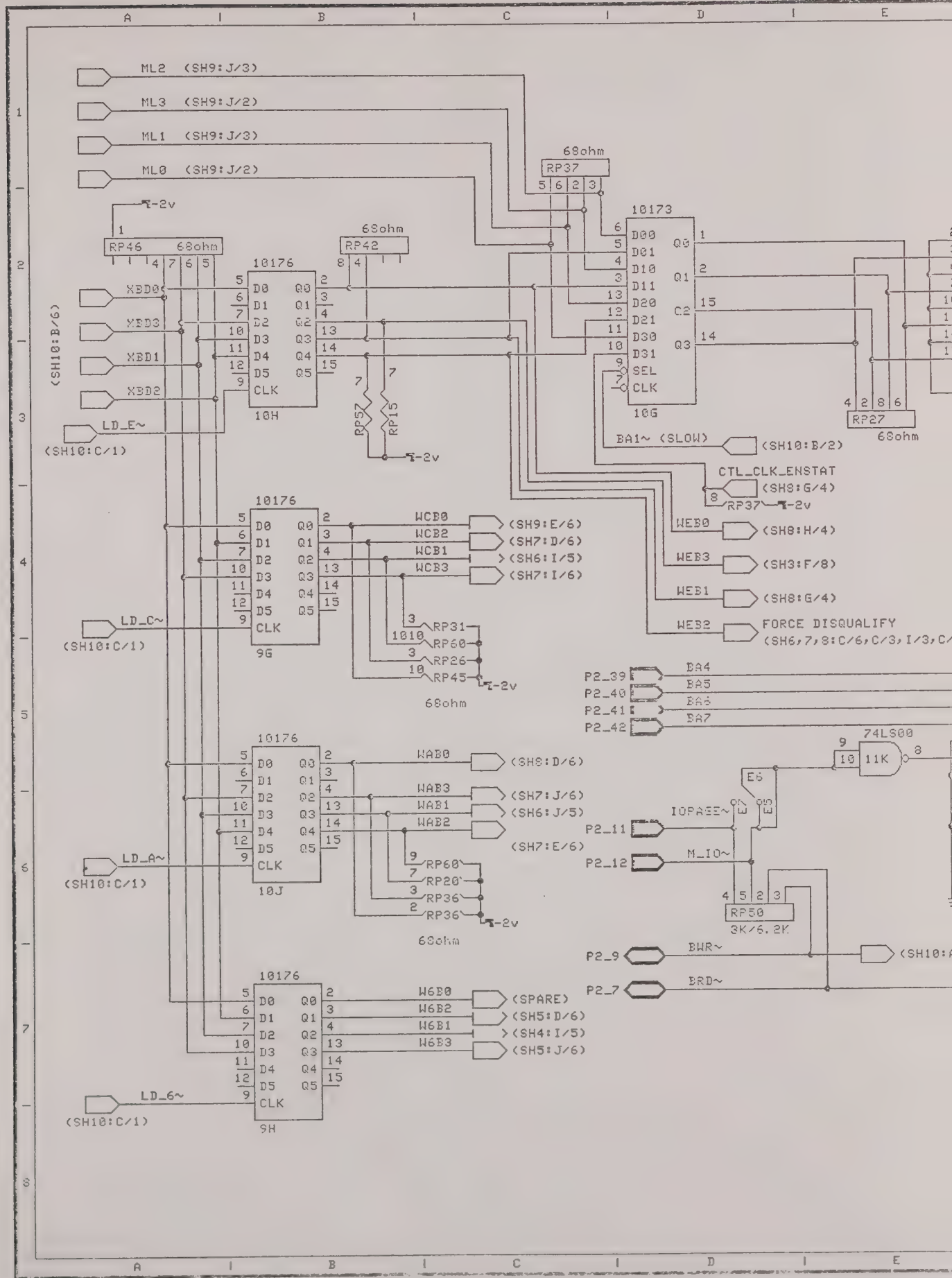
09 SEP 87 11:02 /USER/STEVE/CLOCK 8.DRAW

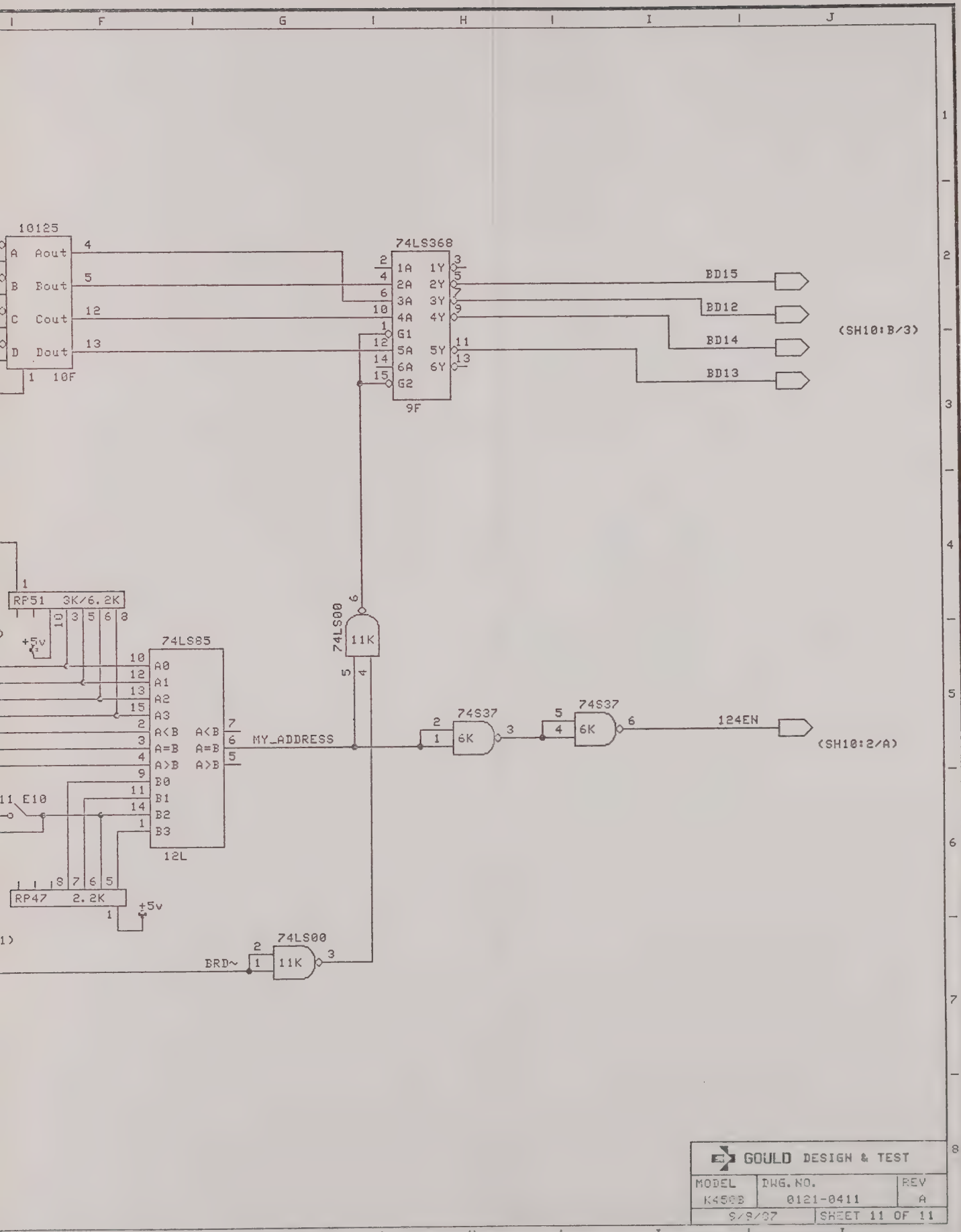

RP22 68ohm
RP56 68ohm
10173
RP28 68ohm
RP38 68ohm
10176
10176
J1_13
J1_17
J1_15
J1_19
L3
L1
L2
L0
J1_9
ARMED
R35 100 -2v
J1_11
R37 120 -2v
11E
11J
11F
RP28 -2v
3 1/2"==0.5ns OR MORE
J1_7
J1_3
TRACE
7 RP16 68ohm -2v
22 100102
(19) 12D
4 RP28 68ohm -2v
W0B9 FORCE READ RAMS
(SH10:J/5)
10109
10D
RP10 -2v
(SH11:B/4)
WCB0
(SH8:C/8)
LEVEL MEMORY ADDRESS RESET
20 100102
CTL_CLK~
RP16
-2v
RP22
E2
E1
J1_5
J1_1
CABLE_CTL_CLK
E4
E3
2 RP16 -2v
100102
(19) 12D
10231
S1
D1
R1
CE1
(CLK)
11D
24 100102
(19) 12D
R5 30
C1 56pf
R6 680 -5.2v
R36 100 -2v
9 RP22 -2v
3 RP22 -2v
J1_2
J1_4
J1_6
J1_8
J1_10
J1_12
J1_14
J1_16
J1_18
J1_20


DATA
D(4:1)
10474
12F
10H016
11G
100101
12E
RP56
RP28
RP38
RP16
(LAST ON TRACE)
2"==0.3ns
OR MORE
12D
100102
RP29
68ohm
-2v
RP22
R32
2K
R33
3K
10H105
12K
RP56
68
12H
12J
12G
ADDRESS
A(9:0)
ML0
ML1
ML2
ML3
(SH11:D/2)
RP64
J4
J3
GOULD DESIGN & TEST
MODEL
K450B
DWG. NO.
0121-0411
REV
A
9/9/87
SHEET 9 OF 11


P2_33
P2_10
3 RP50 +5v
-2v
RP46
RP46
RP45
10161
LD_0~
LD_2~
LD_4~
LD_6~
LD_S~
LD_A~
LD_C~
LD_E~
(SH10:B/8)
9J
10124
P2_38
BA3
Z4LS00
11K
P2_9
BWR
P2_37
B
P2_36
BA1
124EN
9K
R17
68
BA1~
C4
.01uf
(SH11:D/3)
RP49 3K/6.2K
+5v
P2_29
BD12
P2_31
BD14
P2_32
BD15
P2_30
BD13
7J
RP48
3K/6.2K
RP44
68ohm
XBD12
XBD14
XBD15
XBD13
P2_25
BD8
P2_26
BD9
P2_28
BD11
P2_27
BD10
6J
RP45
68ohm
XBD8
XBD9
XBD11
XBD10
XBD(9:4)
XBD
P2_23
BD6
P2_24
BD7
P2_21
BD4
P2_22
BD5
8J
RP43
68ohm
XBD6
XBD7
XBD4
XBD5
3K/6.2K
RP50
P2_20
BD3
P2_18
BD1
P2_17
BD0
P2_19
BD2
P2_16
10K
XBD3
XBD1
XBD0
XBD2
(SH11:B/2)
68ohm
RP37
10101
11H
(12)
W8D1
DIAG LATCH CLK
(SH4:G/5)
(SH5:B/6)
(SH5:G/6)
W8B0
DIAG INTERNAL CL
(SH3:E/5)
LD_8~
(SH10:C/2)
10176
XBD10
XBD11
XBD12
XBD13
XBD14
XBD15
D0
D1
D2
D3
D4
D5
Q0
Q1
Q2
Q3
Q4
Q5
CLK
7A
WEB10
WEB11
WEB12
WEB13
WEB14
WEB15
RP2 68ohm
4A-1
-2v
7B
WCB10
WCB11
WCB12
WCB13
WCB14
WCB15
RP6 68ohm
4A-2
7C
WAB10
WAB11
WAB12
WAB13
WAB14
WAB15
RP9 68ohm
7D
W8B10
W8B11
W8B12
W8B13
W8B14
W8B15
RP13 68ohm
7E
W6B10
W6B11
W6B12
W6B13
W6B14
W6B15
RP21 68ohm
5E-2
7F
W4B10
W4B11
W4B12
W4B13
W4B14
W4B15
RP26 68ohm
5F-2
7G
W2B10
W2B11
W2B12
W2B13
W2B14
W2B15
RP31 68ohm
5G-2
LD_2~
LD_0~


10176
XBD4
XBD5
XBD6
XBD7
XBD8
XBD9
XBD(9:4)
XBD
D0
D1
D2
D3
D4
D5
CLK
Q0
Q1
Q2
Q3
Q4
Q5
WEB4
WEB5
WEB6
WEB7
WEB8
WEB9
(SH3:F/7)
(SH3:D/5)
RP15 68ohm
-2v
8A
LD_E~
SHT 11:A4
(SH6:C,D/5)
WCB4
WCB5
WCB6
WCB7
WCB8
WCB9
(SH4:C,D/5)
RP4 68ohm
8B
LD_C~
SHT 11:A5
(SH7:C,D/2)
RP1
WAB4
WAB5
WAB6
WAB7
WAB8
WAB9
(SH5:C,D/2)
RP8 68ohm
8C
LD_A~
SHT 11:A6
(SH7:H,I/2)
W8B4
W8B5
W8B6
W8B7
W8B8
W8B9
(SH5:H,I/2)
RP12 68ohm
8D
(SH8:C,D/2)
W6B4
W6B5
W6B6
W6B7
W6B8
W6B9
(SH4:H,I/5)
RP25 68ohm
8E
LD_6~
SHT 11:A7
(SH6:H,I/5)
W4B4
W4B5
W4B6
W4B7
W4B8
W4B9
(SH5:B,C/6)
RP30 68ohm
8F
(SH7:C,D/6)
W2B4
W2B5
W2B6
W2B7
W2B8
W2B9
(SH5:H,I/6)
RP35 68ohm
8G
(SH7:H,I/6)
XBD10
XBD11
XBD12
XBD13
XBD14
XBD15
W0B10
W0B11
W0B12
W0B13
W0B14
W0B15
(SH8:C,D/6)
RP36 68ohm
7H
W0B4
W0B5
W0B6
W0B7
W0B8
W0B9
(SH8:B/6)
(SH7:G/6)
(SH7:B/6)
(SH6:G/5)
(SH5:B/6)
RP43 68ohm
8H
RP16
68ohm
(SH9:A/4)
FORCE READ RAMS
GOULD DESIGN & TEST
MODEL K4503
DWG. NO. 0121-0411
REV A
9/3/87
SHEET 10 OF 11
09 SEP 87 11:05 /USER/STEVE/CLOCK10.DRAW


ML2 (SH9:J/3)
ML3 (SH9:J/2)
ML1 (SH9:J/3)
ML0 (SH9:J/2)
68ohm
RP37
10173
-2v
RP46 68ohm
68ohm
RP42
10176
XBD0
XBD3
XBD1
XBD2
(SH10:B/6)
LD_E~
(SH10:C/1)
10H
RP57
RP15
-2v
BA1~ (SLOW)
(SH10:B/2)
CTL_CLK_ENSTAT
(SH8:G/4)
RP37
-2v
10G
RP27
68ohm
WEB0
(SH8:H/4)
WEB3
(SH3:F/8)
WEB1
(SH8:G/4)
WEB2
FORCE DISQUALIFY
(SH6,7,8:C/6,C/3,I/3,C/
10176
WCB0
WCB2
WCB1
WCB3
(SH9:E/6)
(SH7:D/6)
(SH6:I/5)
(SH7:I/6)
LD_C~
(SH10:C/1)
9G
RP31
RP60
RP26
RP45
-2v
68ohm
P2_39
P2_40
P2_41
P2_42
BA4
BA5
BA6
BA7
74LS00
11K
E6
IOPASE~
M_IO~
P2_11
P2_12
RP50
3K/6.2K
10176
WAB0
WAB3
WAB1
WAB2
(SH8:D/6)
(SH7:J/6)
(SH6:J/5)
(SH7:E/6)
LD_A~
(SH10:C/1)
10J
RP60
RP20
RP36
RP36
-2v
68ohm
P2_9
BWR~
P2_7
BRD~
10176
W6B0
W6B2
W6B1
W6B3
(SPARE)
(SH5:D/6)
(SH4:I/5)
(SH5:J/6)
LD_6~
(SH10:C/1)
9H



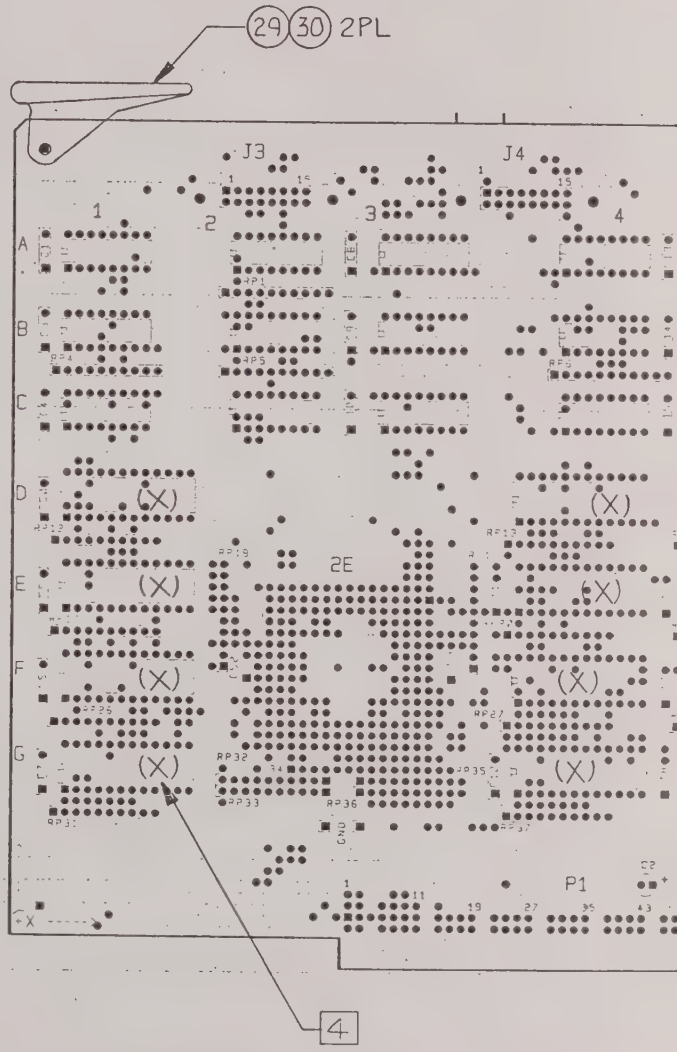
GOULD DESIGN & TEST

MODEL	DWG. NO.	REV
K450B	0121-0411	A
9/8/87	SHEET 11 OF 11	

09 SEP 87 11:08 /USER/STEVE/CLOCK 11.DRAW

DRAWING NUMBER
0121-0415

DRAWING NUMBER



(NOTES CONT. ON SHT 2)

4 (X) INDICATES SOCKET LOCATIONS-REF ONLY.

3. MANUFACTURE PER GOULD WORKMANSHIP STD. 87000012.

2. ASSY. REFLECTS SCHEM DWG 0121-0416 & FAB DWN 0121-0417

1 MARK ASSY. DASH NO. REV & SERIAL NO. APPROX. WHERE SHO USING CONTRASTING INDELIBLE INK.

NOTES: (UNLESS OTHERWISE SPECIFIED)

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	51	5600	PILOT RELEASE PER ECO #	MM	DGW	5/6/87
	52	5703	REVISED PER ECO 6/2/87	MM	DGW	6/4/87
	53	5721	REV ROLL ONLY 6/11/87	MM	DGW	6/15/87
	54	5756	REV ROLL ONLY 7/20/87	MM		

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT.
SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES, XX ± .020 ± 1°, XXX ± .010
HOLE SIZE: .0-.599 ± .003, .600-.999 ± .004, 1.000-1.499 ± .005

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DRAWN	MM	DATE 4/21/87
CHECKED	DGW	5/6/87
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		
ENG. SERV.		DATE

GOULD Instruments Division Santa Clara Operations

TITLE: ASSY, DATA BD K450B

SCALE	SIZE	PART NUMBER	REV
	C	0121-0415	54

MODEL K450 B SHEET 1 OF 3

DRAWING NUMBER

0121-0415 p.243

DRAWING NUMBER

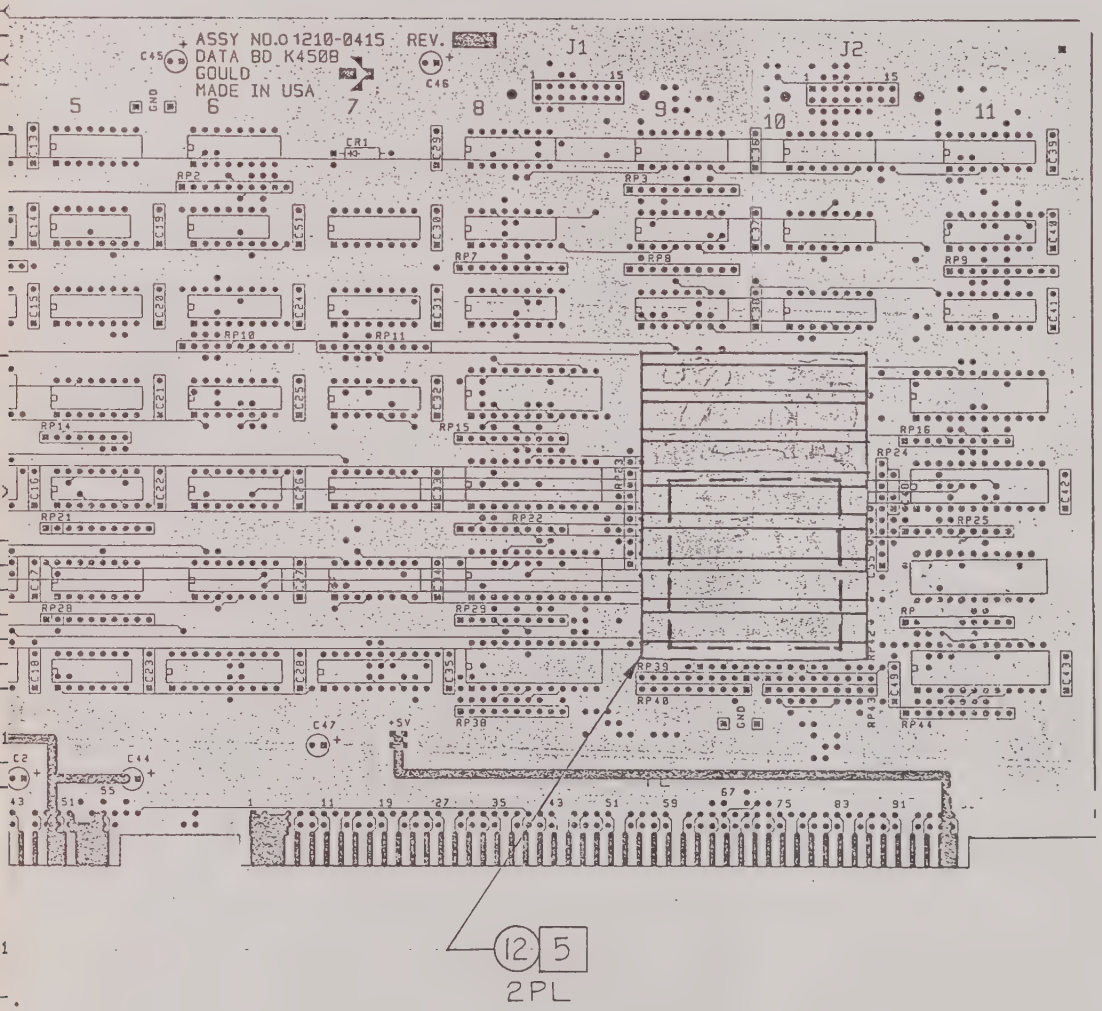
NOTES:

5 SEE SHT 3 FOR HEAT SINK INSTALLATION INSTRUCTION

D C B A

4 3

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: .X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: 0.599 ± .003, 600.359 ± .004, 1.000 1.499 ± .005

DASH NO.	NUMBER NEXT ASSEMBLY	QTY

ENG. SERV.		DATE
DRAWN		DATE
CHECKED		
PROJ. ENG.		
MANUFACTURING		
QUALITY ASSUR		

GOULD Instruments Division Santa Clara Operations

TITLE: ASSY. DATA BD. K450B

SCALE	SIZE	PART NUMBER	REV
	C	0121-0415	54

MODEL K450 B SHEET 2 OF 3

DRAWING NUMBER 0121-0415 P.3 of 3

DRAWING NUMBER

INSTRUCTIONS FOR APPLICATION AND CURING OF HEAT SINK ADHESIVE FOR K450B DATA BOARD 0121-0415-10,-20 HEAT SINK:

WARNING: GROUND STRAPS MUST BE WORN AT ALL TIMES WHEN HANDLING THE GATE ARRAYS TO PREVENT ELECTROSTATIC DISCHARGE !!!

1. Mavidon 1134 Heat Sink Adhesive consists of two parts, 1134A blue paste and 1134B amber liquid, contained in a single cartridge.

2. Before applying the adhesive, be certain that the surface of the gate array and of the heat sink are clean and free of any contamination; wipe with Freon.

3. Position the Heat Sink 0121-0419-10 with the fins facing down on a flat work surface per detail 2.

4. Apply a thin layer of adhesive, approximately .005 inches, to the surface of the round cap on the gate array. Align the gate array in the proper position per detail 1. Firmly press the gate array into place to ensure excess adhesive "squeezes" out.

   NOTE THE ORIENTATION OF THE GATE ARRAY PER DETAIL 1.

5. The cure time is as follows:

   a. 24 hours at room temperature; OR

   b. 2 hours at 60 degrees centigrade.

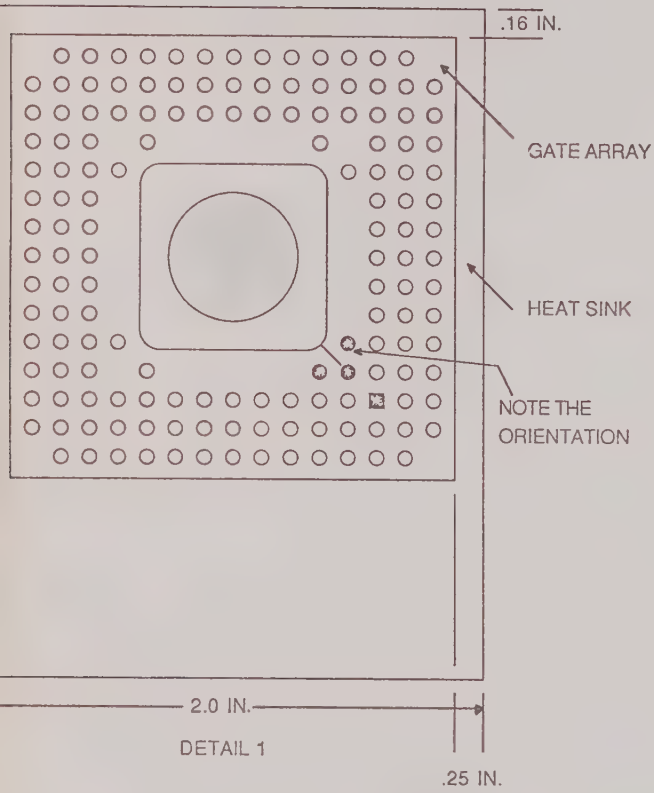
   CARE SHOULD BE TAKEN TO MAINTAIN THE POSITION OF THE GATE ARRAY DURING THE CURE CYCLE.

2.682 IN.

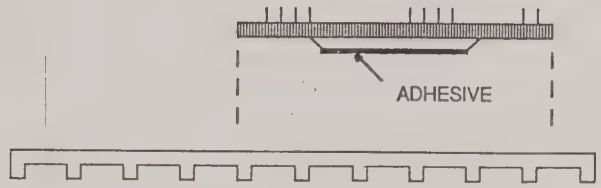
NOTE:

NOTES: (UNLESS OTHERWISE SPECIFIED)

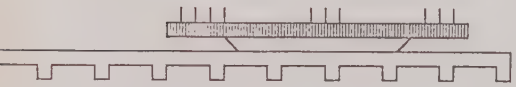
REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE



DETAIL 1



DETAIL 2



COMPLETED ASSEMBLY

NOT TO SCALE

-05	-04	-03	-02	-01	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES; .XX ± .020 ± 1°; .XXX ± .010

HOLE SIZE: .0-.599 ± .003; .600-.999 ± .004; 1.000-1.499 ± .005

DRAWN	DATE
CHECKED	
PROJ. ENG.	
MANUFACTURING	
QUALITY ASSUR	
ENG. SERV.	DATE

GOULD Instruments Division Santa Clara Operations

TITLE: ASSY, DATA BD. K450B

SCALE	SIZE	PART NUMBER	REV
	C	0121-0415	54

MODEL K450 B SHEET 3 OF 3

BILL OF MATERIAL

AS OF 10/30/87

0121-0415-10 ASSY,PCB,DATA,32 CH,K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0416	DWG,SCHEMATIC DATA BD K450B	0	EA	REF
0	D0121-0415	DWG,ASSY,PCB,DATA K450B	0	EA	REF
1	0121-0417-10	FAB,PCB,DATA BD,K450B	1	EA	
2	9000-5120-10	IC SCX36165GW01 GATE ARRAY	2	EA	2E,9E
3	1850-0147-20	IC HM10474-10,RAM,1KX4 ACC.T	16	EA	11D,11E, 11F,11G 1D,1E,1F, 1G,4D,4E, 4F,4G,8D 8E,8F,8G
4	1850-0131-10	IC MC10H016L B/N COUNTER	12	EA	11A,11B, 11C 1A,1B,1C, 4A,4B,4C, 8A,8B,8C,
5	1000-0026-10	DIO 1N4148	1	EA	CR1
6	1850-0128-10	IC MC10H176 HEX MAST SLAV D FF	12	EA	10A,10B, 10C 2A,2B,2C, 3A,3B,3C, 9A,9B,9C,
7	1850-0021-10	IC MC10124L QUAD MTTL	6	EA	5D,5E,6C, 6D,7C,7D
8	1850-0014-10	IC MC10125F/L QUAD MECL	4	EA	6E,6F,7E, 7F
9	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	2	EA	6G,7G
10	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	5G
11	1800-0290-10	IC 74S85N 4-BIT MAG COMP	1	EA	5F
12	0121-0419-10	HEATSINK,K450B	2	EA	@2E,9E
13	1800-0278-10	IC 74LS155N DUAL 2 TO 4	1	EA	5C
14	1800-0115-10	IC 74LS74N, 14, FF, D, X2	1	EA	5B
15	1800-0280-10	IC 74S37N BUFFER/CLK DR	1	EA	6B
16	1850-0151-10	IC IOH103,ECL,QUAD 2-1N OR GAT	1	EA	6A
17	8200-0040-10	ADHESIVE,HEAT SINK, MAVIDON	0	ST	
18	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	5	EA	C2,C44-47
19	4000-0073-10	CAP,.01UF,50V,AXIAL T & R	50	EA	C1,3,5-43 C4 C48-55
21	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	2	EA	RP21,28
22	3700-0080-10	RPAK,100,0.3W,2%,10/9	31	EA	RP1-13, RP15-20, RP22-27, RP29-31 RP37,38 RP44
23	3700-0039-10	RPAK,56,0.18W,2%,10/9	8	EA	RP32,33,35

BILL OF MATERIAL
AS OF 10/30/87

0121-0415-10 ASSY,PCB,DATA,32 CH,K450B
MODEL K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
23	3700-0039-10	RPAK,56,0.18W,2%,10/9	8	EA	RP36,39, RP40,42,43
24	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	1	EA	RP14
25	3700-0094-10	RPAK 75 OHM .18W 2% 10 P	2	EA	RP34,41
26	6000-0374-10	CONN 16 PIN HDR RT ANGLE	4	EA	J1-4
27	0121-0409-10	FAB,PCB,SMD CAP,K450B	2	EA	2E,9E
28	6100-0137-10	SKT 24 PIN DIP LOW PRO	16	EA	X11E,X11F, X11G, X1D,X1E, X1F,X1G, X4D,X4E, X4F,X4G, X8D,X8E, X8F, X8G,X11D,
29	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
30	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	

BILL OF MATERIAL

AS OF 10/30/87

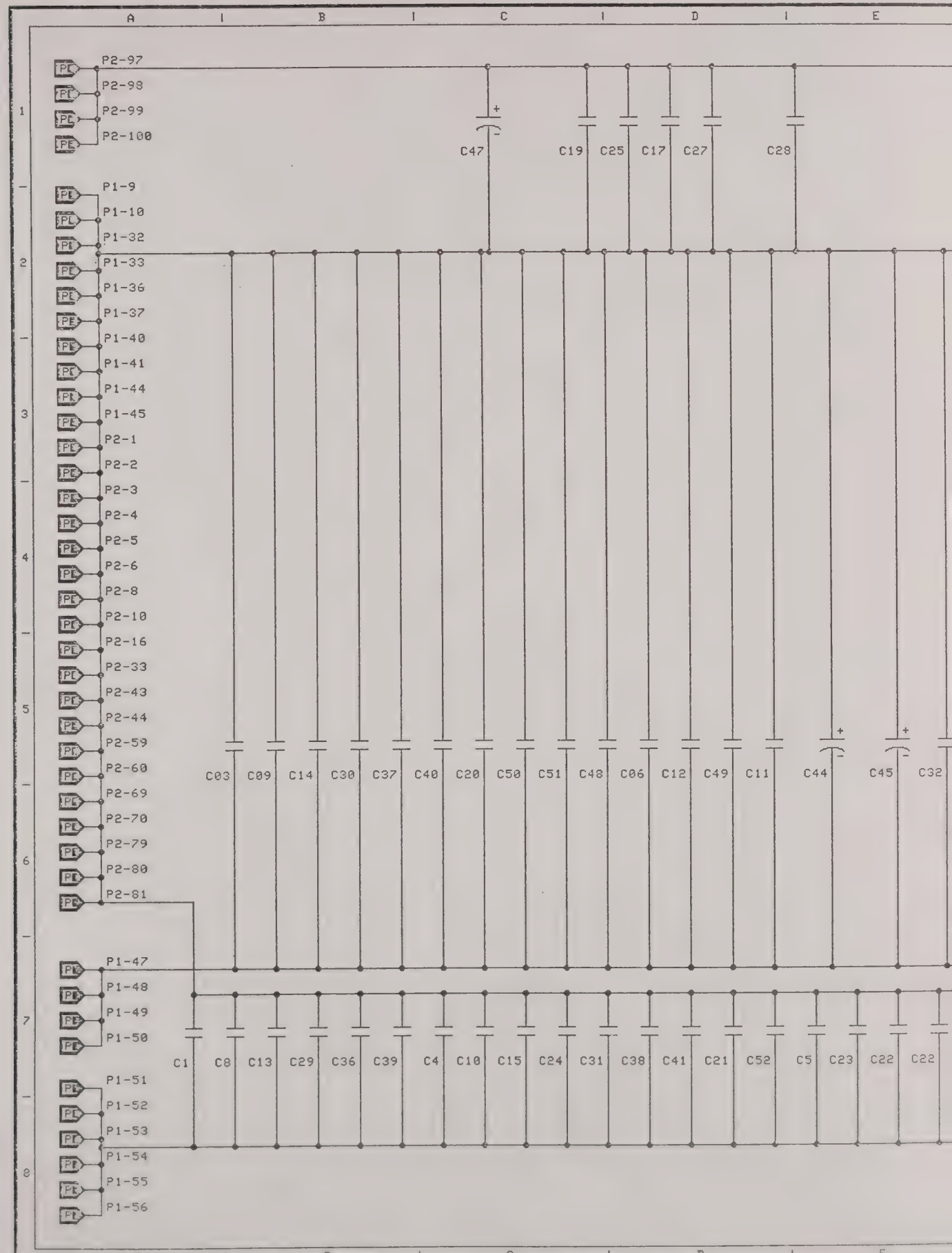
0121-0415-20 2ASSY,PCB,DATA,16 CH, K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0416	DWG,SCHEMATIC DATA BD K450B	0	EA	REF
0	D0121-0415	DWG,ASSY,PCB,DATA K450B	0	EA	REF
1	0121-0417-10	FAB,PCB,DATA BD.K450B	1	EA	
2	9000-5120-10	IC SCX36165GW01 GATE ARRAY	1	EA	9E
3	1850-0147-20	IC HM10474-10,RAM,1KX4 ACC.T	8	EA	11F,11G 8D,8E,8F 8G,11D,11E
4	1850-0131-10	IC MC10H016L B/N COUNTER	6	EA	11A,11B, 11C 8A,8B,8C,
5	1000-0026-10	DIO 1N4148	1	EA	CR1
6	1850-0128-10	IC MC10H176 HEX MAST SLAV D FF	6	EA	10A,10B, 10C 9A,9B,9C,
7	1850-0021-10	IC MC10124L QUAD MTTL	6	EA	5D,5E,6C, 6D,7C,7D
8	1850-0014-10	IC MC10125P/L QUAD MECL	4	EA	6E,6F,7E, 7F
9	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	2	EA	6G,7G
10	1800-0123-10	IC 74LS14N HEX SCHMITT	1	EA	5G
11	1800-0290-10	IC 74S85N 4-BIT MAG COMP	1	EA	5F
12	0121-0419-10	HEATSINK,K450B	1	EA	@9E
13	1800-0278-10	IC 74LS155N DUAL 2 TO 4	1	EA	5C
14	1800-0115-10	IC 74LS74N, 14, FF, D, X2	1	EA	5B
15	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	6B
16	1850-0151-10	IC IOH103,ECL,QUAD 2-1N OR GAT	1	EA	6A E
17	8200-0040-10	ADHESIVE,HEAT SINK, MAVIDON	0	ST	
18	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	5	EA	C2,C44,C45 C46,C47
19	4000-0073-10	CAP,.01UF,50V,AXIAL T & R	37	EA	54,55,12 C13-43, C48,49,51
21	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	2	EA	RP21,RP28
22	3700-0080-10	RPAK,100,0.3W,2%,10/9	17	EA	RP15,16 RP2,3 RP22-25 RP29,30 RP38,44 RP7-11
23	3700-0039-10	RPAK,56,0.18W,2%,10/9	4	EA	RP39,RP40 RP42,RP43
24	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	1	EA	RP14

BILL OF MATERIAL
AS OF 10/30/87

0121-0415-20 2ASSY,PCB,DATA,16 CH, K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
25	3700-0094-10	RPAK 75 OHM .18W 2% 10 P	2	EA	RP34,41
26	6000-0374-10	CONN 16 PIN HDR RT ANGLE	2	EA	J1,J2
27	0121-0409-10	FAB,PCB,SMD CAP,K450B	1	EA	9E
28	6100-0137-10	SKT 24 PIN DIP LOW PRO	8	EA	X11D,X11E, X11F,X11G X8D,X8E, X8F,X8G
29	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
30	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	


A
B
C
D
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1
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6
7
8
P2-97
P2-98
P2-99
P2-100
P1-9
P1-10
P1-32
P1-33
P1-36
P1-37
P1-40
P1-41
P1-44
P1-45
P2-1
P2-2
P2-3
P2-4
P2-5
P2-6
P2-8
P2-10
P2-16
P2-33
P2-43
P2-44
P2-59
P2-60
P2-69
P2-70
P2-79
P2-80
P2-81
P1-47
P1-48
P1-49
P1-50
P1-51
P1-52
P1-53
P1-54
P1-55
P1-56
C47
C19
C25
C17
C27
C28
C03
C09
C14
C30
C37
C40
C20
C50
C51
C48
C06
C12
C49
C11
C44
C45
C32
C1
C8
C13
C29
C36
C39
C4
C10
C15
C24
C31
C38
C41
C21
C52
C5
C23
C22
C22

REVISIONS

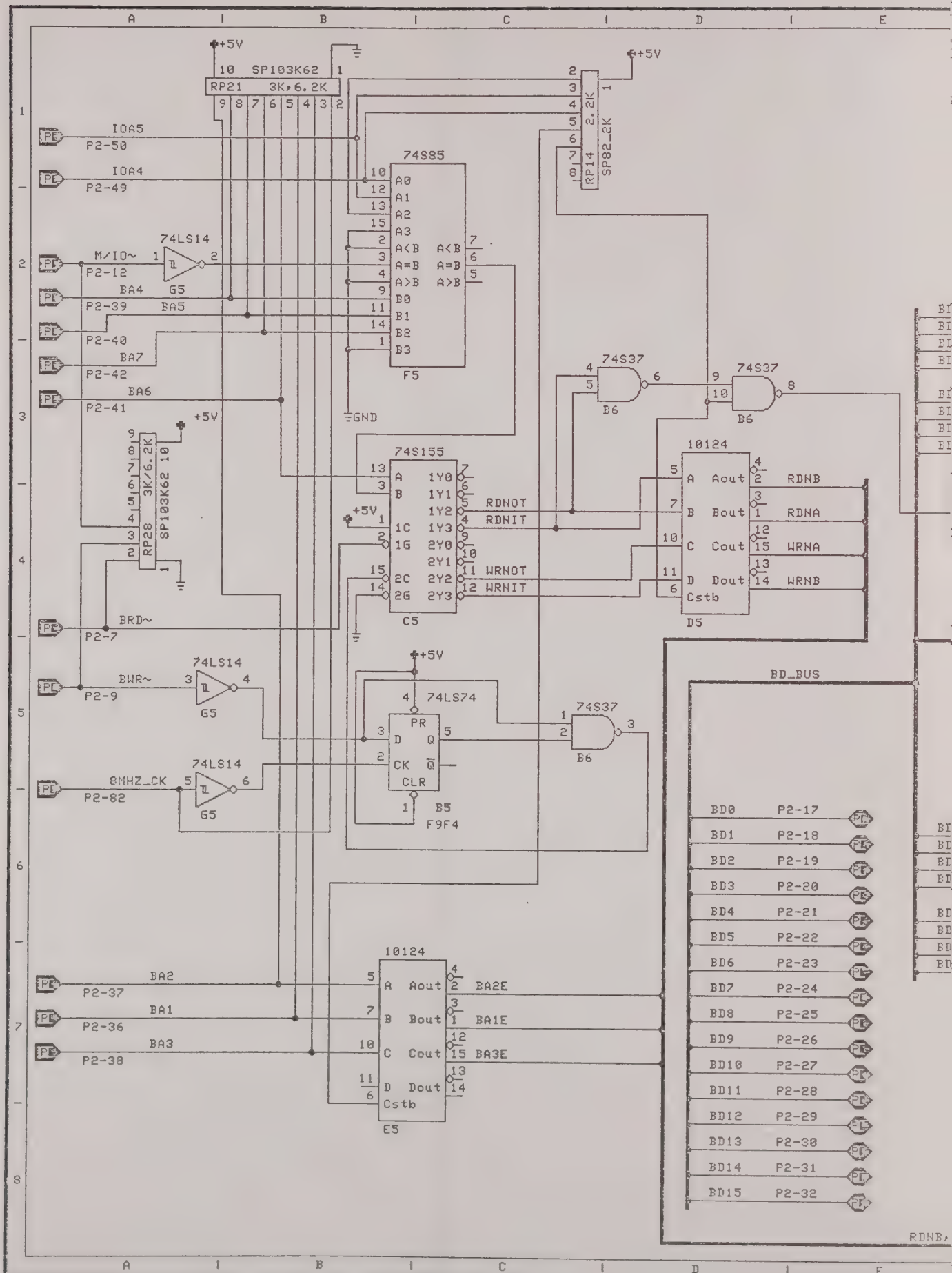
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE
4:A6 6:A6	53	5721	CHANGE RP 34 & 41 TO 75 OHM FROM 150 OHM	SM			6-87
4:C1 6:C1	54	5756	ADD 49 Pfd CAPS TO E2 & E9 Q0 THROUGH Q15 OUTPUTS	SM			7-87

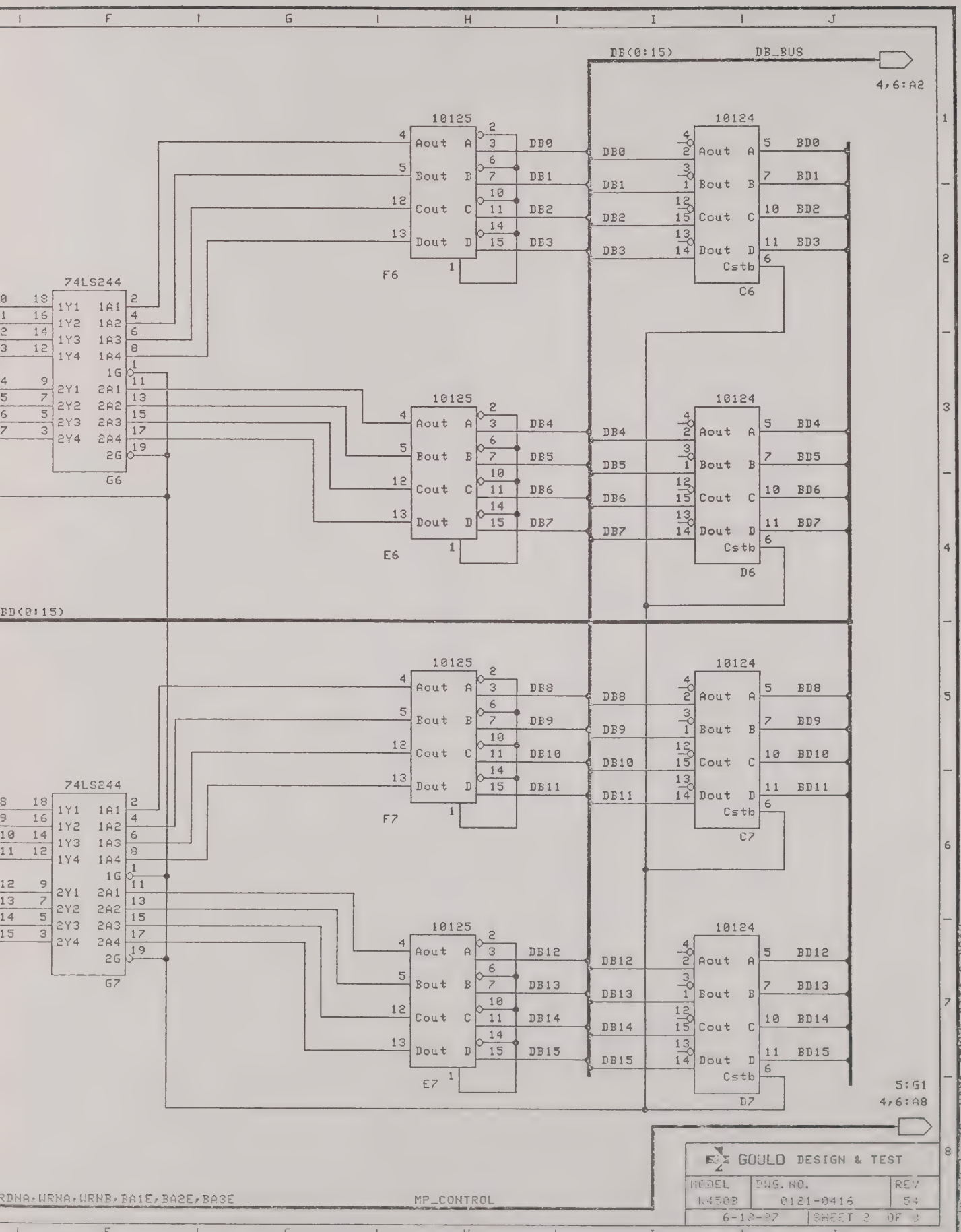
NOTE: THIS DOCUMENT IS TO REFERENCE THE REWORK TO DATA BOARDS DATING MAY87-SEPT87 INVOLVING THE 0121-0409-10 FAB, PCB, SMD CAP RETROFIT.

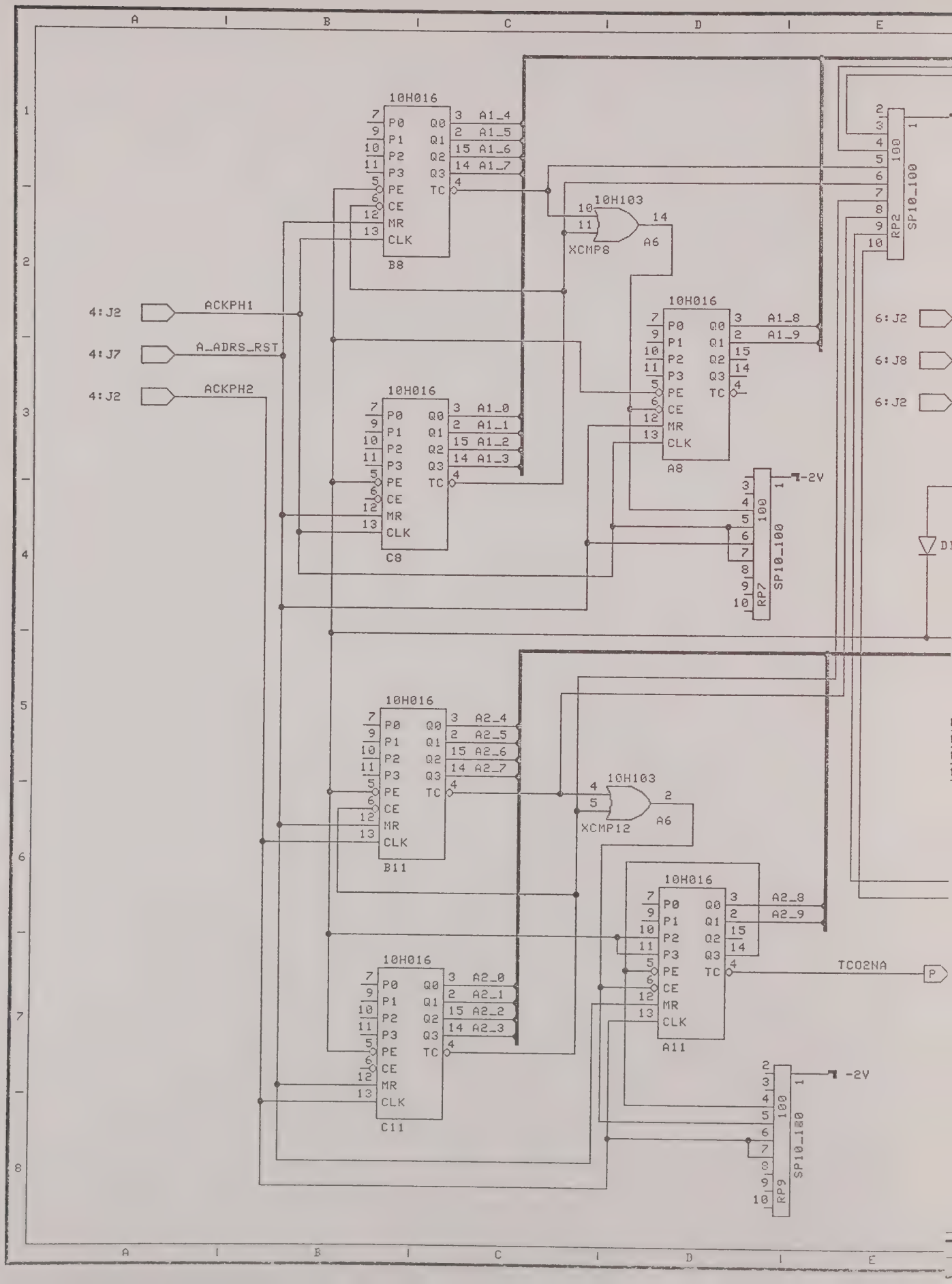
DRAWN STEVE MEIERS	DATE 6-87	GOULD DESIGN & TEST		
PROJ. ENGR PAUL DRAPKIN	6-87	TITLE DATA BOARD		
MANUFACTURING				
QUALITY ASSUR		MODEL K450B	PART NUMBER 0121-0416	REV 54
ECO NO.		7-7-87	SHEET 1 OF 8	

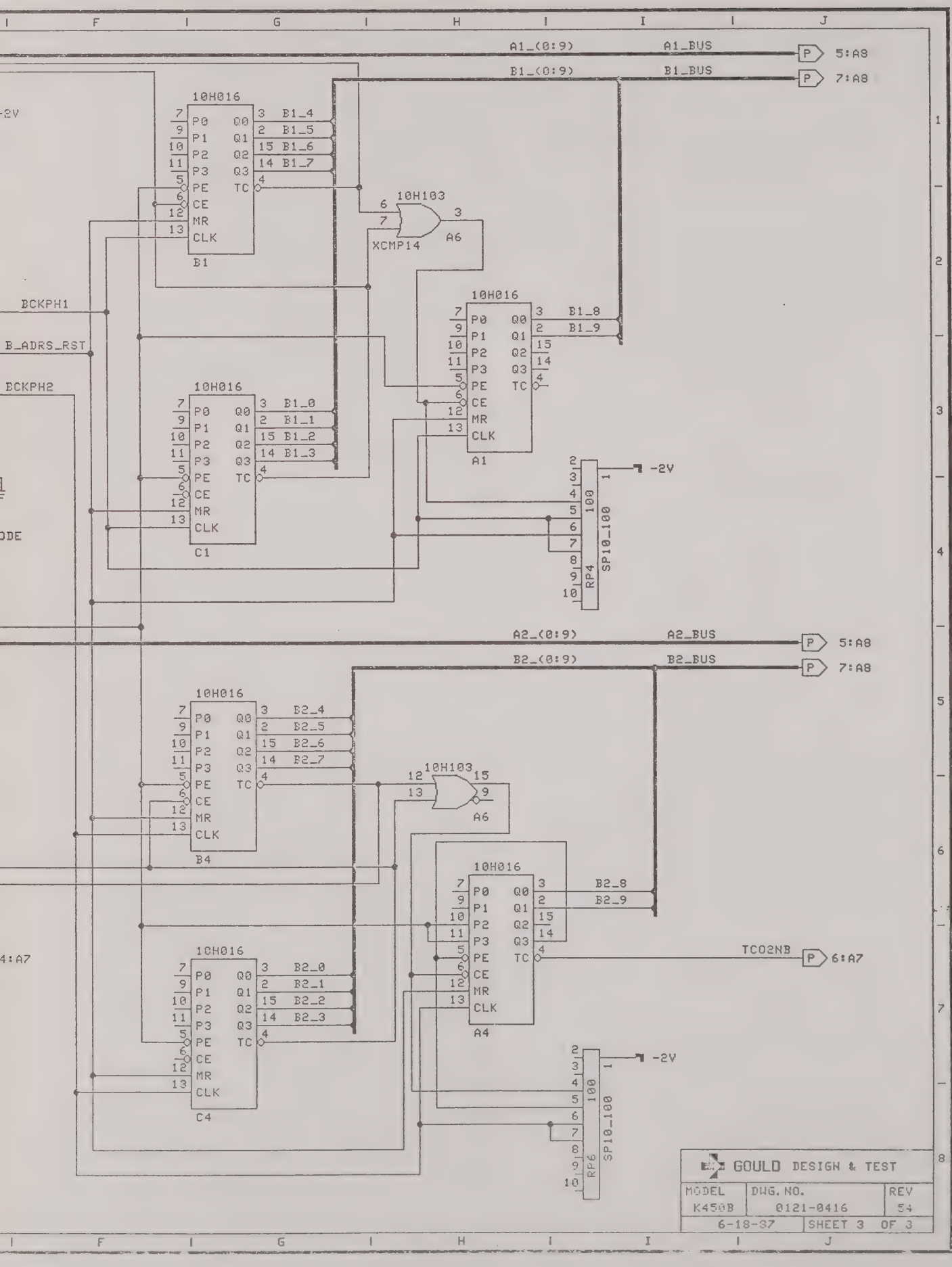
DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	

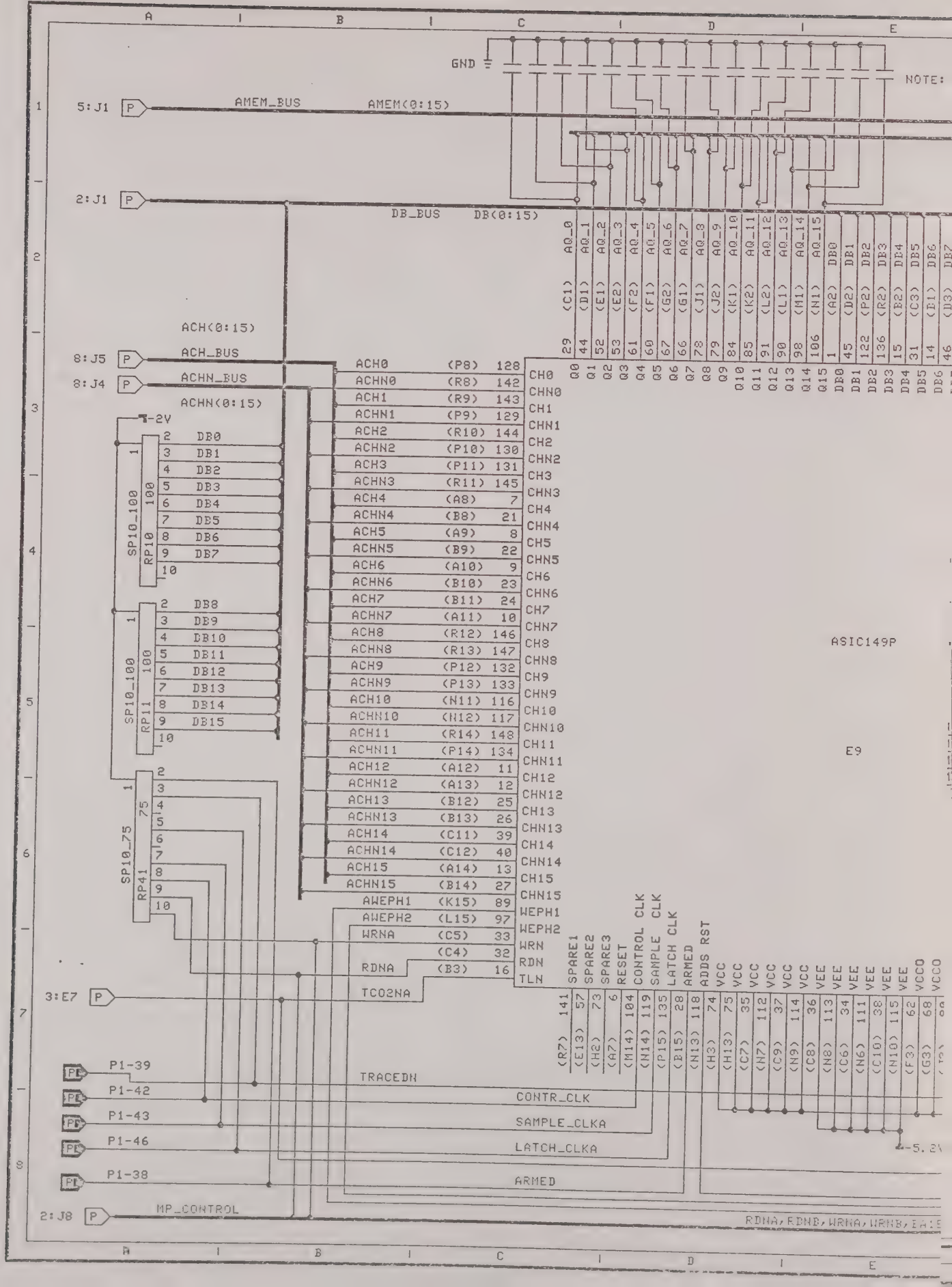
14 JUL 87 10:34 /USER/STEVE/DATA 1. DRAW

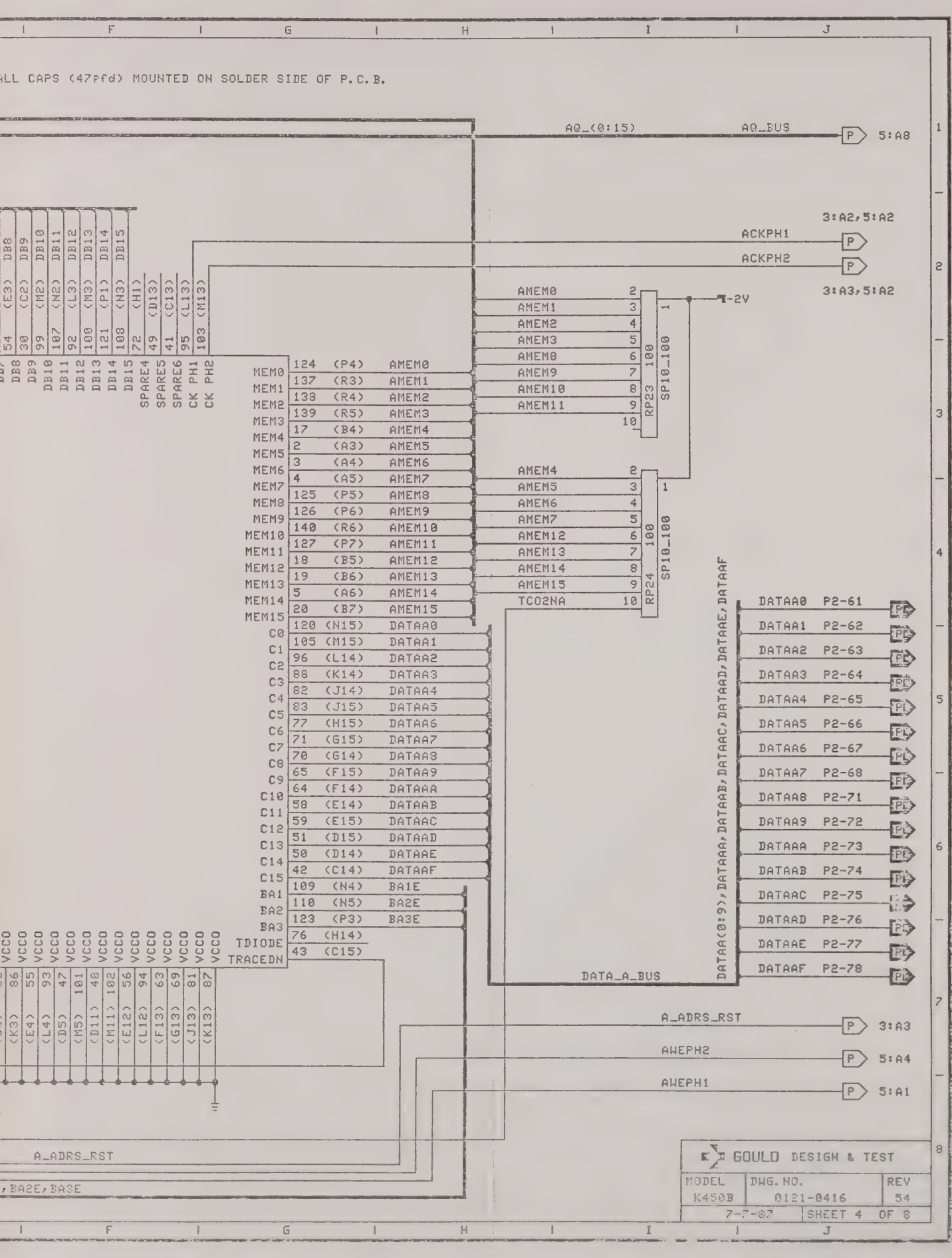

+5V
SP103K62
RP21
3K,6.2K
IOA5
P2-50
IOA4
P2-49
74S85
A0
A1
A2
A3
A<B
A=B
A>B
B0
B1
B2
B3
F5
74LS14
M/IO~
P2-12
G5
BA4
P2-39
BA5
P2-40
BA7
P2-42
BA6
P2-41
GND
RP14
2.2K
SP82_2K
74S37
B6
74S155
1Y0
1Y1
1Y2
1Y3
2Y0
2Y1
2Y2
2Y3
1C
1G
2C
2G
C5
RDNOT
RDNIT
WRNOT
WRNIT
10124
Aout
Bout
Cout
Dout
Cstb
D5
RDNB
RDNA
WRNA
WRNB
RP28
BRD~
P2-7
BWR~
P2-9
74LS74
PR
D
CK
Q
CLR
B5
F9F4
8MHZ_CK
P2-82
BD_BUS
BD0
P2-17
BD1
P2-18
BD2
P2-19
BD3
P2-20
BD4
P2-21
BD5
P2-22
BD6
P2-23
BD7
P2-24
BD8
P2-25
BD9
P2-26
BD10
P2-27
BD11
P2-28
BD12
P2-29
BD13
P2-30
BD14
P2-31
BD15
P2-32
BA2
P2-37
BA1
P2-36
BA3
P2-38
BA2E
BA1E
BA3E
E5
RDNB,

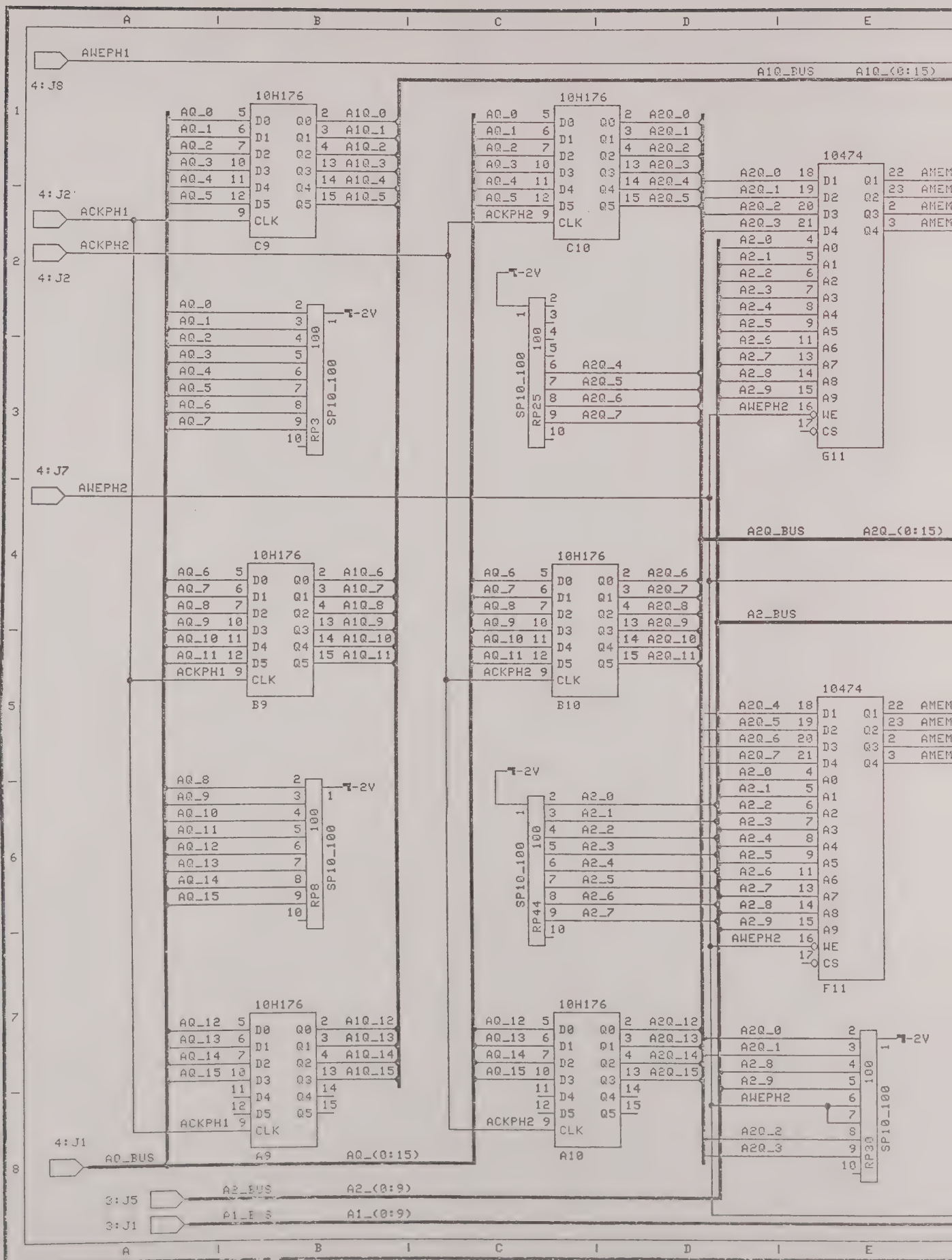

DB(0:15)
DB_BUS
4,6:A2
10125
10124
74LS244
F6
C6
E6
D6
G6
F7
C7
E7
D7
G7
Aout
Bout
Cout
Dout
Cstb
1Y1 1Y2 1Y3 1Y4
1A1 1A2 1A3 1A4
2Y1 2Y2 2Y3 2Y4
2A1 2A2 2A3 2A4
1G
2G
BD(0:15)
5:G1
4,6:A8
RDNA,WRNA,WRNB,BA1E,BA2E,BA3E
MP_CONTROL
GOULD DESIGN & TEST
MODEL
K450B
DWG. NO.
0121-0416
REV
54
6-10-87
SHEET 2 OF 3
14 JUL 87 10:35 /USER/STEVE/DATA 2.DRW

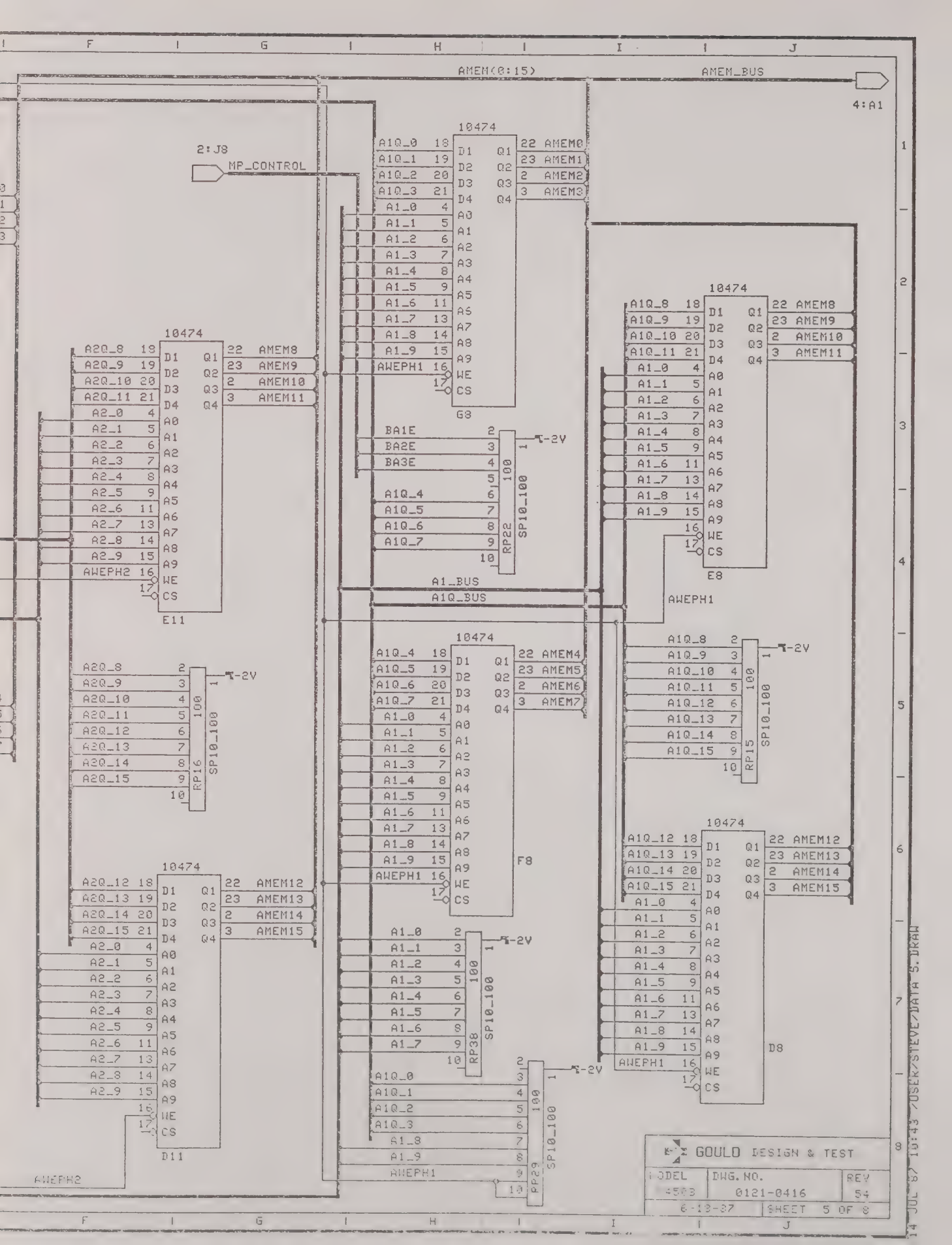

10H016
B8
A1_4
A1_5
A1_6
A1_7
10H103
XCMP8
A6
10H016
A8
A1_8
A1_9
10H016
C8
A1_0
A1_1
A1_2
A1_3
4:J2
ACKPH1
4:J7
A_ADRS_RST
4:J2
ACKPH2
-2V
SP10_100
RP7
RP2
6:J2
6:J8
6:J2
10H016
B11
A2_4
A2_5
A2_6
A2_7
10H103
XCMP12
A6
10H016
A11
A2_8
A2_9
TCO2NA
10H016
C11
A2_0
A2_1
A2_2
A2_3
-2V
SP10_100
RP9

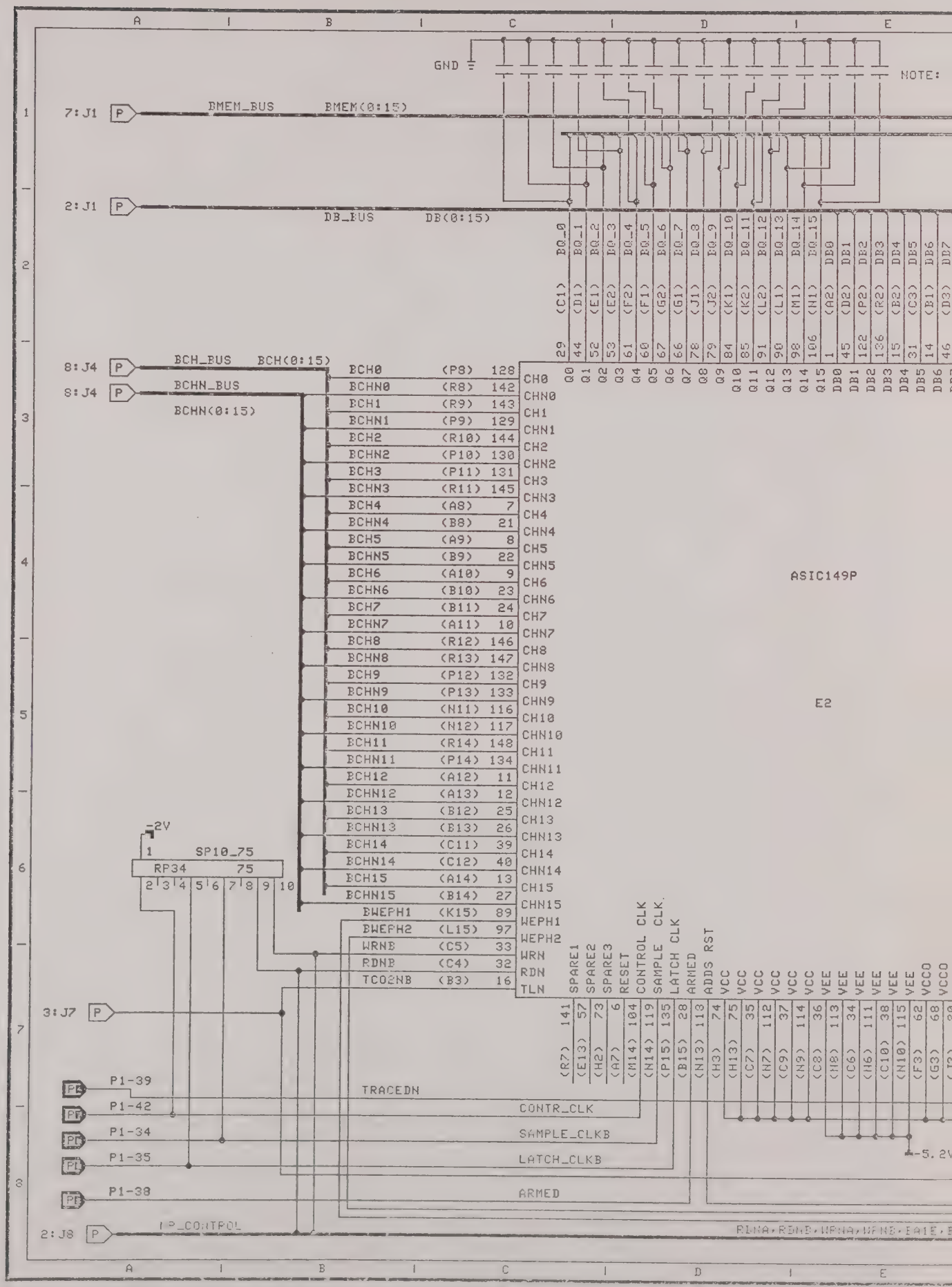

A1_(0:9)
A1_BUS
5:A8
B1_(0:9)
B1_BUS
7:A8
10H016
B1
B1_4
B1_5
B1_6
B1_7
10H103
XCMP14
A6
BCKPH1
B_ADRS_RST
BCKPH2
B1_8
B1_9
A1
C1
B1_0
B1_1
B1_2
B1_3
-2V
SP10_100
RP4
A2_(0:9)
A2_BUS
B2_(0:9)
B2_BUS
B4
B2_4
B2_5
B2_6
B2_7
B2_8
B2_9
A4
C4
B2_0
B2_1
B2_2
B2_3
TCO2NB
6:A7
RP6
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0416
REV 54
6-18-87
SHEET 3 OF 3
14 JUL 87 10:37 /USER/STEVE/DATA 3.DRAW

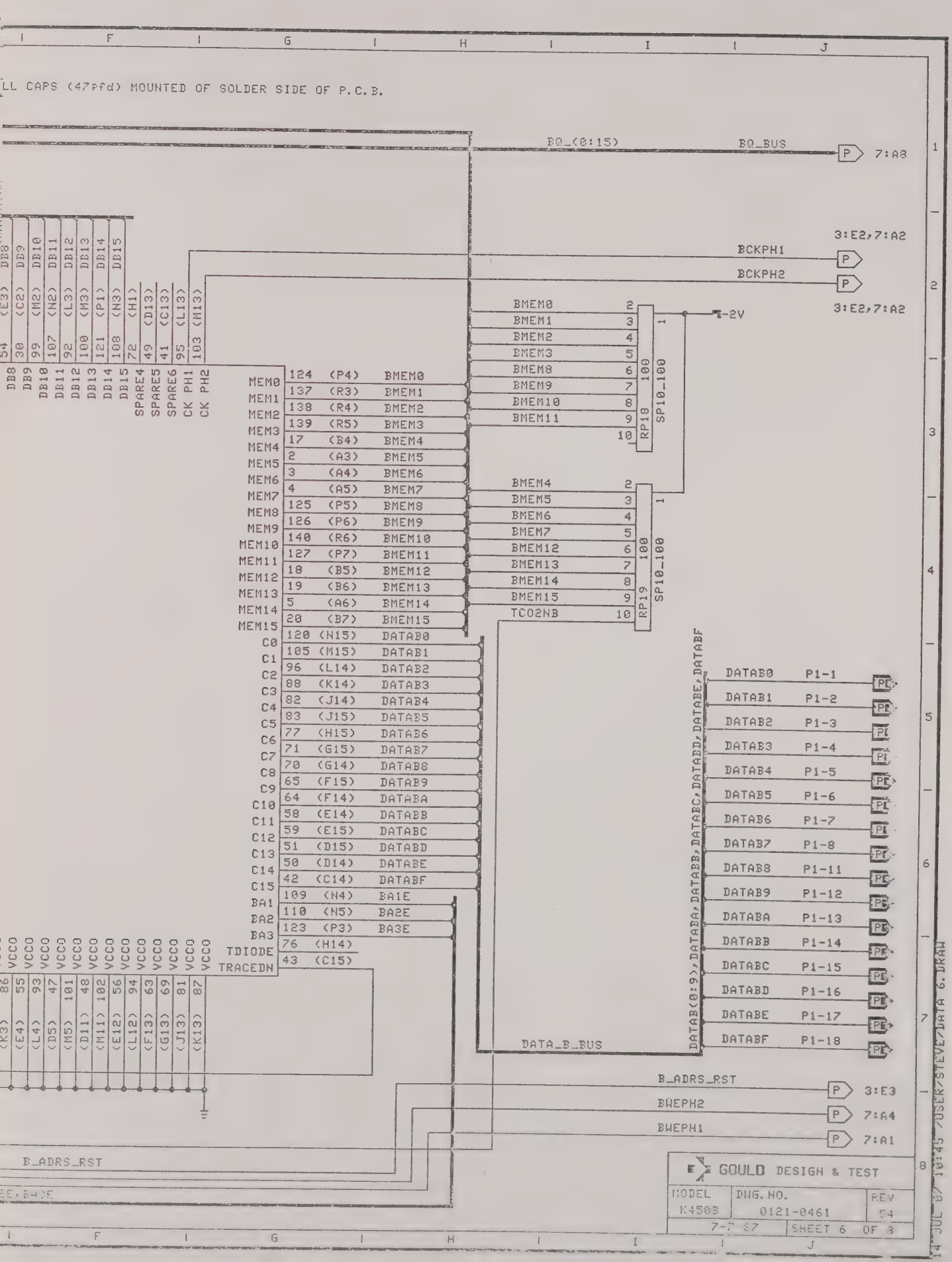

GND
NOTE:
5:J1
AMEM_BUS
AMEM(0:15)
2:J1
DB_BUS
DB(0:15)
ACH(0:15)
8:J5
ACH_BUS
8:J4
ACHN_BUS
ACHN(0:15)
-2V
SP10_100
RP10
RP11
SP10_75
RP41
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
DB8
DB9
DB10
DB11
DB12
DB13
DB14
DB15
ACH0 (P8) 128
ACHN0 (R8) 142
ACH1 (R9) 143
ACHN1 (P9) 129
ACH2 (R10) 144
ACHN2 (P10) 130
ACH3 (P11) 131
ACHN3 (R11) 145
ACH4 (A8) 7
ACHN4 (B8) 21
ACH5 (A9) 8
ACHN5 (B9) 22
ACH6 (A10) 9
ACHN6 (B10) 23
ACH7 (B11) 24
ACHN7 (A11) 10
ACH8 (R12) 146
ACHN8 (R13) 147
ACH9 (P12) 132
ACHN9 (P13) 133
ACH10 (N11) 116
ACHN10 (N12) 117
ACH11 (R14) 148
ACHN11 (P14) 134
ACH12 (A12) 11
ACHN12 (A13) 12
ACH13 (B12) 25
ACHN13 (B13) 26
ACH14 (C11) 39
ACHN14 (C12) 40
ACH15 (A14) 13
ACHN15 (B14) 27
AWEPH1 (K15) 89
AWEPH2 (L15) 97
WRNA (C5) 33
(C4) 32
RDNA (B3) 16
TCO2NA
CH0
CHN0
CH1
CHN1
CH2
CHN2
CH3
CHN3
CH4
CHN4
CH5
CHN5
CH6
CHN6
CH7
CHN7
CH8
CHN8
CH9
CHN9
CH10
CHN10
CH11
CHN11
CH12
CHN12
CH13
CHN13
CH14
CHN14
CH15
CHN15
WEPH1
WEPH2
WRN
RDN
TLN
3:E7
P1-39
P1-42
P1-43
P1-46
P1-38
TRACEDN
CONTR_CLK
SAMPLE_CLKA
LATCH_CLKA
ARMED
2:J8
MP_CONTROL
ASIC149P
E9
SPARE1
SPARE2
SPARE3
RESET
CONTROL CLK
SAMPLE CLK
LATCH CLK
ARMED
ADDS RST
VCC
VEE
VCCO
AQ_0
AQ_1
AQ_2
AQ_3
AQ_4
AQ_5
AQ_6
AQ_7
AQ_8
AQ_9
AQ_10
AQ_11
AQ_12
AQ_13
AQ_14
AQ_15
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
-5.2V
RDNA, RDNB, WRNA, WRNB, EA:5

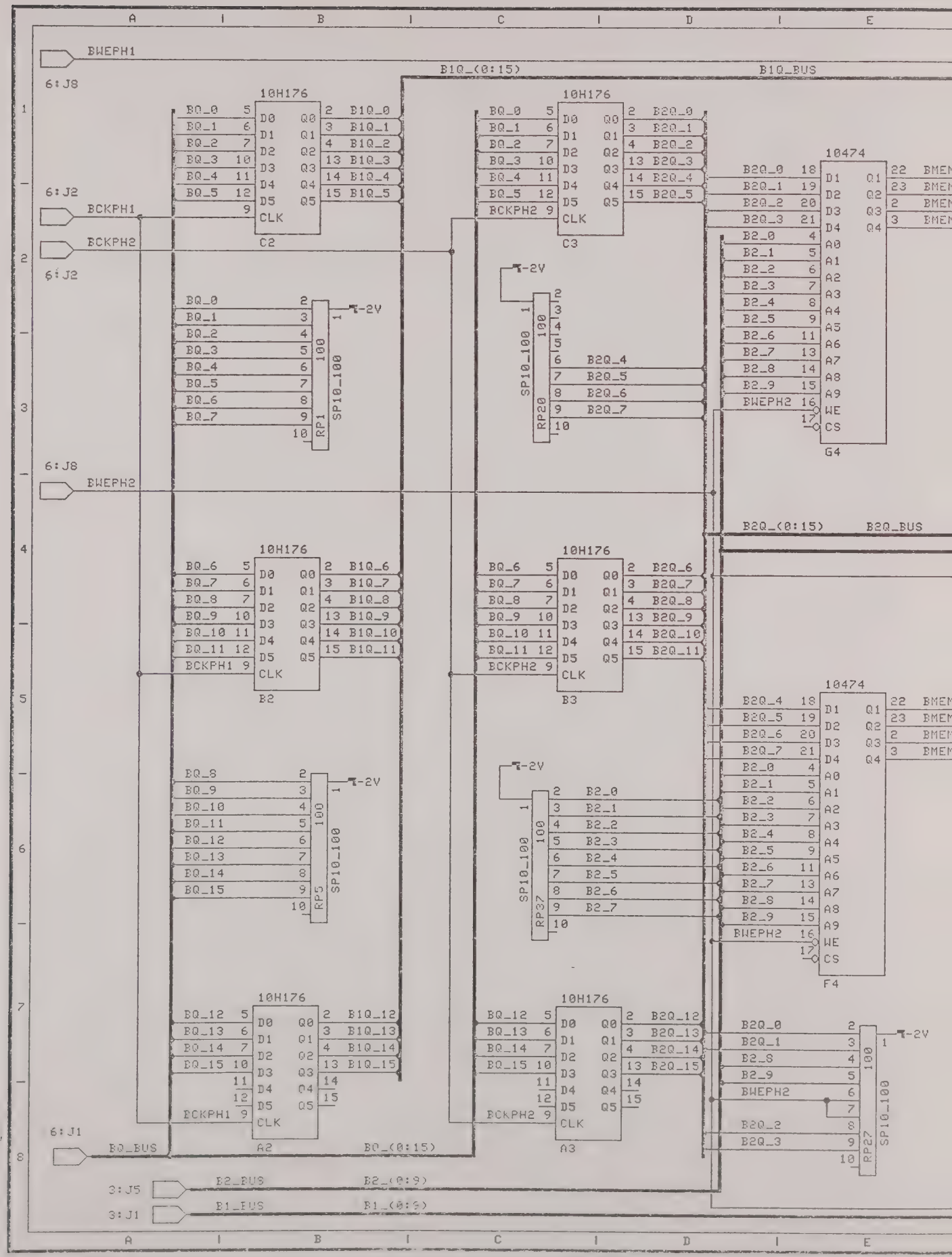

ALL CAPS (47pfd) MOUNTED ON SOLDER SIDE OF P.C.B.
AQ_(0:15)
AQ_BUS
5:A8
3:A2,5:A2
ACKPH1
ACKPH2
3:A3,5:A2
-2V
AMEM0
AMEM1
AMEM2
AMEM3
AMEM8
AMEM9
AMEM10
AMEM11
RP23 100 SP10_100
AMEM4
AMEM5
AMEM6
AMEM7
AMEM12
AMEM13
AMEM14
AMEM15
TCO2NA
RP24 100 SP10_100
DATAA0 P2-61
DATAA1 P2-62
DATAA2 P2-63
DATAA3 P2-64
DATAA4 P2-65
DATAA5 P2-66
DATAA6 P2-67
DATAA7 P2-68
DATAA8 P2-71
DATAA9 P2-72
DATAAA P2-73
DATAAB P2-74
DATAAC P2-75
DATAAD P2-76
DATAAE P2-77
DATAAF P2-78
DATAA(0:9),DATAAA,DATAAB,DATAAC,DATAAD,DATAAE,DATAAF
DATA_A_BUS
A_ADRS_RST
3:A3
AWEPH2
5:A4
AWEPH1
5:A1
MEM0 MEM1 MEM2 MEM3 MEM4 MEM5 MEM6 MEM7 MEM8 MEM9 MEM10 MEM11 MEM12 MEM13 MEM14 MEM15
C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15
BA1 BA2 BA3
TDIODE
TRACEDN
SPARE4 SPARE5 SPARE6 CK PH1 CK PH2
VCCO
A_ADRS_RST
BA2E,BA3E
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0416
REV 54
7-7-87
SHEET 4 OF 8
14 JUL 87 10:40 /USER/STEVE/DATA 4.DRAW

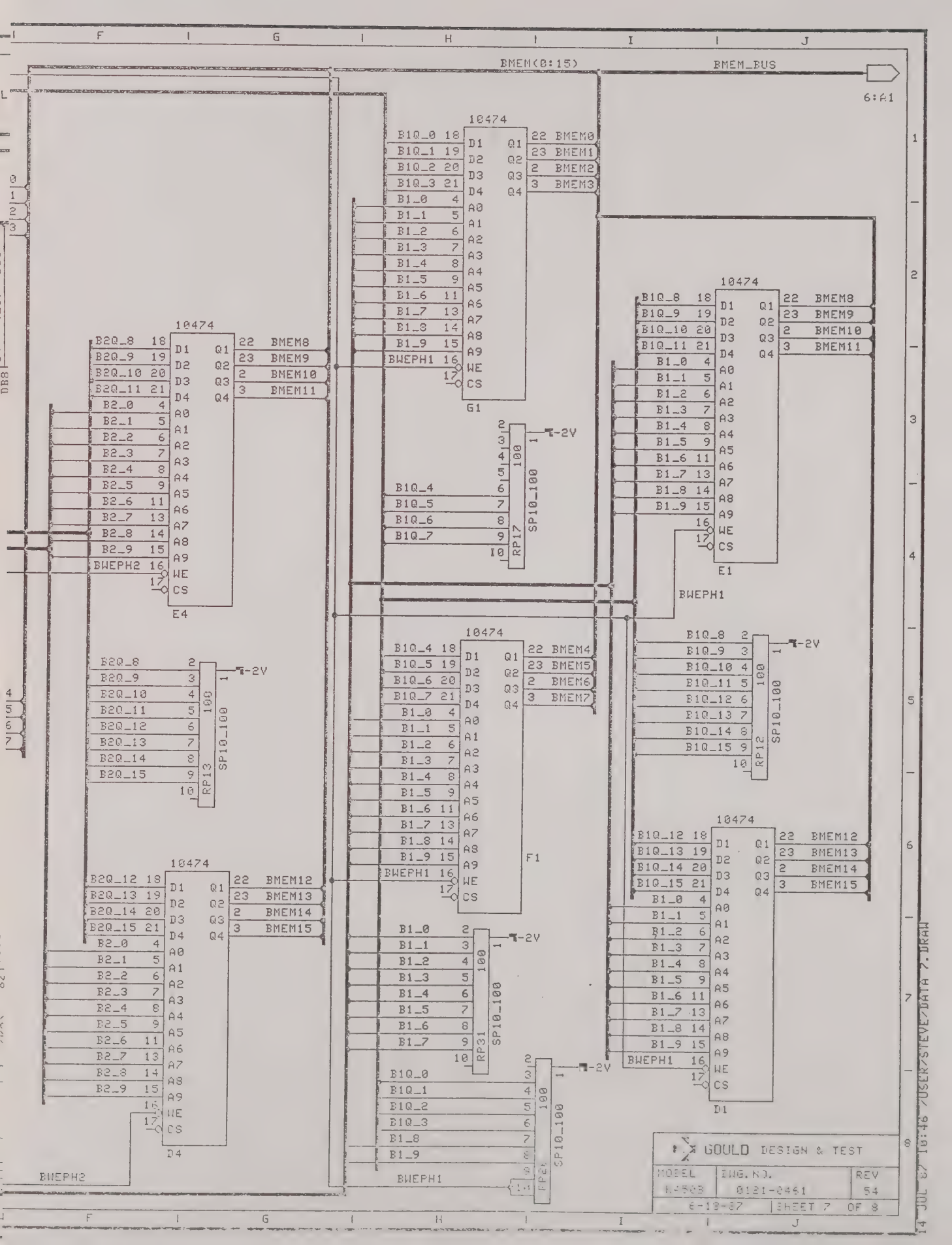

A B C D E
AWEPH1
A1Q_BUS A1Q_(0:15)
4:J8
10H176
AQ_0 AQ_1 AQ_2 AQ_3 AQ_4 AQ_5
D0 D1 D2 D3 D4 D5 CLK
Q0 Q1 Q2 Q3 Q4 Q5
A1Q_0 A1Q_1 A1Q_2 A1Q_3 A1Q_4 A1Q_5
C9
4:J2
ACKPH1
ACKPH2
4:J2
10H176
A2Q_0 A2Q_1 A2Q_2 A2Q_3 A2Q_4 A2Q_5
C10
10474
A2Q_0 A2Q_1 A2Q_2 A2Q_3
A2_0 A2_1 A2_2 A2_3 A2_4 A2_5 A2_6 A2_7 A2_8 A2_9
AWEPH2
WE CS
AMEM
G11
-2V
SP10_100
RP3
RP25
4:J7
AWEPH2
A2Q_BUS A2Q_(0:15)
A2_BUS
10H176
A1Q_6 A1Q_7 A1Q_8 A1Q_9 A1Q_10 A1Q_11
B9
A2Q_6 A2Q_7 A2Q_8 A2Q_9 A2Q_10 A2Q_11
B10
10474
A2Q_4 A2Q_5 A2Q_6 A2Q_7
F11
RP8
RP44
10H176
A1Q_12 A1Q_13 A1Q_14 A1Q_15
A9
A2Q_12 A2Q_13 A2Q_14 A2Q_15
A10
RP30
4:J1
A0_BUS
A0_(0:15)
3:J5
A2_BUS
A2_(0:9)
3:J1
A1_BUS
A1_(0:9)

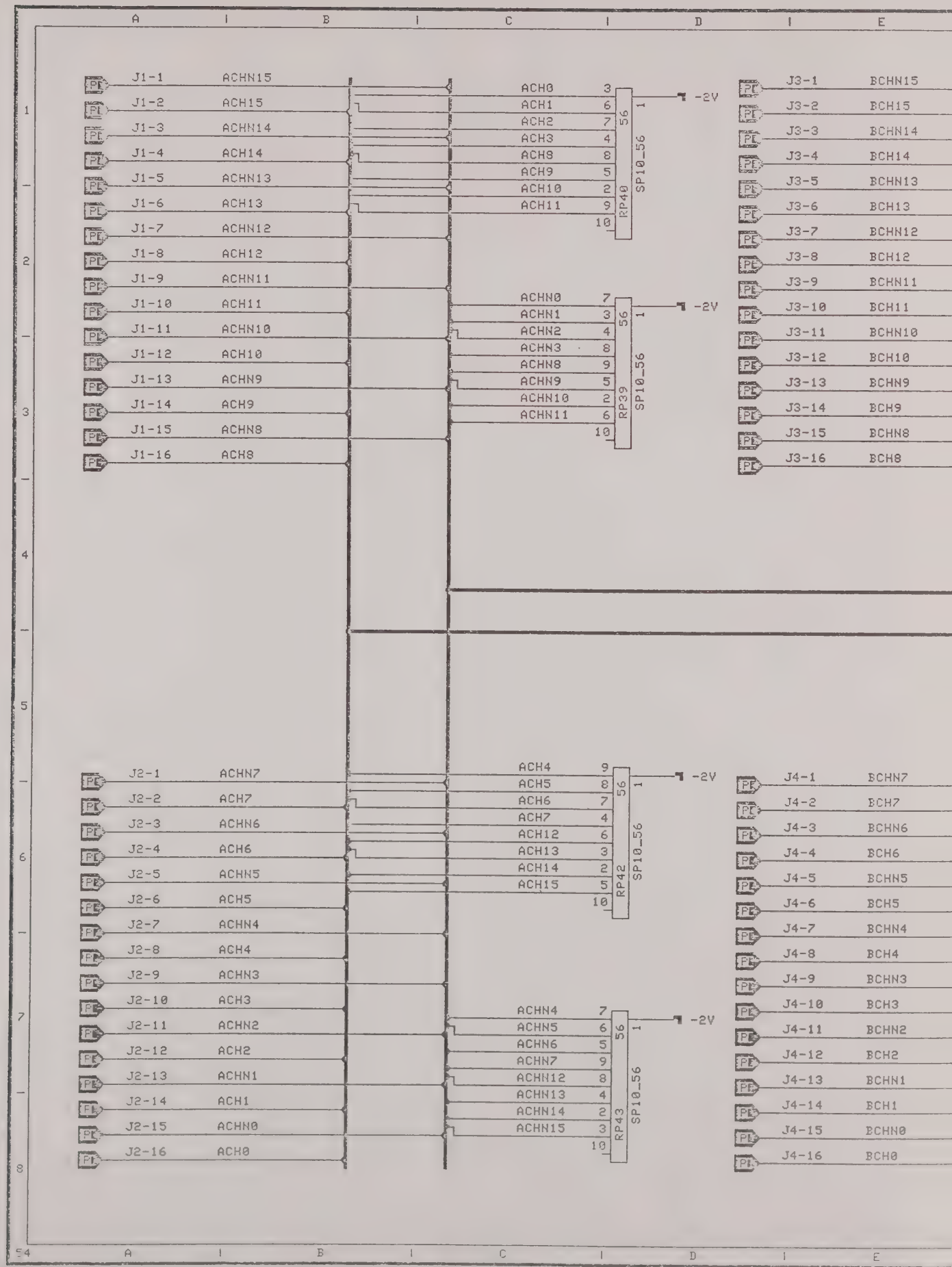

AMEM(0:15)
AMEM_BUS
4:A1
2:J8
MP_CONTROL
10474
G8
E8
E11
F8
D8
D11
A1_BUS
A1Q_BUS
AWEPH1
AWEPH2
RP22 SP10_100
RP15 SP10_100
RP16 SP10_100
RP38 SP10_100
RP29 SP10_100
-2V
GOULD DESIGN & TEST
MODEL 4503
DWG. NO. 0121-0416
REV 54
6-13-87
SHEET 5 OF 8
14 JUL 87 10:43 /USER/STEVE/DATA 5.DRAW

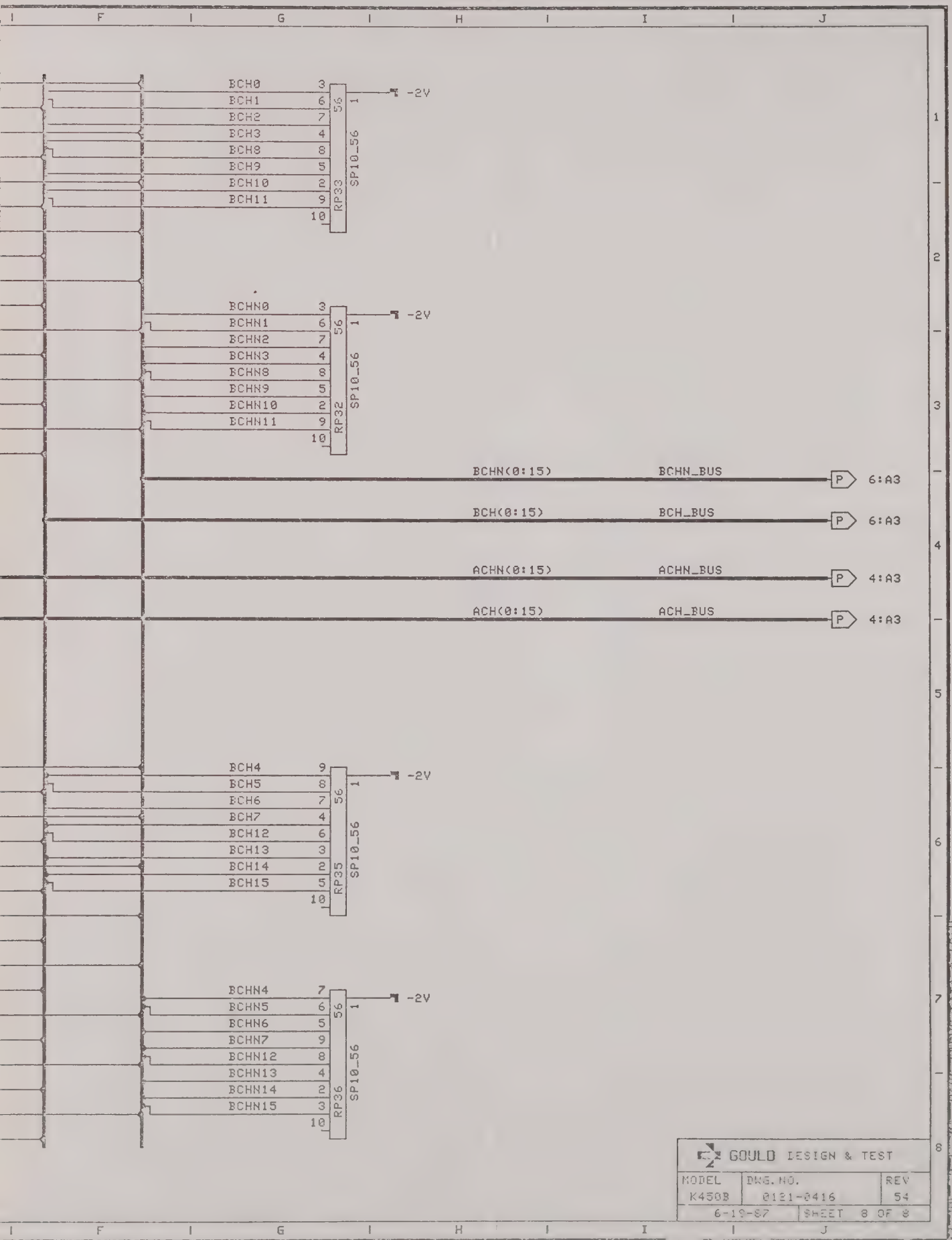

GND
NOTE:
7:J1
BMEM_BUS
BMEM(0:15)
2:J1
DB_BUS
DB(0:15)
8:J4
BCH_BUS
BCH(0:15)
8:J4
BCHN_BUS
BCHN(0:15)
ASIC149P
E2
-2V
SP10_75
RP34
75
3:J7
P1-39
P1-42
P1-34
P1-35
P1-38
2:J8
TRACEDN
CONTR_CLK
SAMPLE_CLKB
LATCH_CLKB
ARMED
-5.2V

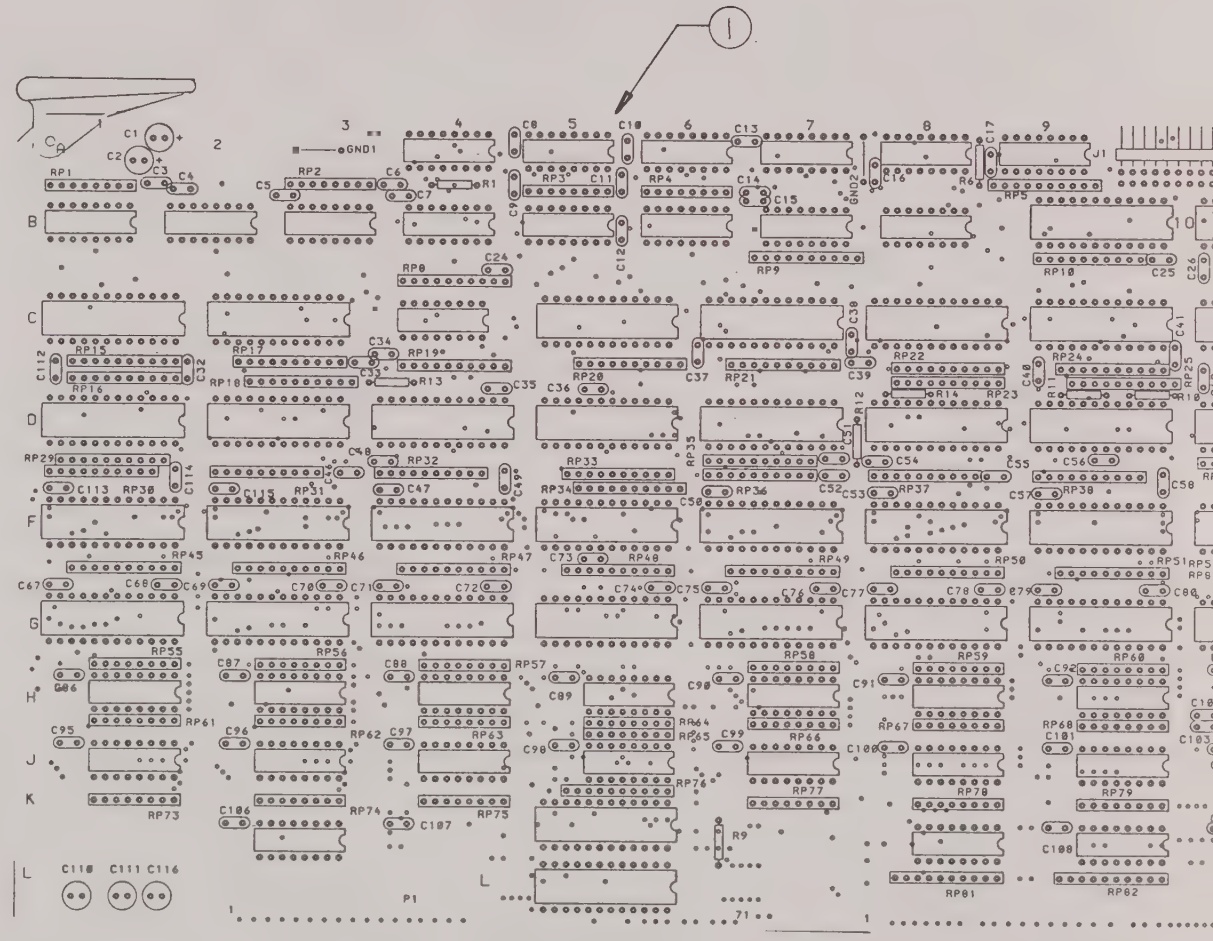

LL CAPS (47pfd) MOUNTED OF SOLDER SIDE OF P.C.B.
BQ_(0:15)
BQ_BUS
P 7:A8
3:E2,7:A2
BCKPH1
BCKPH2
3:E2,7:A2
BMEM0
BMEM1
BMEM2
BMEM3
BMEM8
BMEM9
BMEM10
BMEM11
RP18 100 SP10_100
-2V
BMEM4
BMEM5
BMEM6
BMEM7
BMEM12
BMEM13
BMEM14
BMEM15
TCO2NB
RP19 100 SP10_100
DB8 (E3)
DB9 (C2)
DB10 (M2)
DB11 (N2)
DB12 (L3)
DB13 (M3)
DB14 (P1)
DB15 (N3)
SPARE4 (H1)
SPARE5 (D13)
SPARE6 (C13)
CK PH1 (L13)
CK PH2 (M13)
MEM0 124 (P4) BMEM0
MEM1 137 (R3) BMEM1
MEM2 138 (R4) BMEM2
MEM3 139 (R5) BMEM3
MEM4 17 (B4) BMEM4
MEM5 2 (A3) BMEM5
MEM6 3 (A4) BMEM6
MEM7 4 (A5) BMEM7
MEM8 125 (P5) BMEM8
MEM9 126 (P6) BMEM9
MEM10 140 (R6) BMEM10
MEM11 127 (P7) BMEM11
MEM12 18 (B5) BMEM12
MEM13 19 (B6) BMEM13
MEM14 5 (A6) BMEM14
MEM15 20 (B7) BMEM15
C0 120 (N15) DATAB0
C1 105 (M15) DATAB1
C2 96 (L14) DATAB2
C3 88 (K14) DATAB3
C4 82 (J14) DATAB4
C5 83 (J15) DATAB5
C6 77 (H15) DATAB6
C7 71 (G15) DATAB7
C8 70 (G14) DATAB8
C9 65 (F15) DATAB9
C10 64 (F14) DATABA
C11 58 (E14) DATABB
C12 59 (E15) DATABC
C13 51 (D15) DATABD
C14 50 (D14) DATABE
C15 42 (C14) DATABF
BA1 109 (N4) BA1E
BA2 110 (N5) BA2E
BA3 123 (P3) BA3E
TDIODE 76 (H14)
TRACEDN 43 (C15)
DATAB0 P1-1
DATAB1 P1-2
DATAB2 P1-3
DATAB3 P1-4
DATAB4 P1-5
DATAB5 P1-6
DATAB6 P1-7
DATAB7 P1-8
DATAB8 P1-11
DATAB9 P1-12
DATABA P1-13
DATABB P1-14
DATABC P1-15
DATABD P1-16
DATABE P1-17
DATABF P1-18
DATAB(0:9),DATABA,DATABB,DATABC,DATABD,DATABE,DATABF
DATA_B_BUS
B_ADRS_RST
P 3:E3
BWEPH2
P 7:A4
BWEPH1
P 7:A1
VCCO 86 (K3)
VCCO 55 (E4)
VCCO 93 (L4)
VCCO 47 (D5)
VCCO 101 (M5)
VCCO 48 (D11)
VCCO 102 (M11)
VCCO 56 (E12)
VCCO 94 (L12)
VCCO 63 (F13)
VCCO 69 (G13)
VCCO 81 (J13)
VCCO 87 (K13)
B_ADRS_RST
GOULD DESIGN & TEST
MODEL K4503
DWG. NO. 0121-0461
REV 54
7-7-87
SHEET 6 OF 8
14 JUL 87 10:45 /USER/STEVE/DATA 6.DRAW


BWEPH1
B1Q_(0:15)
B1Q_BUS
6:J8
10H176
BQ_0 5
BQ_1 6
BQ_2 7
BQ_3 10
BQ_4 11
BQ_5 12
9
CLK
D0 D1 D2 D3 D4 D5
Q0 Q1 Q2 Q3 Q4 Q5
2 3 4 13 14 15
B1Q_0 B1Q_1 B1Q_2 B1Q_3 B1Q_4 B1Q_5
C2
6:J2
BCKPH1
BCKPH2
6:J2
B2Q_0 B2Q_1 B2Q_2 B2Q_3 B2Q_4 B2Q_5
BCKPH2 9
C3
10474
B2Q_0 18
B2Q_1 19
B2Q_2 20
B2Q_3 21
B2_0 4
B2_1 5
B2_2 6
B2_3 7
B2_4 8
B2_5 9
B2_6 11
B2_7 13
B2_8 14
B2_9 15
BWEPH2 16
17
D1 D2 D3 D4
Q1 Q2 Q3 Q4
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
WE
CS
22 23 2 3
BMEM
G4
-2V
SP10_100
100
RP1
RP20
BQ_0 2
BQ_1 3
BQ_2 4
BQ_3 5
BQ_4 6
BQ_5 7
BQ_6 8
BQ_7 9
10
1
B2Q_4 B2Q_5 B2Q_6 B2Q_7
6:J8
BWEPH2
B2Q_(0:15)
B2Q_BUS
BQ_6 BQ_7 BQ_8 BQ_9 BQ_10 BQ_11
B1Q_6 B1Q_7 B1Q_8 B1Q_9 B1Q_10 B1Q_11
B2
B2Q_6 B2Q_7 B2Q_8 B2Q_9 B2Q_10 B2Q_11
B3
B2Q_4 B2Q_5 B2Q_6 B2Q_7
F4
BQ_8 BQ_9 BQ_10 BQ_11 BQ_12 BQ_13 BQ_14 BQ_15
RP5
RP37
B2_0 B2_1 B2_2 B2_3 B2_4 B2_5 B2_6 B2_7
BQ_12 BQ_13 BQ_14 BQ_15
B1Q_12 B1Q_13 B1Q_14 B1Q_15
A2
B2Q_12 B2Q_13 B2Q_14 B2Q_15
A3
B2Q_0 B2Q_1 B2_8 B2_9 BWEPH2 B2Q_2 B2Q_3
RP27
6:J1
BQ_BUS
BQ_(0:15)
3:J5
B2_BUS
B2_(0:9)
3:J1
B1_BUS
B1_(0:9)


BMEM(0:15)
BMEM_BUS
6:A1
10474
G1
E1
E4
F1
D1
D4
RP17
RP12
RP13
RP31
SP10_100
-2V
BWEPH1
BWEPH2
GOULD DESIGN & TEST
MODEL
DWG. NO.
0121-0461
REV
54
6-19-87
SHEET 7 OF 8
14 JUL 87 10:46 /USER/STEVE/DATA 7.DRAW


A
B
C
D
E
J1-1 ACHN15
J1-2 ACH15
J1-3 ACHN14
J1-4 ACH14
J1-5 ACHN13
J1-6 ACH13
J1-7 ACHN12
J1-8 ACH12
J1-9 ACHN11
J1-10 ACH11
J1-11 ACHN10
J1-12 ACH10
J1-13 ACHN9
J1-14 ACH9
J1-15 ACHN8
J1-16 ACH8
ACH0 3
ACH1 6
ACH2 7
ACH3 4
ACH8 8
ACH9 5
ACH10 2
ACH11 9
10
RP40
56
1
SP10_56
-2V
ACHN0 7
ACHN1 3
ACHN2 4
ACHN3 8
ACHN8 9
ACHN9 5
ACHN10 2
ACHN11 6
10
RP39
56
1
SP10_56
-2V
J3-1 BCHN15
J3-2 BCH15
J3-3 BCHN14
J3-4 BCH14
J3-5 BCHN13
J3-6 BCH13
J3-7 BCHN12
J3-8 BCH12
J3-9 BCHN11
J3-10 BCH11
J3-11 BCHN10
J3-12 BCH10
J3-13 BCHN9
J3-14 BCH9
J3-15 BCHN8
J3-16 BCH8
J2-1 ACHN7
J2-2 ACH7
J2-3 ACHN6
J2-4 ACH6
J2-5 ACHN5
J2-6 ACH5
J2-7 ACHN4
J2-8 ACH4
J2-9 ACHN3
J2-10 ACH3
J2-11 ACHN2
J2-12 ACH2
J2-13 ACHN1
J2-14 ACH1
J2-15 ACHN0
J2-16 ACH0
ACH4 9
ACH5 8
ACH6 7
ACH7 4
ACH12 6
ACH13 3
ACH14 2
ACH15 5
10
RP42
56
1
SP10_56
-2V
ACHN4 7
ACHN5 6
ACHN6 5
ACHN7 9
ACHN12 8
ACHN13 4
ACHN14 2
ACHN15 3
10
RP43
56
1
SP10_56
-2V
J4-1 BCHN7
J4-2 BCH7
J4-3 BCHN6
J4-4 BCH6
J4-5 BCHN5
J4-6 BCH5
J4-7 BCHN4
J4-8 BCH4
J4-9 BCHN3
J4-10 BCH3
J4-11 BCHN2
J4-12 BCH2
J4-13 BCHN1
J4-14 BCH1
J4-15 BCHN0
J4-16 BCH0
1
2
3
4
5
6
7
8


BCH0
BCH1
BCH2
BCH3
BCH8
BCH9
BCH10
BCH11
RP33
SP10_56
-2V
BCHN0
BCHN1
BCHN2
BCHN3
BCHN8
BCHN9
BCHN10
BCHN11
RP32
SP10_56
-2V
BCHN(0:15)
BCHN_BUS
6:A3
BCH(0:15)
BCH_BUS
6:A3
ACHN(0:15)
ACHN_BUS
4:A3
ACH(0:15)
ACH_BUS
4:A3
BCH4
BCH5
BCH6
BCH7
BCH12
BCH13
BCH14
BCH15
RP35
SP10_56
-2V
BCHN4
BCHN5
BCHN6
BCHN7
BCHN12
BCHN13
BCHN14
BCHN15
RP36
SP10_56
-2V
GOULD DESIGN & TEST
MODEL K4508
DWG. NO. 0121-0416
REV 54
6-19-87
SHEET 8 OF 8



4 (X) INDICATES SOCKET LOCATIONS – REF ONLY.

3. MANUFACTURE PER GOULD WORKMANSHIP STD. 87000012.

2. ASSY. REFLECTS SCHEM DWG 0121-0421 & FAB DWG 0121-0422.

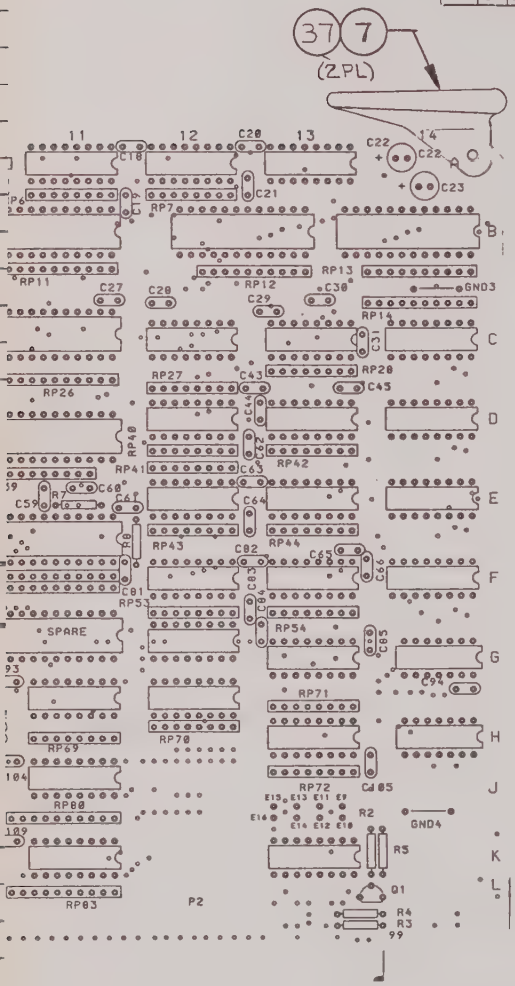
1 MARK ASSY. DASH NO. REV & SERIAL NO. APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK.

NOTES: UNLESS OTHERWISE SPECIFIED.

DWG. NO. 0121-0420	SH 1	REV 54

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	50	5668	PILOT RELEASE PER ECO #	DLW	JLW	5/4/87
	51	5698	BOM CHANGES ONLY 6/2/87	MM	DLW	6/25/87
	52	5728	REV ROLL ONLY 6/29/87	MM	BTM	6/29/87
	53	5741	REV ROLL ONLY 7/9/87	MM	BTM	7/29
	54	5774	REV ROLL ONLY 8/5/87	MM	[illegible]	8/7/87



-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN DLW	3/25/87
CHECKED	
PROJ ENG.	

GOULD Electronics

TITLE: ASSY CONTROL BD.

SIZE	DWG. NO.	REV.
C	0121-0420	54

SCALE N/A | MODEL K450 B | SHEET 1 OF 1

NEXT ASSY	USED ON
K4503-XXX	K450 B
FIRST APPLICATION	

BILL OF MATERIAL

AS OF 10/30/87

0121-0420-10 ASSY,PCB,CONTROL,K450B
MODEL: K450B

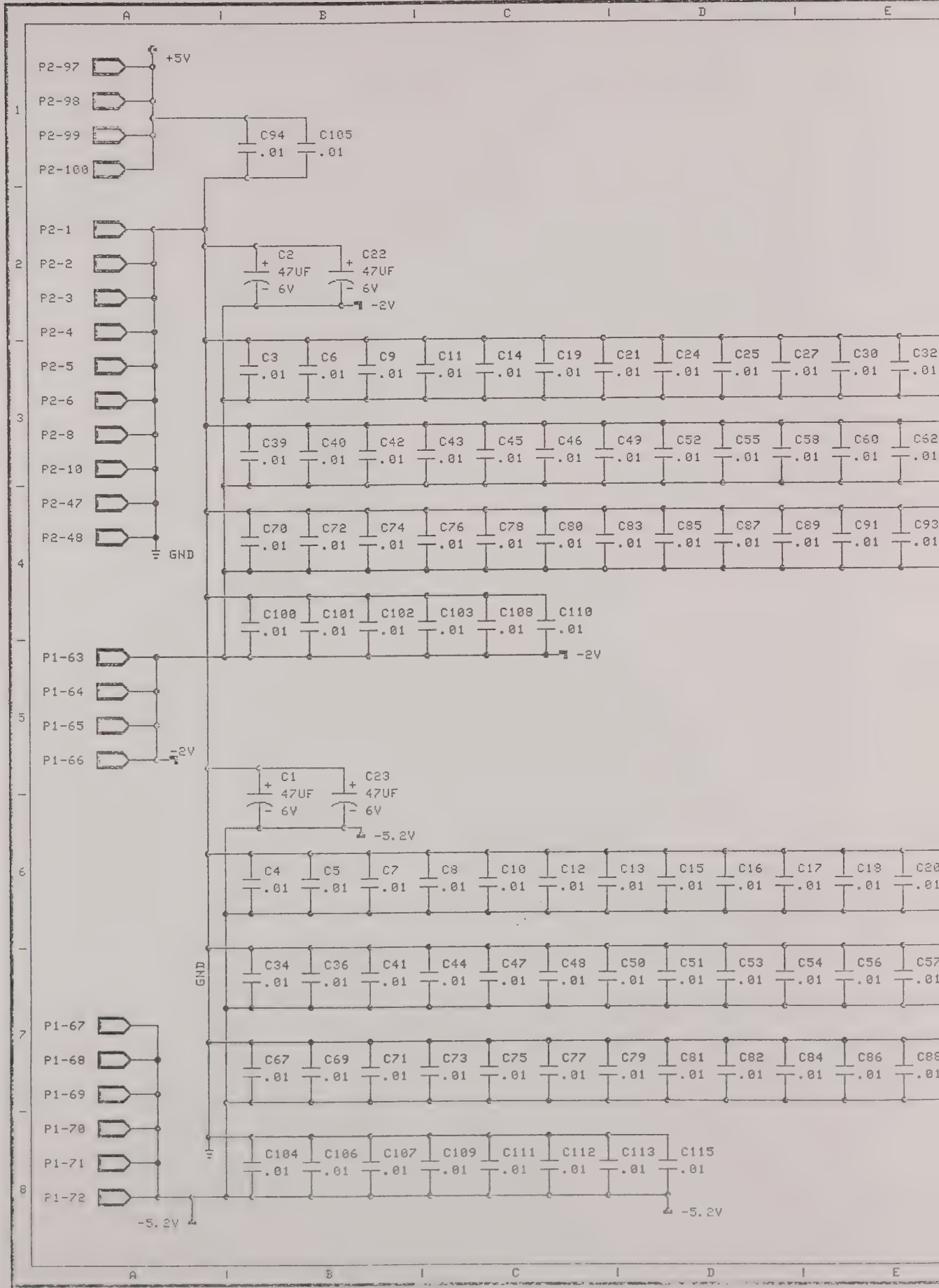
ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0421	SCHEM,PCB,CONTROL,K450B	0	EA	REF
0	D0121-0420	DWG,ASSY,PCB,CONTROL,K450B	0	EA	
1	0121-0422-10	FAB,PCB,CONTROL,K450B	1	EA	
2	1850-0147-20	IC HM10474-10,RAM,1KX4 ACC.T	12	EA	1F,3F,4F, 1G,3G,4G, 7F,8F,9F, 7G,8G,9G,
3	1800-0105-10	IC 74LS00N 2-IN NAND LOW	1	EA	14G
4	1800-0254-10	IC 74LS85N 4-BIT MAG	1	EA	13H
5	1800-0349-10	IC 74368AN HEX BUS DR	1	EA	12H
6	6000-0307-10	CONN 20 PIN HDR. RT. ANGL	1	EA	J1
7	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
8	1850-0103-10	IC MC10125L QUAD ECL-TT	2	EA	13K,12G
9	1850-0097-10	IC MC10231L DUAL D F/F	1	EA	5A
10	1850-0104-10	IC MC10124L QUAD TTL	5	EA	11H,11J 8K,9K,11K,
11	1850-0099-10	IC MC10164L 8-INPUT MULT	5	EA	12D,12E 4C,12C,12F
12	1850-0106-10	IC MC10117L DUAL 2 WIDE	1	EA	4A
13	1850-0111-10	IC MC10103L QUAD 2-IN	1	EA	11A
14	1850-0131-10	IC MC10H016L B/N COUNTER	4	EA	13C-13F
15	1850-0098-10	IC MC10176L HEX D F/F	16	EA	1H,3H,4H, 1J,3J,4J, 3K 6A,7A,12A, 7H,8H,9H, 7J,8J,9J,
16	1850-0077-10	IC F100101DC TPL 5OR/NOR	9	EA	3D,4D,8D 5F,7D,9D, 9B,1D,11D,
17	1850-0078-10	IC F100102DC 2IN OR/NOR	11	EA	11C,11B,5L 11F,5D 1C,3C,5C, 7C,8C,9C,
18	1850-0079-10	IC F100112DC QUAD DRIVER	1	EA	5K
20	1850-0089-10	IC F10145ADC 16 X 4 RAM	10	EA	1B-8B,8A, 9A
21	1850-0089-20	IC HD10145 HITACHI/FAIRCHILD	7	EA	14C-14F 5H,5J,13A,
22	1850-0091-10	IC F100155DC QUAD MUX	3	EA	5G,12B,14B
23	1850-0100-10	IC MC10161L 1 OF 8 DEC	1	EA	13G
24	4010-0103-10	CAP,0.01UF,50V,10%,CER	109	EA	93,C95-104 C106-109, C112-115 C3-21,C24- C94,105

BILL OF MATERIAL

AS OF 10/30/87

0121-0420-10 ASSY,PCB,CONTROL,K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
25	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	7	EA	C1,C2,C22, C111,C116 C23,C110,
26	1400-0019-10	TRAN 2N3906	1	EA	Q1
27	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	1	EA	RP71
28	3700-0088-10	RPAK,3K/6.2K,0.17W,2%,8/12	2	EA	RP70,72
29	3700-0091-10	RPAK,68,0.2W,2%,8/7	37	EA	27,28,40-44,54-69, 73,74,75, 77,78,79 RP1-4,6,7 RP53
30	3700-0092-10	RPAK,68,0.2W,2%,10/9	41	EA	29-39,45-52,76,84 RP5,8-26,
31	3000-2001-10	RES,2K,5%,1/4W,C	1	EA	R1
32	3000-2006-10	RES,20,5%,1/4W,C	1	EA	R2
33	3000-1800-10	RES,180,5%,1/4W,C	1	EA	R3
34	3000-3300-10	RES,330,5%,1/4W,C	1	EA	R4
35	3000-5106-10	RES,51,5%,1/4W,C	1	EA	R5
36	6100-0137-10	SKT 24 PIN DIP LOW PRO	12	EA	X1F,X3F, X1G,X3G, X4F,X7F, X4G,X7G, X8F,X9F, X8G,X9G
37	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
38	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	17	EA	X13A,X14E-X14F X1B-X8B, X5H,X5J, X8A,X9A,
41	6100-0119-10	SKT 14 PIN DIP LO-PROFIL	1	EA	X14H
42	3000-1002-10	RES,10K,5%,1/4W,C	1	EA	R14
43	1800-0280-10	IC 74S37N BUFFER/CLK DR.	1	EA	14H
45	3000-6806-10	RES,68,5%,1/4W,C	6	EA	R6,R9-13
46	3000-6800-10	RES,680,5%,1/4W,C	2	EA	R7,R8
48	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	4	EA	RP80-83


A
B
C
D
E
1
2
3
4
5
6
7
8
P2-97
P2-98
P2-99
P2-100
+5V
C94 .01
C105 .01
P2-1
P2-2
P2-3
P2-4
P2-5
P2-6
P2-8
P2-10
P2-47
P2-48
GND
C2 47UF 6V
C22 47UF 6V
-2V
C3 .01
C6 .01
C9 .01
C11 .01
C14 .01
C19 .01
C21 .01
C24 .01
C25 .01
C27 .01
C30 .01
C32 .01
C39 .01
C40 .01
C42 .01
C43 .01
C45 .01
C46 .01
C49 .01
C52 .01
C55 .01
C58 .01
C60 .01
C62 .01
C70 .01
C72 .01
C74 .01
C76 .01
C78 .01
C80 .01
C83 .01
C85 .01
C87 .01
C89 .01
C91 .01
C93 .01
C100 .01
C101 .01
C102 .01
C103 .01
C108 .01
C110 .01
-2V
P1-63
P1-64
P1-65
P1-66
-2V
C1 47UF 6V
C23 47UF 6V
-5.2V
C4 .01
C5 .01
C7 .01
C8 .01
C10 .01
C12 .01
C13 .01
C15 .01
C16 .01
C17 .01
C18 .01
C20 .01
GND
C34 .01
C36 .01
C41 .01
C44 .01
C47 .01
C48 .01
C50 .01
C51 .01
C53 .01
C54 .01
C56 .01
C57 .01
P1-67
P1-68
P1-69
P1-70
P1-71
P1-72
C67 .01
C69 .01
C71 .01
C73 .01
C75 .01
C77 .01
C79 .01
C81 .01
C82 .01
C84 .01
C86 .01
C88 .01
C104 .01
C106 .01
C107 .01
C109 .01
C111 .01
C112 .01
C113 .01
C115 .01
-5.2V
-5.2V

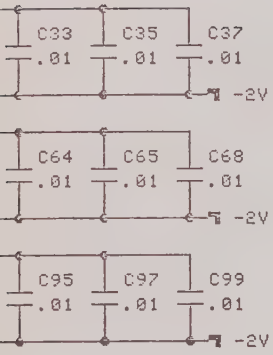
P1-33-48,60 — N.C.

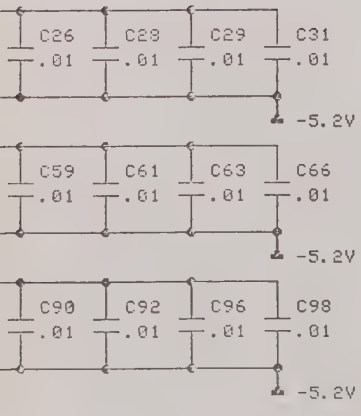
P2-11,13-15, 34,35,87-94 — N.C.

REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE
	51	5698	RELEASED PER ECO	M.S.			6/10 1987
	52	5728	REV. ROLL ONLY				
8:E4 9:B8	53	5741	ADD 8 INCHES TO DELAY_PE~	S.M.			7/13 1987
	54	5774	REV. ROLL ONLY	R.H.			

NOTES:

1. All RPs are 68 Ohms, unless otherwise specified.
2. May use HD10145 ICs in place of 10145A ICs: ONLY in locations: 5H,5J,13A,14C-14F.
3. R6 is used as a TEST POINT at top of the board, sheet 7.





DASH NO.	NUMBER	QTY	ECO NO.
	NEXT ASSEMBLY		

	DRAWN	DATE
	PROJ. ENGR	
	MANUFACTURING	
	QUALITY ASSUR	

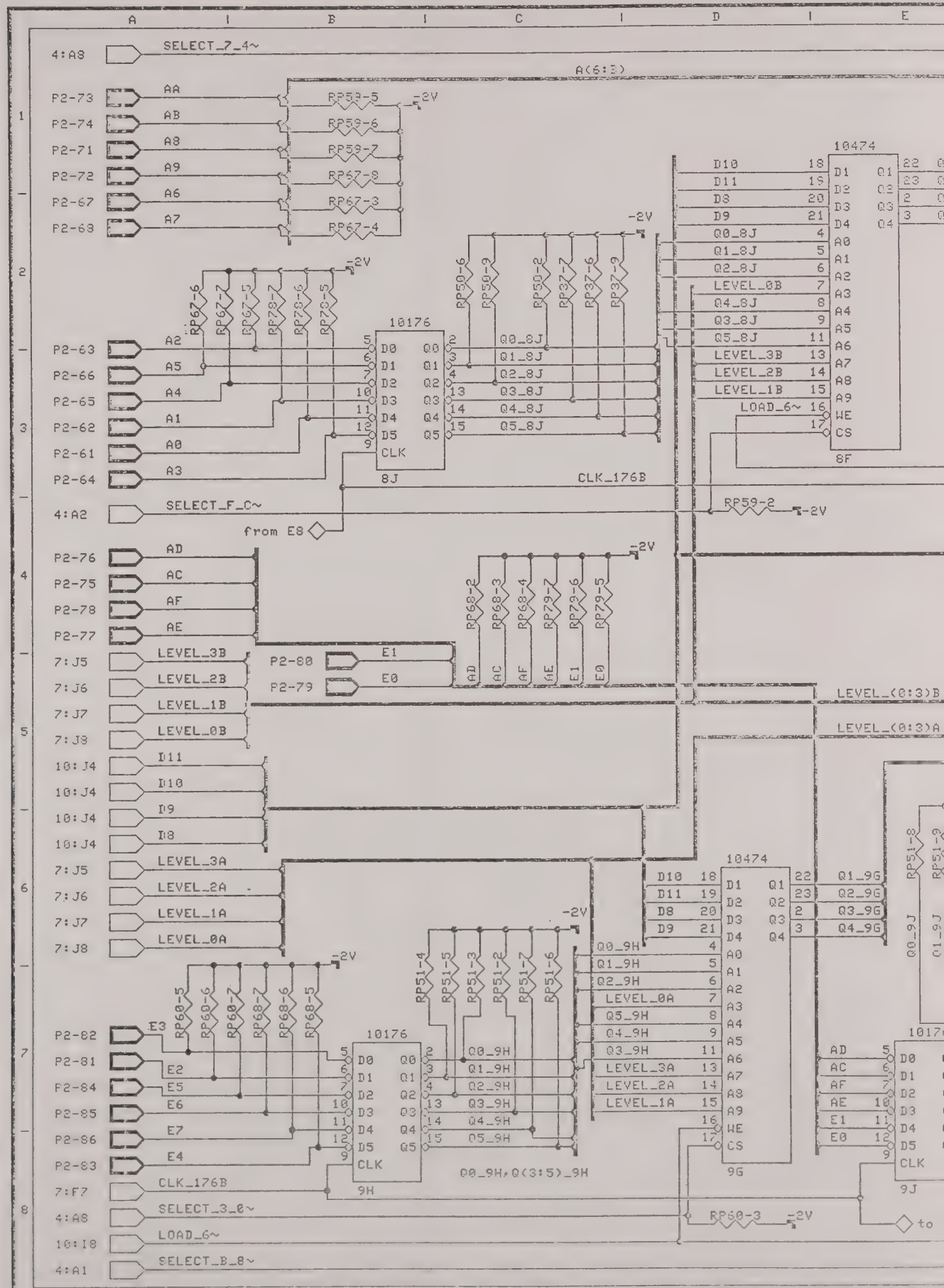
GOULD DESIGN & TEST

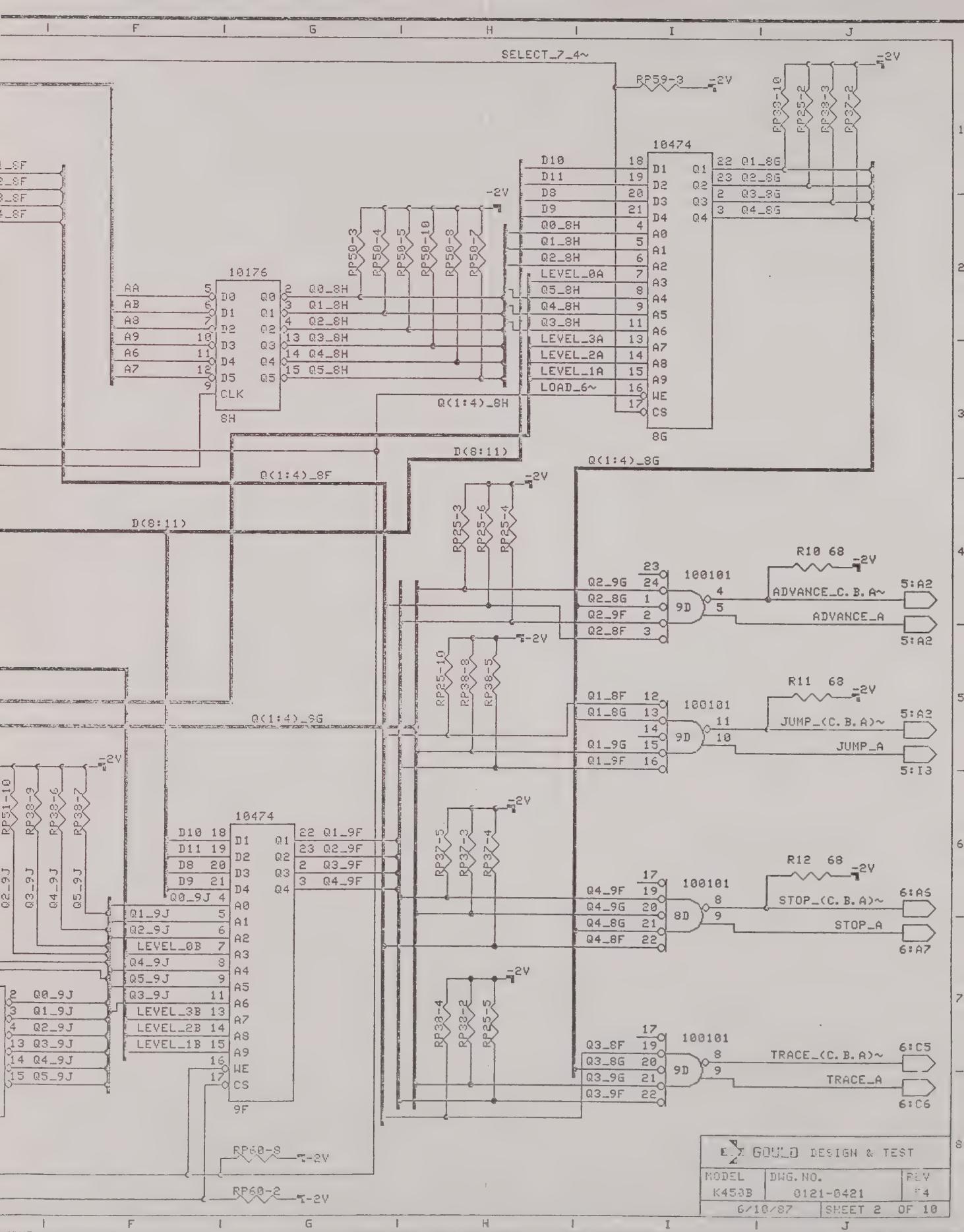
TITLE
SCHEMATIC
CONTROL BOARD

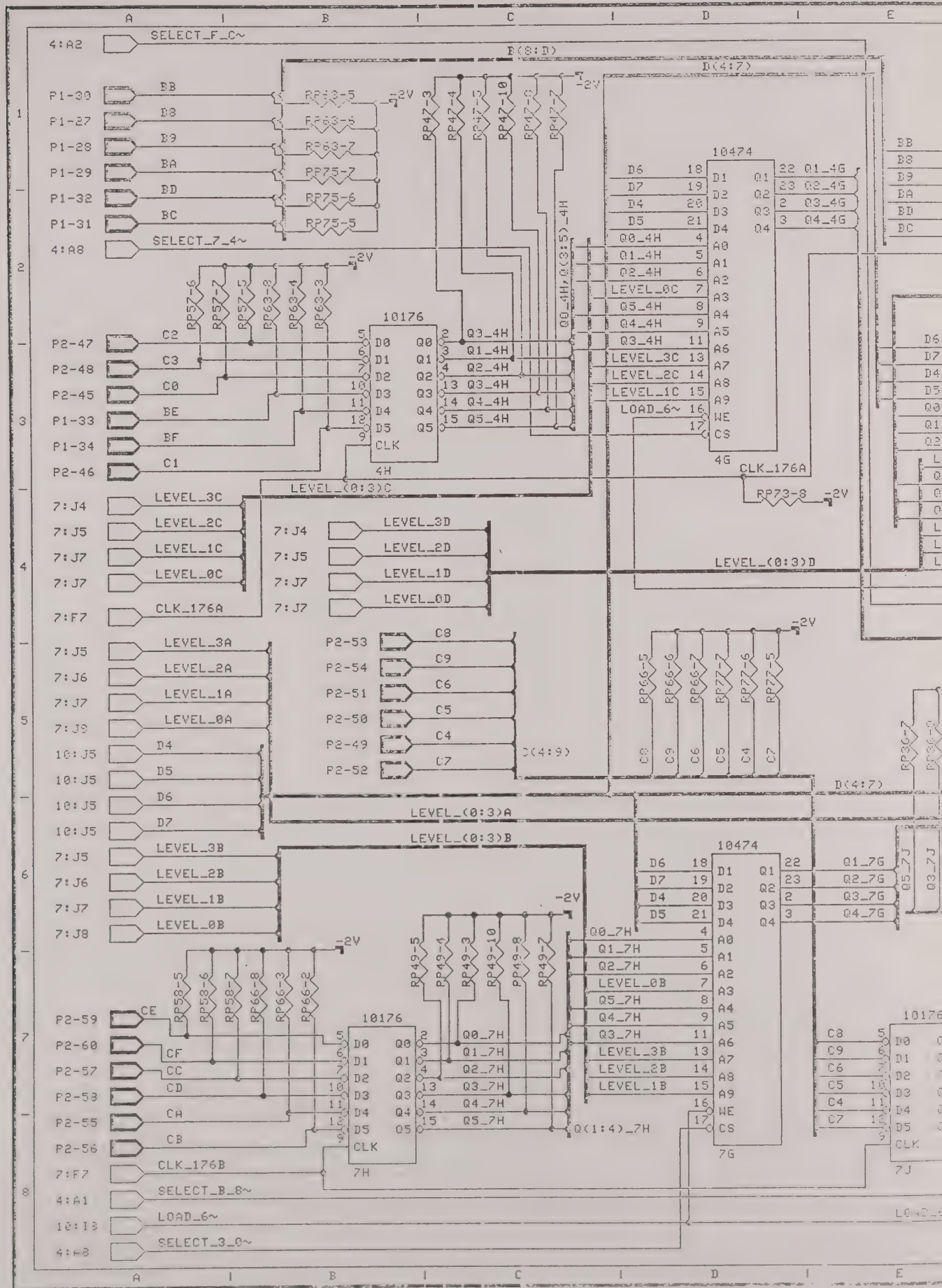
MODEL	PART NUMBER	REV
4480	0121-0421	54

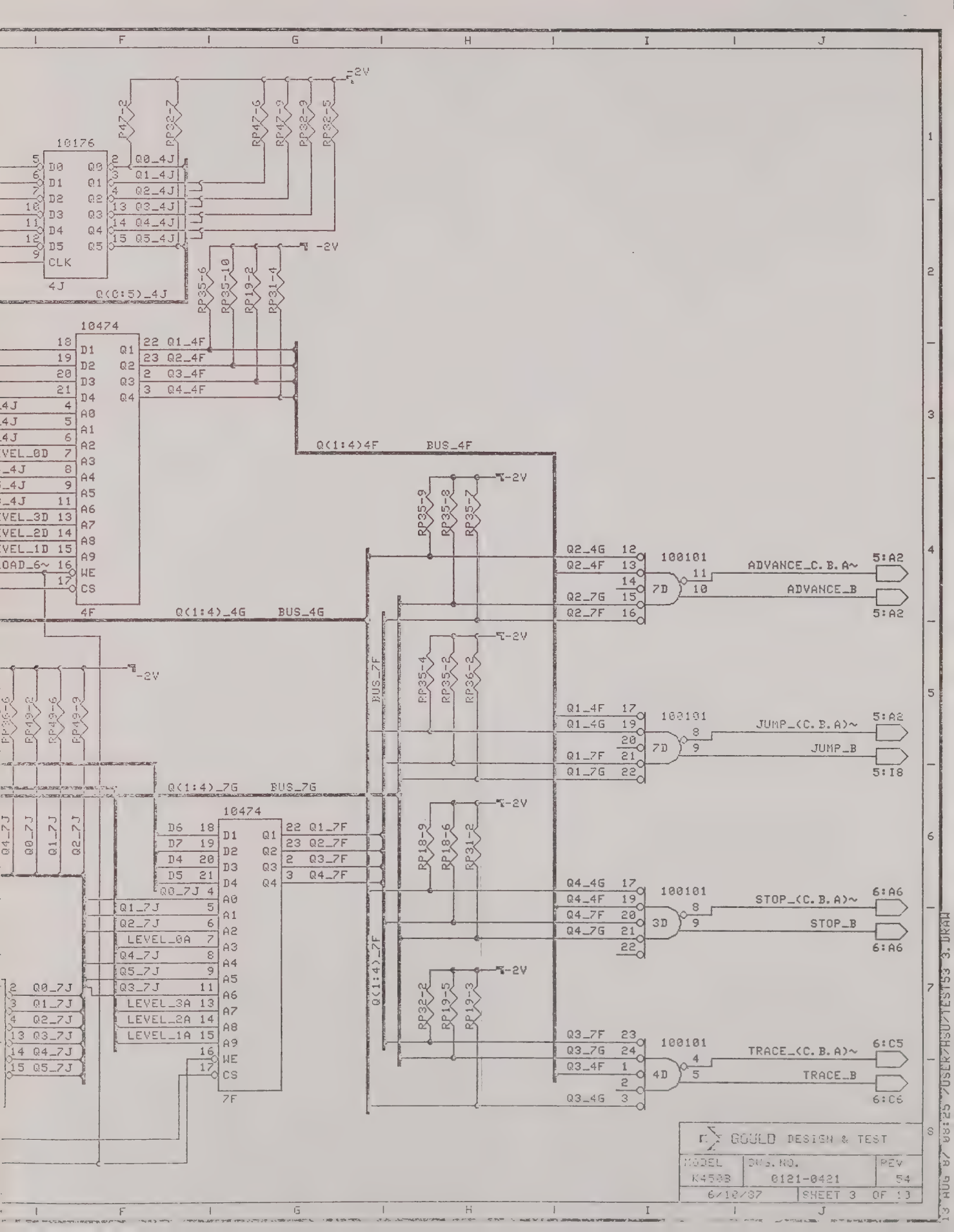
6 15 87 | SHEET 1 OF 10

13 AUG 87 08:29 /USER/HSU/TEST53 1.DRAW


A(6:3)
SELECT_7_4~
P2-73
P2-74
P2-71
P2-72
P2-67
P2-68
AA
AB
A8
A9
A6
A7
RP53-5
RP53-6
RP53-7
RP67-9
RP67-3
RP67-4
-2V
10474
10176
8J
8F
CLK_176B
SELECT_F_C~
from E8
RP59-2
P2-63
P2-66
P2-65
P2-62
P2-61
P2-64
A2
A5
A4
A1
A0
A3
RP67-6
RP67-7
RP67-5
RP78-7
RP78-6
RP78-5
RP50-6
RP50-9
RP50-2
RP37-7
RP37-6
RP37-9
Q0_8J
Q1_8J
Q2_8J
Q3_8J
Q4_8J
Q5_8J
D10
D11
D8
D9
LEVEL_0B
LEVEL_3B
LEVEL_2B
LEVEL_1B
LOAD_6~
P2-76
P2-75
P2-78
P2-77
AD
AC
AF
AE
RP68-2
RP68-3
RP68-4
RP79-7
RP79-6
RP79-5
P2-80
P2-79
E1
E0
7:J5
7:J6
7:J7
7:J8
LEVEL_3B
LEVEL_2B
LEVEL_1B
LEVEL_0B
LEVEL_(0:3)B
LEVEL_(0:3)A
10:J4
10:J4
10:J4
10:J4
D11
D10
D9
D8
7:J5
7:J6
7:J7
7:J8
LEVEL_3A
LEVEL_2A
LEVEL_1A
LEVEL_0A
Q0_9H
Q1_9H
Q2_9H
Q5_9H
Q4_9H
Q3_9H
Q0_9H,Q(3:5)_9H
RP51-4
RP51-5
RP51-3
RP51-2
RP51-7
RP51-6
RP60-5
RP60-6
RP60-7
RP68-7
RP68-6
RP68-5
P2-82
P2-81
P2-84
P2-85
P2-86
P2-83
E3
E2
E5
E6
E7
E4
9H
9G
9J
Q1_9G
Q2_9G
Q3_9G
Q4_9G
RP51-8
RP60-3
7:F7
4:A8
10:I8
4:A1
CLK_176B
SELECT_3_0~
LOAD_6~
SELECT_B_8~
to


SELECT_7_4~
RP59-3
-2V
RP38-10
RP25-2
RP38-3
RP37-2
10474
D10
D11
D8
D9
Q0_8H
Q1_8H
Q2_8H
LEVEL_0A
Q5_8H
Q4_8H
Q3_8H
LEVEL_3A
LEVEL_2A
LEVEL_1A
LOAD_6~
Q1_8G
Q2_8G
Q3_8G
Q4_8G
8G
RP50-3
RP50-4
RP50-5
RP50-10
RP50-8
RP50-7
10176
AA
AB
A8
A9
A6
A7
CLK
8H
Q(1:4)_8H
D(8:11)
Q(1:4)_8G
Q(1:4)_8F
RP25-3
RP25-6
RP25-4
R10 68
100101
Q2_9G
Q2_8G
Q2_9F
Q2_8F
ADVANCE_C.B.A~
ADVANCE_A
5:A2
RP25-10
RP38-8
RP38-5
R11 68
Q1_8F
Q1_8G
Q1_9G
Q1_9F
JUMP_(C.B.A)~
JUMP_A
5:I3
Q(1:4)_9G
RP51-10
RP38-9
RP38-6
RP38-7
10474
Q1_9J
Q2_9J
LEVEL_0B
Q4_9J
Q5_9J
Q3_9J
LEVEL_3B
LEVEL_2B
LEVEL_1B
Q0_9J
Q1_9J
Q2_9J
Q3_9J
Q4_9J
Q5_9J
9F
RP37-5
RP37-3
RP37-4
R12 68
Q4_9F
Q4_9G
Q4_8G
Q4_8F
STOP_(C.B.A)~
STOP_A
6:A7
RP38-4
RP38-2
RP25-5
Q3_8F
Q3_8G
Q3_9G
Q3_9F
TRACE_(C.B.A)~
TRACE_A
6:C6
RP60-8
RP60-2
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0421
REV F4
6/10/87
SHEET 2 OF 10


SELECT_F_C~
B(8:D)
D(4:7)
BB
B8
B9
BA
BD
BC
SELECT_7_4~
P1-30
P1-27
P1-28
P1-29
P1-32
P1-31
4:A2
4:A8
RP63-5
RP63-6
RP63-7
RP75-7
RP75-6
RP75-5
-2V
RP47-3
RP47-4
RP47-5
RP47-10
RP47-8
RP47-7
10474
Q0_4H,Q(3:5)_4H
Q0_4H
Q1_4H
Q2_4H
LEVEL_0C
Q5_4H
Q4_4H
Q3_4H
LEVEL_3C
LEVEL_2C
LEVEL_1C
LOAD_6~
Q1_4G
Q2_4G
Q3_4G
Q4_4G
4G
CLK_176A
RP73-8
RP57-6
RP57-7
RP57-5
RP63-8
RP63-4
RP63-3
10176
4H
C2
C3
C0
BE
BF
C1
P2-47
P2-48
P2-45
P1-33
P1-34
P2-46
Q3_4H
Q1_4H
Q2_4H
Q3_4H
Q4_4H
Q5_4H
LEVEL_(0:3)C
LEVEL_(0:3)D
7:J4
7:J5
7:J7
7:J7
7:F7
LEVEL_3C
LEVEL_2C
LEVEL_1C
LEVEL_0C
CLK_176A
7:J4
7:J5
7:J7
7:J7
LEVEL_3D
LEVEL_2D
LEVEL_1D
LEVEL_0D
P2-53
P2-54
P2-51
P2-50
P2-49
P2-52
C8
C9
C6
C5
C4
C7
C(4:9)
RP66-5
RP66-6
RP66-7
RP77-7
RP77-6
RP77-5
RP36-7
7:J5
7:J6
7:J7
7:J9
10:J5
10:J5
10:J5
10:J5
LEVEL_3A
LEVEL_2A
LEVEL_1A
LEVEL_0A
D4
D5
D6
D7
LEVEL_(0:3)A
LEVEL_(0:3)B
7:J5
7:J6
7:J7
7:J8
LEVEL_3B
LEVEL_2B
LEVEL_1B
LEVEL_0B
Q1_7G
Q2_7G
Q3_7G
Q4_7G
Q5_7J
Q3_7J
RP49-5
RP49-4
RP49-3
RP49-10
RP49-8
RP49-7
RP58-5
RP58-6
RP58-7
RP66-8
RP66-3
RP66-2
10176
7H
P2-59
P2-60
P2-57
P2-58
P2-55
P2-56
7:F7
4:A1
10:I3
4:H3
CE
CF
CC
CD
CA
CB
CLK_176B
SELECT_B_8~
LOAD_6~
SELECT_3_0~
Q0_7H
Q1_7H
Q2_7H
Q3_7H
Q4_7H
Q5_7H
Q(1:4)_7H
LEVEL_0B
LEVEL_3B
LEVEL_2B
LEVEL_1B
7G
7J


10176
4J
Q(0:5)_4J
Q0_4J
Q1_4J
Q2_4J
Q3_4J
Q4_4J
Q5_4J
-2V
10474
4F
Q(1:4)4F
BUS_4F
Q(1:4)_4G
BUS_4G
Q(1:4)_7G
BUS_7G
Q(1:4)_7F
BUS_7F
7F
Q1_4F
Q2_4F
Q3_4F
Q4_4F
Q1_7F
Q2_7F
Q3_7F
Q4_7F
Q2_4G
Q1_4G
Q4_4G
Q3_7F
Q3_7G
Q3_4F
Q3_4G
100101
7D
3D
4D
ADVANCE_C.B.A~
ADVANCE_B
JUMP_(C.B.A)~
JUMP_B
STOP_(C.B.A)~
STOP_B
TRACE_(C.B.A)~
TRACE_B
5:A2
5:I8
6:A6
6:C5
6:C6
LEVEL_0A
LEVEL_3A
LEVEL_2A
LEVEL_1A
GOULD DESIGN & TEST
MODEL K4503
DWG. NO. 0121-0421
REV 54
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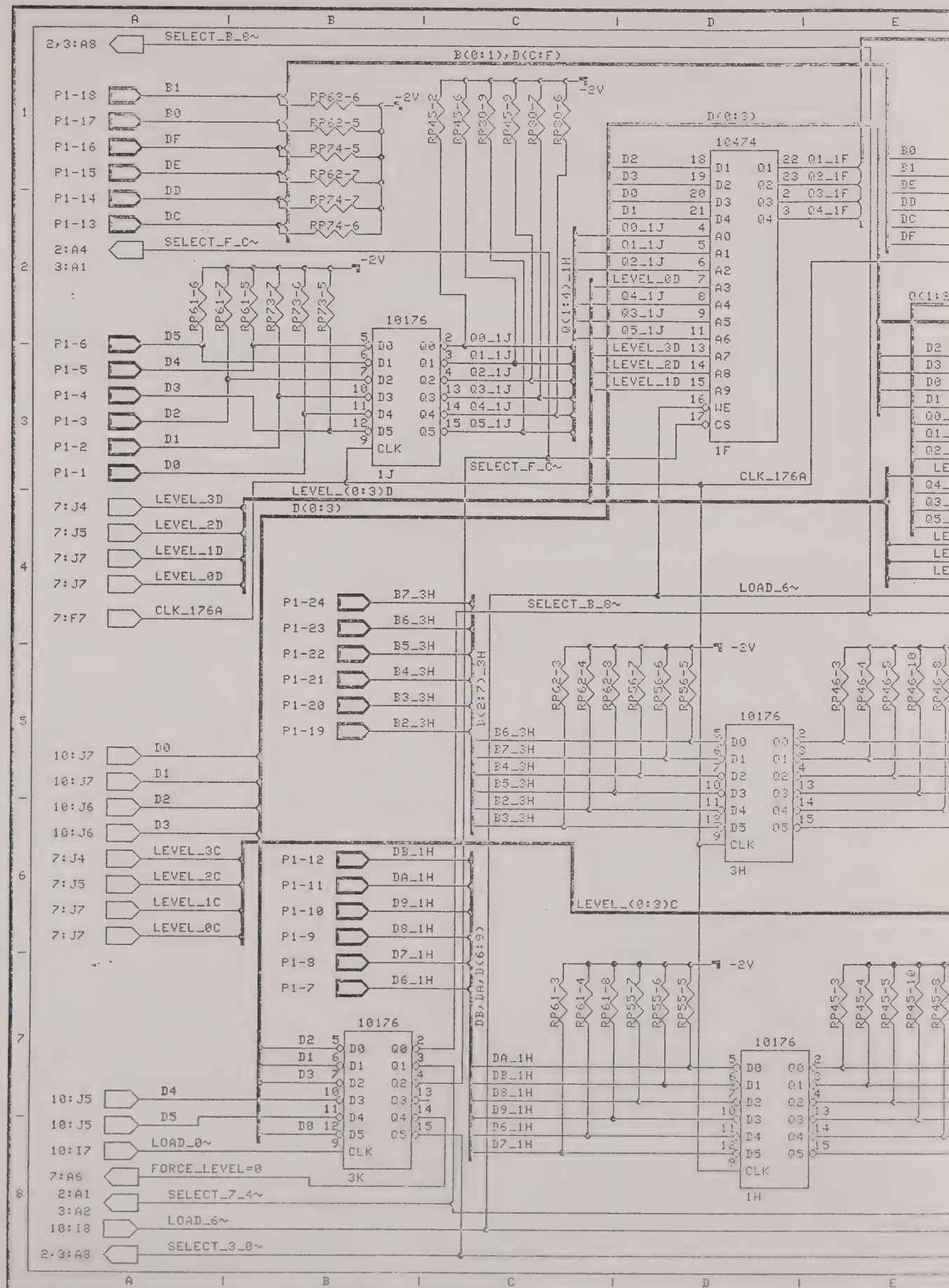
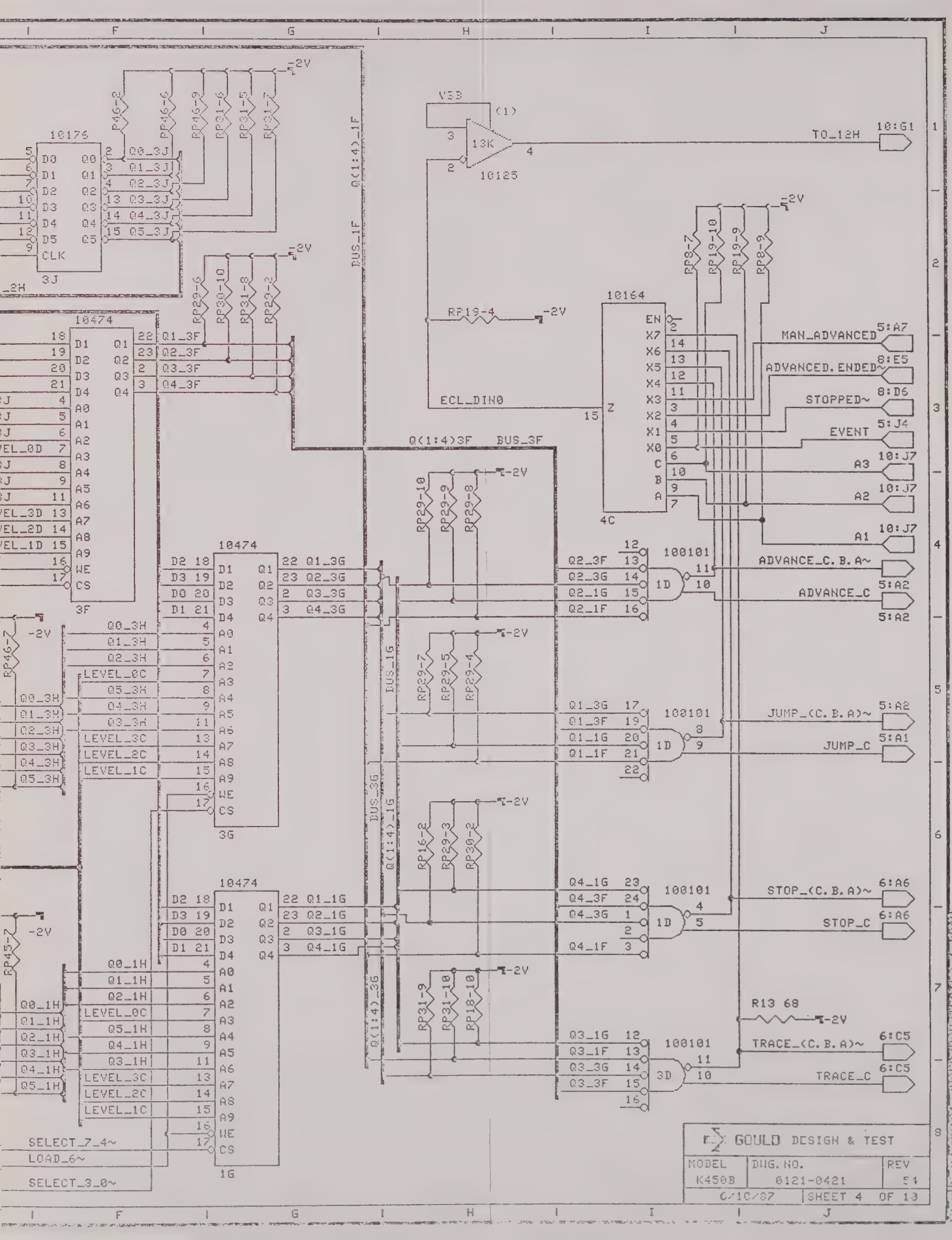
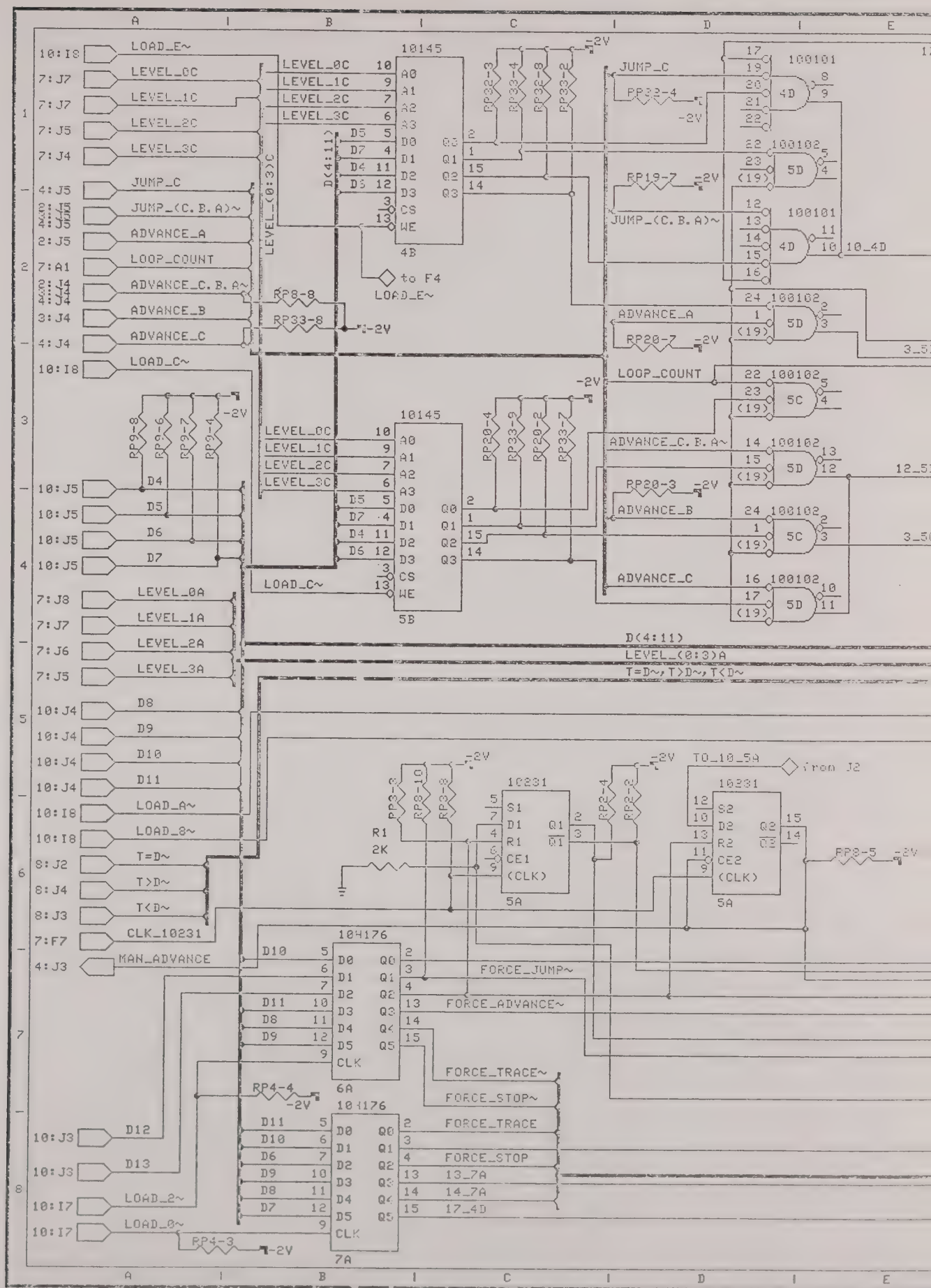
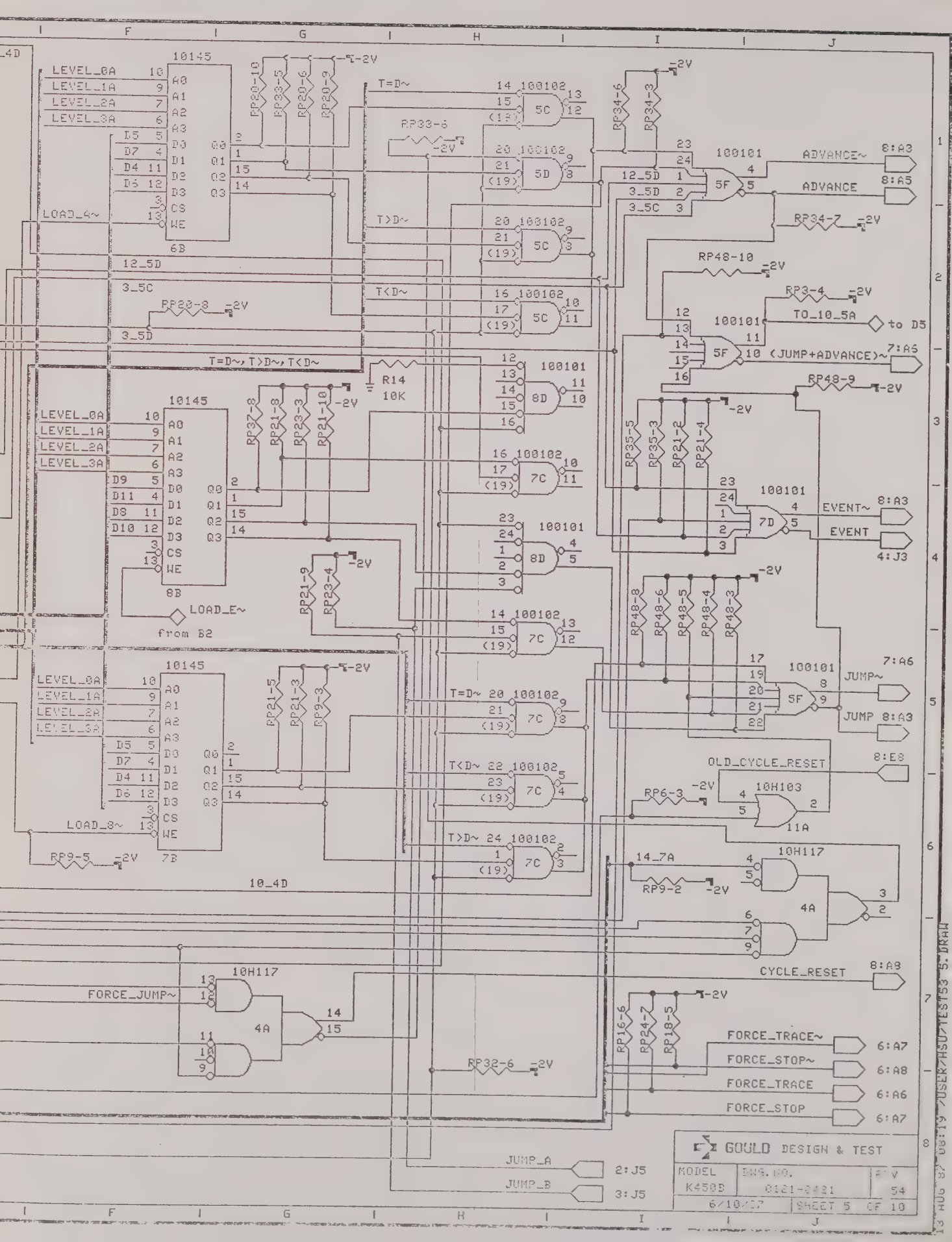

SELECT_B_8~
B(0:1),D(C:F)
P1-18
P1-17
P1-16
P1-15
P1-14
P1-13
B1
B0
DF
DE
DD
DC
RP62-6
RP62-5
RP74-5
RP62-7
RP74-7
RP74-6
-2V
SELECT_F_C~
2:A4
3:A1
RP61-6
RP61-7
RP61-5
RP73-7
RP73-6
RP73-5
10176
P1-6
P1-5
P1-4
P1-3
P1-2
P1-1
D5
D4
D3
D2
D1
D0
Q0_1J
Q1_1J
Q2_1J
Q3_1J
Q4_1J
Q5_1J
CLK
1J
LEVEL_(0:3)D
D(0:3)
7:J4
7:J5
7:J7
7:J7
7:F7
LEVEL_3D
LEVEL_2D
LEVEL_1D
LEVEL_0D
CLK_176A
RP45-2
RP45-6
RP30-9
RP45-9
RP30-7
RP30-6
Q(1:4)_1H
10474
D(0:3)
D2
D3
D0
D1
Q0_1J
Q1_1J
Q2_1J
LEVEL_0D
Q4_1J
Q3_1J
Q5_1J
LEVEL_3D
LEVEL_2D
LEVEL_1D
WE
CS
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
Q1_1F
Q2_1F
Q3_1F
Q4_1F
1F
CLK_176A
B0
B1
DE
DD
DC
DF
LOAD_6~
P1-24
P1-23
P1-22
P1-21
P1-20
P1-19
B7_3H
B6_3H
B5_3H
B4_3H
B3_3H
B2_3H
B(2:7)_3H
RP62-3
RP62-4
RP62-8
RP56-7
RP56-6
RP56-5
-2V
10176
3H
10:J7
10:J7
10:J6
10:J6
D0
D1
D2
D3
7:J4
7:J5
7:J7
7:J7
LEVEL_3C
LEVEL_2C
LEVEL_1C
LEVEL_0C
P1-12
P1-11
P1-10
P1-9
P1-8
P1-7
DB_1H
DA_1H
D9_1H
D8_1H
D7_1H
D6_1H
DB,DA,D(6:9)
LEVEL_(0:3)C
RP61-3
RP61-4
RP61-8
RP55-7
RP55-6
RP55-5
10176
1H
10:J5
10:J5
10:I7
7:A6
2:A1
3:A2
10:I8
2,3:A8
D4
D5
LOAD_0~
FORCE_LEVEL=0
SELECT_7_4~
LOAD_6~
SELECT_3_0~
3K
RP46-3
RP46-1
RP46-5
RP46-10
RP46-8
RP45-3
RP45-4
RP45-5
RP45-10
RP45-8



10176
3J
10474
3F
10474
3G
10474
1G
10125
13K
10164
4C
100101
1D
3D
TO_12H
10:G1
MAN_ADVANCED
5:A7
ADVANCED.ENDED~
8:E5
STOPPED~
8:D6
EVENT
5:J4
A3
10:J7
A2
10:J7
A1
10:J7
ADVANCE_C.B.A~
5:A2
ADVANCE_C
5:A2
JUMP_(C.B.A)~
5:A2
JUMP_C
5:A1
STOP_(C.B.A)~
6:A6
STOP_C
6:A6
TRACE_(C.B.A)~
6:C5
TRACE_C
6:C5
R13 68
ECL_DIN0
Q(1:4)3F
BUS_3F
Q(1:4)_1F
BUS_1F
BUS_3G
Q(1:4)_3G
Q(1:4)_1G
SELECT_7_4~
LOAD_6~
SELECT_3_0~
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0421
REV 54
6/10/87
SHEET 4 OF 13
13 AUG 87 08:21 /USER/HSU/TEST53 4.DRAW


10:I8 LOAD_E~
7:J7 LEVEL_0C
7:J7 LEVEL_1C
7:J5 LEVEL_2C
7:J4 LEVEL_3C
4:J5 JUMP_C
JUMP_(C.B.A)~
2:J5 ADVANCE_A
7:A1 LOOP_COUNT
ADVANCE_C.B.A~
3:J4 ADVANCE_B
4:J4 ADVANCE_C
10:I8 LOAD_C~
LEVEL_(0:3)C
D(4:11)
10145
4B
5B
to F4
LOAD_E~
RP8-8
RP33-8
-2V
RP32-3
RP33-4
RP32-8
RP33-2
RP32-4
RP19-7
RP20-7
RP20-4
RP33-9
RP20-2
RP33-7
RP20-3
RP9-8
RP9-6
RP9-7
RP9-4
10:J5 D4
10:J5 D5
10:J5 D6
10:J5 D7
100101
100102
4D
5D
5C
10_4D
12_5
3_5
LEVEL_(0:3)A
T=D~, T>D~, T<D~
7:J8 LEVEL_0A
7:J7 LEVEL_1A
7:J6 LEVEL_2A
7:J5 LEVEL_3A
10:J4 D8
10:J4 D9
10:J4 D10
10:J4 D11
10:I8 LOAD_A~
10:I8 LOAD_B~
8:J2 T=D~
8:J4 T>D~
8:J3 T<D~
7:F7 CLK_10231
4:J3 MAN_ADVANCE
R1
2K
RP3-3
RP3-10
RP3-8
RP3-4
RP3-2
10231
5A
TO_10_5A
from J2
RP3-5
104176
6A
7A
D10
D11
D8
D9
D6
D7
CLK
FORCE_JUMP~
FORCE_ADVANCE~
FORCE_TRACE~
FORCE_STOP~
FORCE_TRACE
FORCE_STOP
13_7A
14_7A
17_4D
RP4-4
RP4-3
10:J3 D12
10:J3 D13
10:I7 LOAD_2~
10:I7 LOAD_0~


10145
LEVEL_0A
LEVEL_1A
LEVEL_2A
LEVEL_3A
D5
D7
D4
D6
LOAD_4~
6B
12_5D
3_5C
3_5D
RP20-8
RP20-10
RP33-5
RP20-6
RP20-9
RP33-8
T=D~
T>D~
T<D~
100102
5C
5D
100101
5F
ADVANCE~
ADVANCE
8:A3
8:A5
RP34-6
RP34-3
RP34-7
RP48-10
RP3-4
TO_10_5A
to D5
(JUMP+ADVANCE)~
7:A5
R14
10K
8D
RP48-9
RP37-8
RP21-8
RP23-3
RP21-10
8B
LOAD_E~
from B2
RP21-9
RP23-4
7C
RP35-5
RP35-3
RP21-2
RP21-4
7D
EVENT~
EVENT
4:J3
RP48-8
RP48-6
RP48-5
RP48-4
RP48-3
JUMP~
JUMP 8:A3
7:A6
7B
RP21-5
RP21-3
RP9-3
LOAD_8~
RP9-5
OLD_CYCLE_RESET
8:E8
10H103
11A
RP6-3
10_4D
14_7A
RP9-2
10H117
4A
CYCLE_RESET
8:A8
FORCE_JUMP~
RP32-6
RP16-6
RP24-7
RP18-5
FORCE_TRACE~
FORCE_STOP~
FORCE_TRACE
FORCE_STOP
6:A7
6:A8
6:A6
JUMP_A
JUMP_B
2:J5
3:J5
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-2431
REV 54
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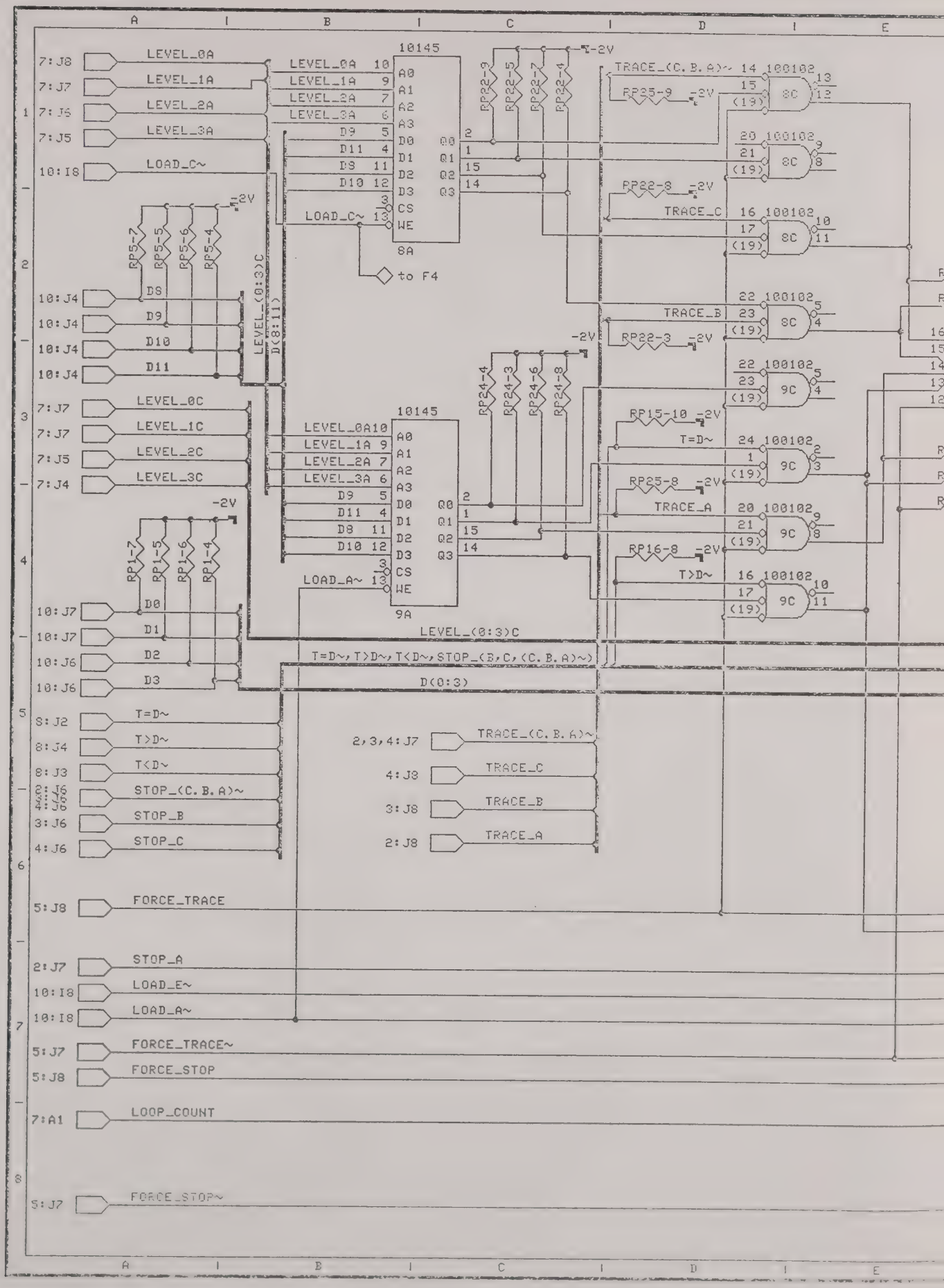
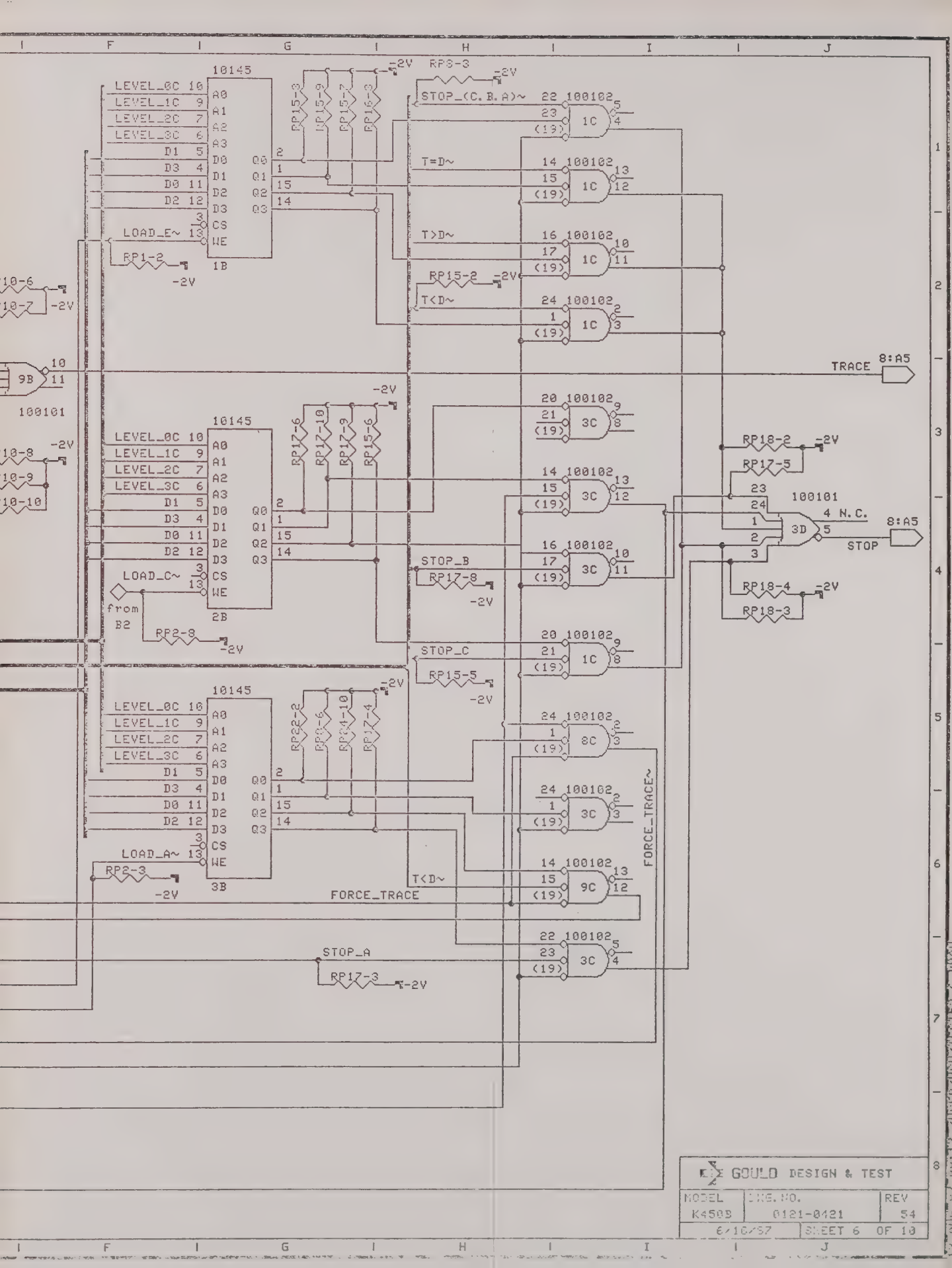
-2V


LEVEL_0A
LEVEL_1A
LEVEL_2A
LEVEL_3A
LOAD_C~
LEVEL_0C
LEVEL_1C
LEVEL_2C
LEVEL_3C
LOAD_A~
10145
8A
9A
to F4
RP5-7
RP5-5
RP5-6
RP5-4
RP1-7
RP1-5
RP1-6
RP1-4
RP24-4
RP24-3
RP24-6
RP24-8
RP32-3
RP32-5
RP32-7
RP32-4
RP25-9
RP22-8
RP22-3
RP15-10
RP25-8
RP16-8
-2V
LEVEL_(0:3)C
D(8:11)
D(0:3)
T=D~, T>D~, T<D~, STOP_(B,C,(C.B.A)~)
TRACE_(C.B.A)~
TRACE_C
TRACE_B
TRACE_A
T=D~
T>D~
T<D~
STOP_(C.B.A)~
STOP_B
STOP_C
FORCE_TRACE
STOP_A
LOAD_E~
FORCE_TRACE~
FORCE_STOP
LOOP_COUNT
FORCE_STOP~


10145
LEVEL_0C
LEVEL_1C
LEVEL_2C
LEVEL_3C
D1
D3
D0
D2
LOAD_E~
LOAD_C~
LOAD_A~
1B
2B
3B
RP1-2
RP2-8
RP2-3
RP15-3
RP15-9
RP15-7
RP16-3
RP17-6
RP17-10
RP17-9
RP15-6
RP2-2
RP2-6
RP14-10
RP17-4
-2V
STOP_(C.B.A)~
T=D~
T>D~
T<D~
RP15-2
STOP_B
RP17-8
STOP_C
RP15-5
STOP_A
RP17-3
FORCE_TRACE
FORCE_TRACE~
100102
100101
1C
3C
8C
9C
3D
9B
TRACE
8:A5
STOP
4 N.C.
RP18-2
RP17-5
RP18-4
RP18-3
from B2
GOULD DESIGN & TEST
MODEL K4503
DWG. NO. 0121-0421
REV 54
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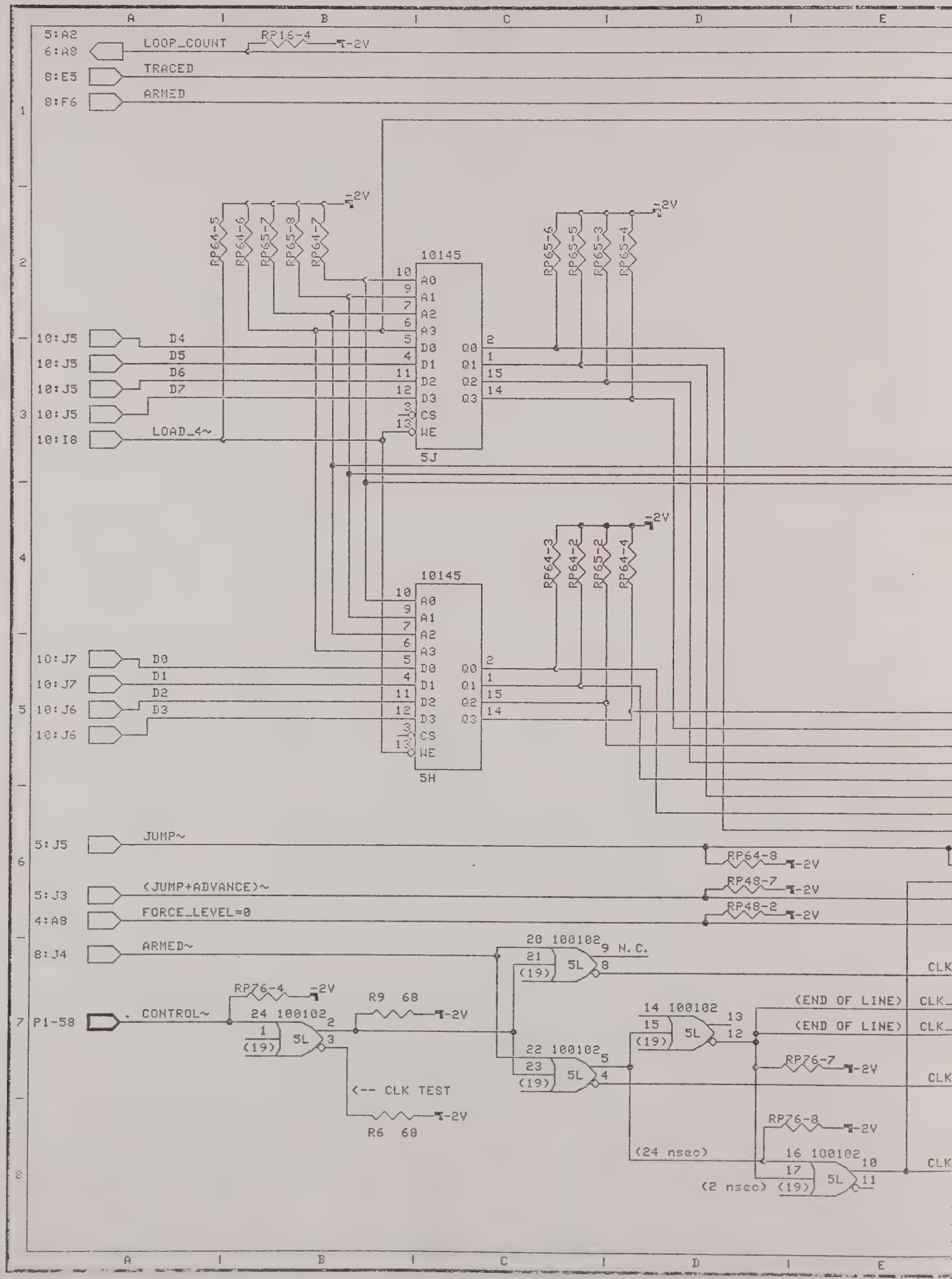
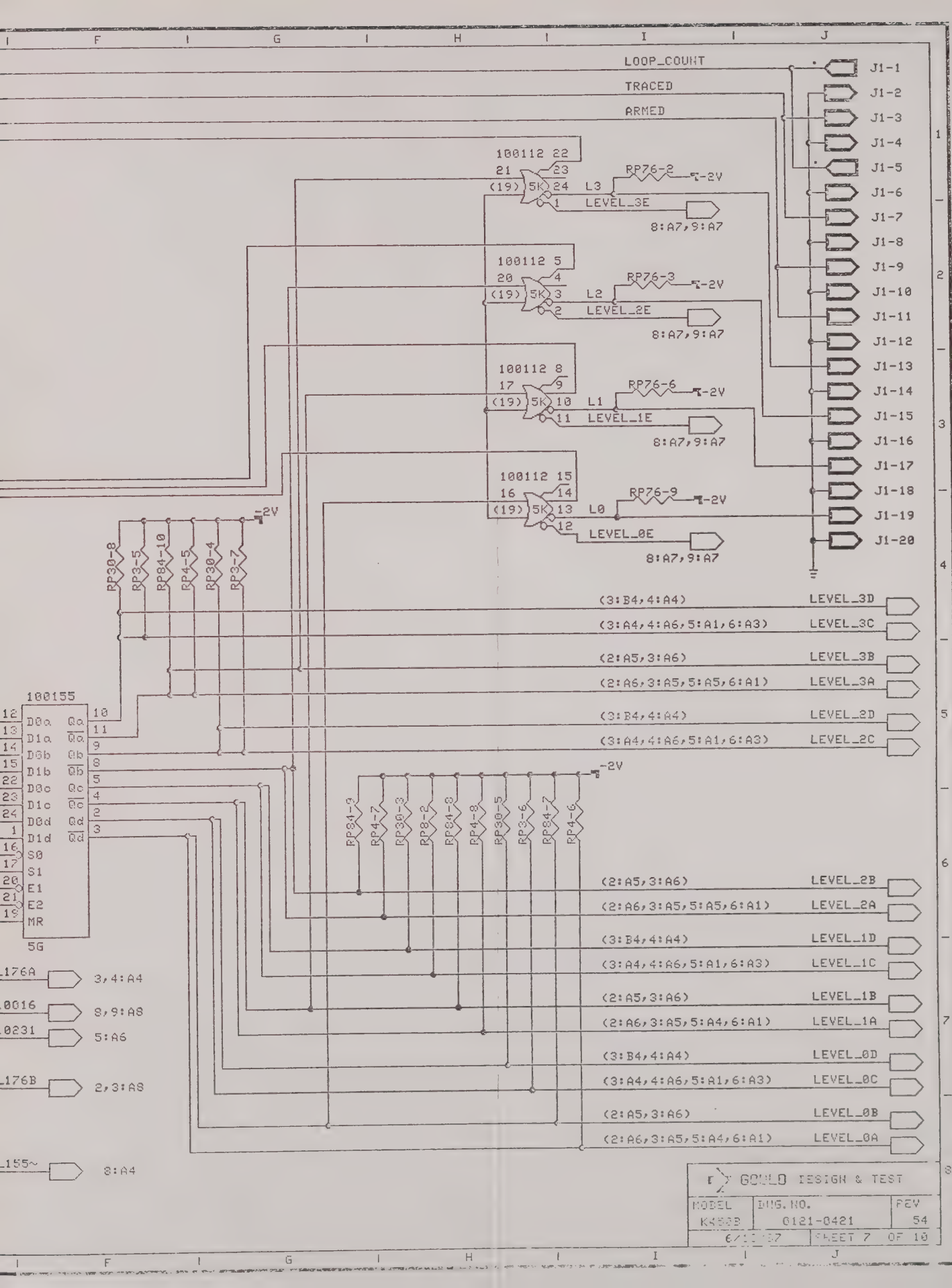

5:A2
6:A8
LOOP_COUNT
RP16-4
-2V
8:E5
TRACED
8:F6
ARMED
10145
5J
10:J5
D4
D5
D6
D7
10:I8
LOAD_4~
RP64-5
RP64-6
RP65-7
RP65-8
RP64-7
RP65-6
RP65-5
RP65-3
RP65-4
10145
5H
10:J7
D0
D1
D2
10:J6
D3
RP64-3
RP64-2
RP65-2
RP64-4
5:J5
JUMP~
RP64-8
5:J3
(JUMP+ADVANCE)~
RP48-7
4:A8
FORCE_LEVEL=0
RP48-2
8:J4
ARMED~
20 100102
21
(19)
5L
9 N.C.
8
CLK
P1-58
CONTROL~
RP76-4
24 100102
1
(19)
5L
2
3
R9 68
(-- CLK TEST
R6 68
22 100102
23
(19)
5L
5
4
14 100102
15
(19)
5L
13
12
(END OF LINE)
CLK
RP76-7
RP76-8
(24 nsec)
16 100102
17
(19)
5L
10
11
(2 nsec)


LOOP_COUNT
TRACED
ARMED
J1-1
J1-2
J1-3
J1-4
J1-5
J1-6
J1-7
J1-8
J1-9
J1-10
J1-11
J1-12
J1-13
J1-14
J1-15
J1-16
J1-17
J1-18
J1-19
J1-20
100112 22
RP76-2
-2V
L3
LEVEL_3E
8:A7,9:A7
100112 5
RP76-3
L2
LEVEL_2E
100112 8
RP76-6
L1
LEVEL_1E
100112 15
RP76-9
L0
LEVEL_0E
RP30-8
RP3-5
RP84-10
RP4-5
RP30-4
RP3-7
100155
D0a Qa
D1a Qa
D0b Qb
D1b Qb
D0c Qc
D1c Qc
D0d Qd
D1d Qd
S0
S1
E1
E2
MR
5G
RP84-9
RP4-7
RP30-3
RP8-2
RP84-8
RP4-8
RP30-5
RP3-6
RP84-7
RP4-6
(3:B4,4:A4) LEVEL_3D
(3:A4,4:A6,5:A1,6:A3) LEVEL_3C
(2:A5,3:A6) LEVEL_3B
(2:A6,3:A5,5:A5,6:A1) LEVEL_3A
(3:B4,4:A4) LEVEL_2D
(3:A4,4:A6,5:A1,6:A3) LEVEL_2C
(2:A5,3:A6) LEVEL_2B
(2:A6,3:A5,5:A5,6:A1) LEVEL_2A
(3:B4,4:A4) LEVEL_1D
(3:A4,4:A6,5:A1,6:A3) LEVEL_1C
(2:A5,3:A6) LEVEL_1B
(2:A6,3:A5,5:A4,6:A1) LEVEL_1A
(3:B4,4:A4) LEVEL_0D
(3:A4,4:A6,5:A1,6:A3) LEVEL_0C
(2:A5,3:A6) LEVEL_0B
(2:A6,3:A5,5:A4,6:A1) LEVEL_0A
3,4:A4
8,9:A8
5:A6
2,3:A8
8:A4
GOULD DESIGN & TEST
MODEL K4500
DWG. NO. 0121-0421
REV 54
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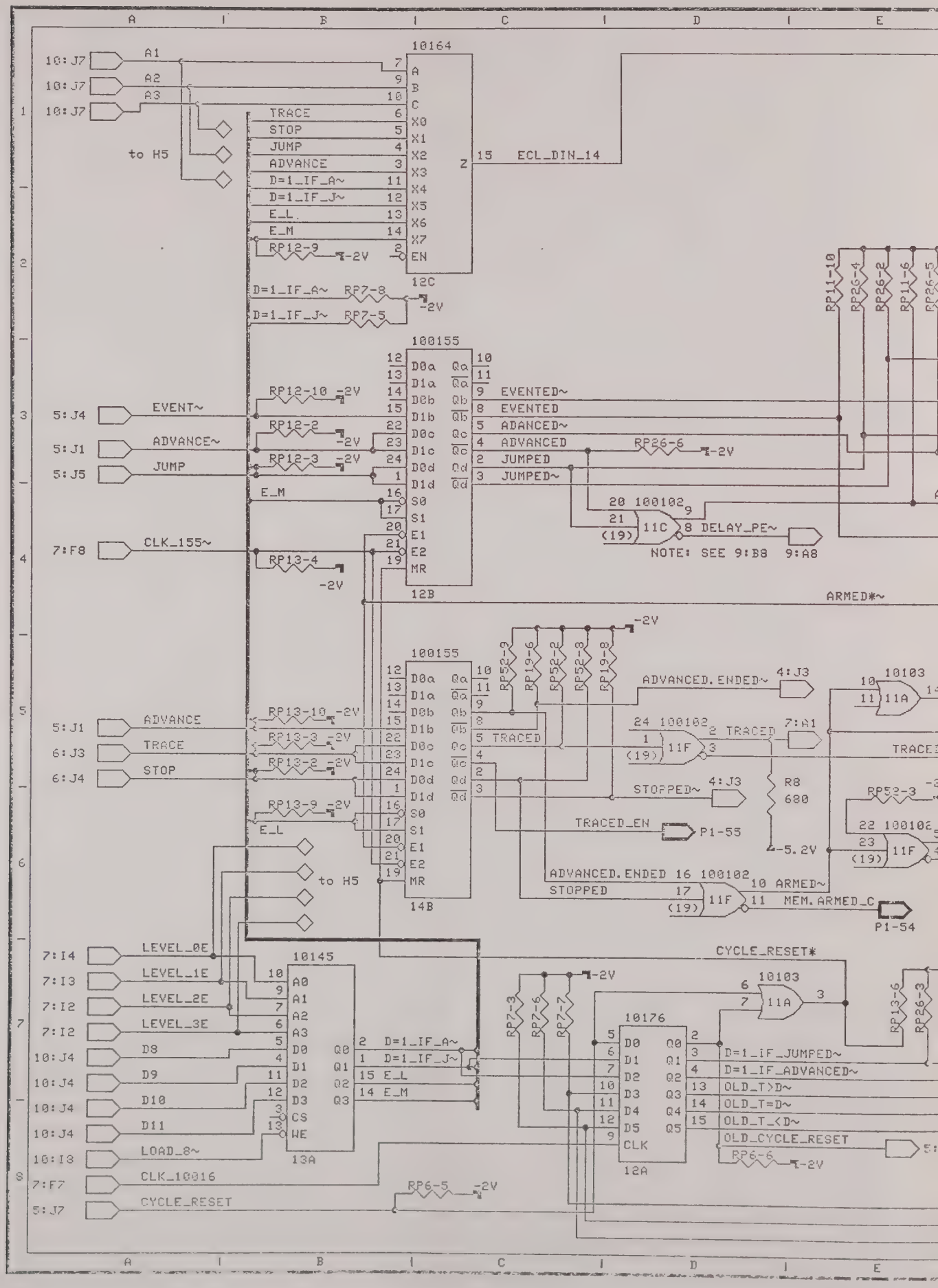
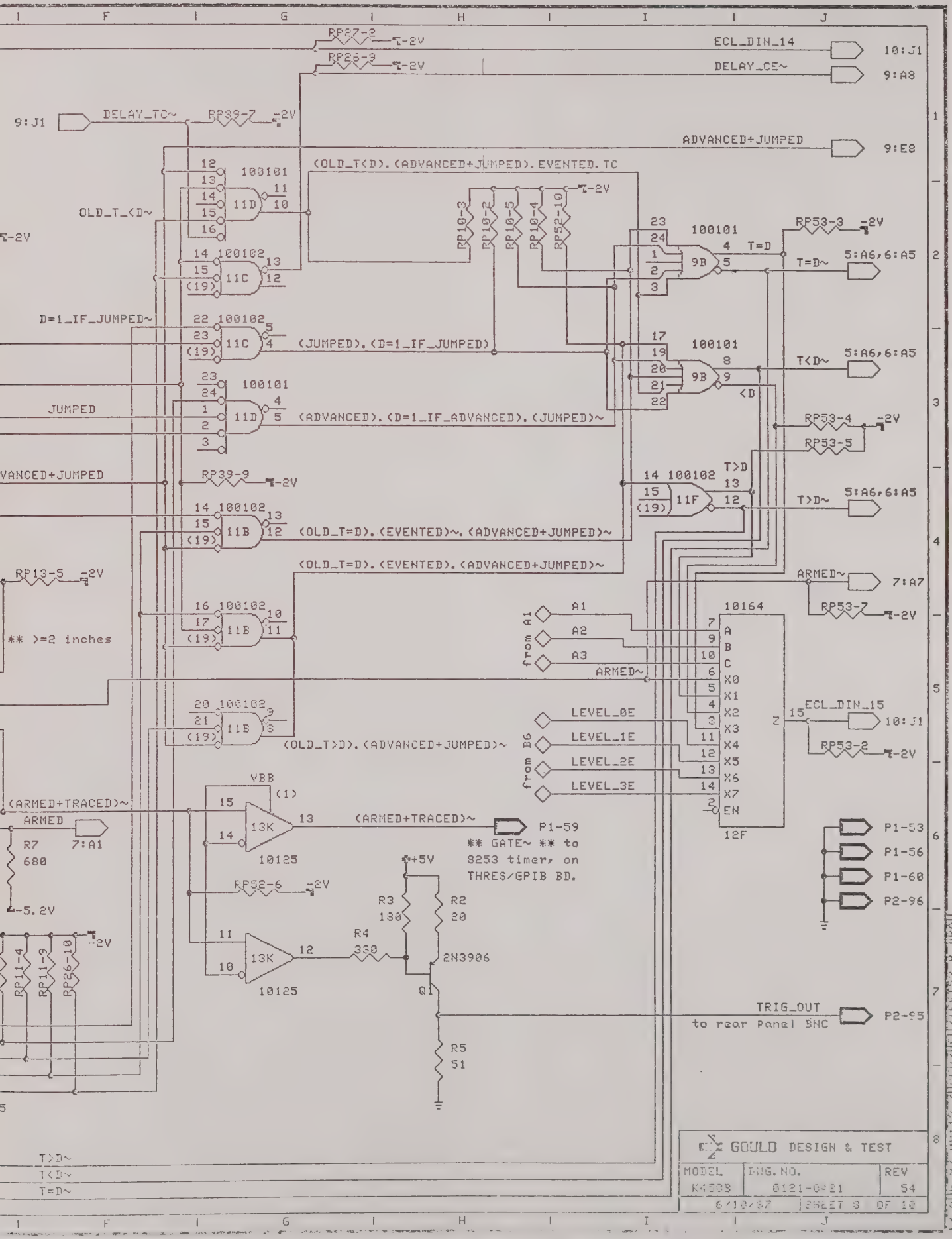
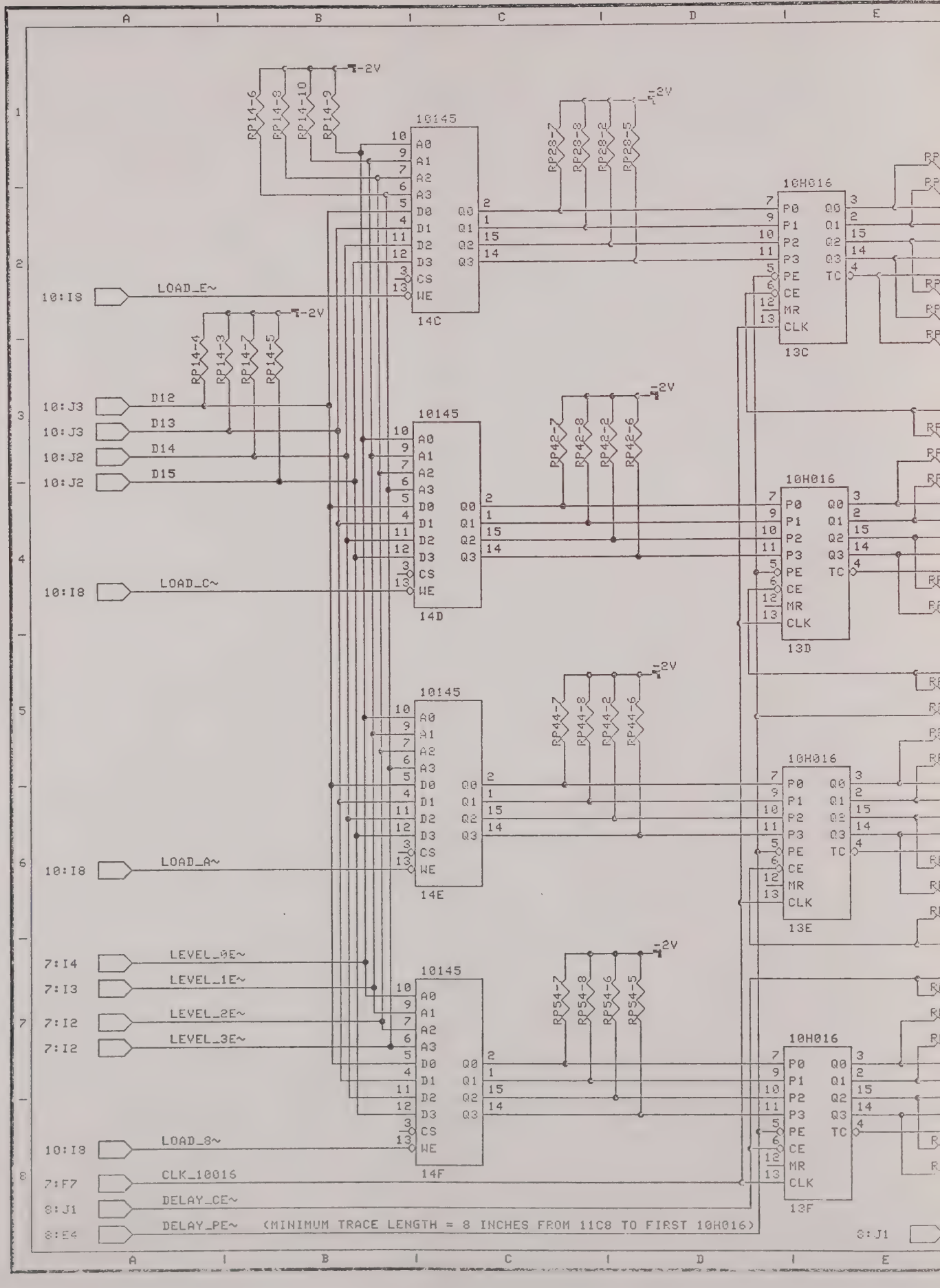
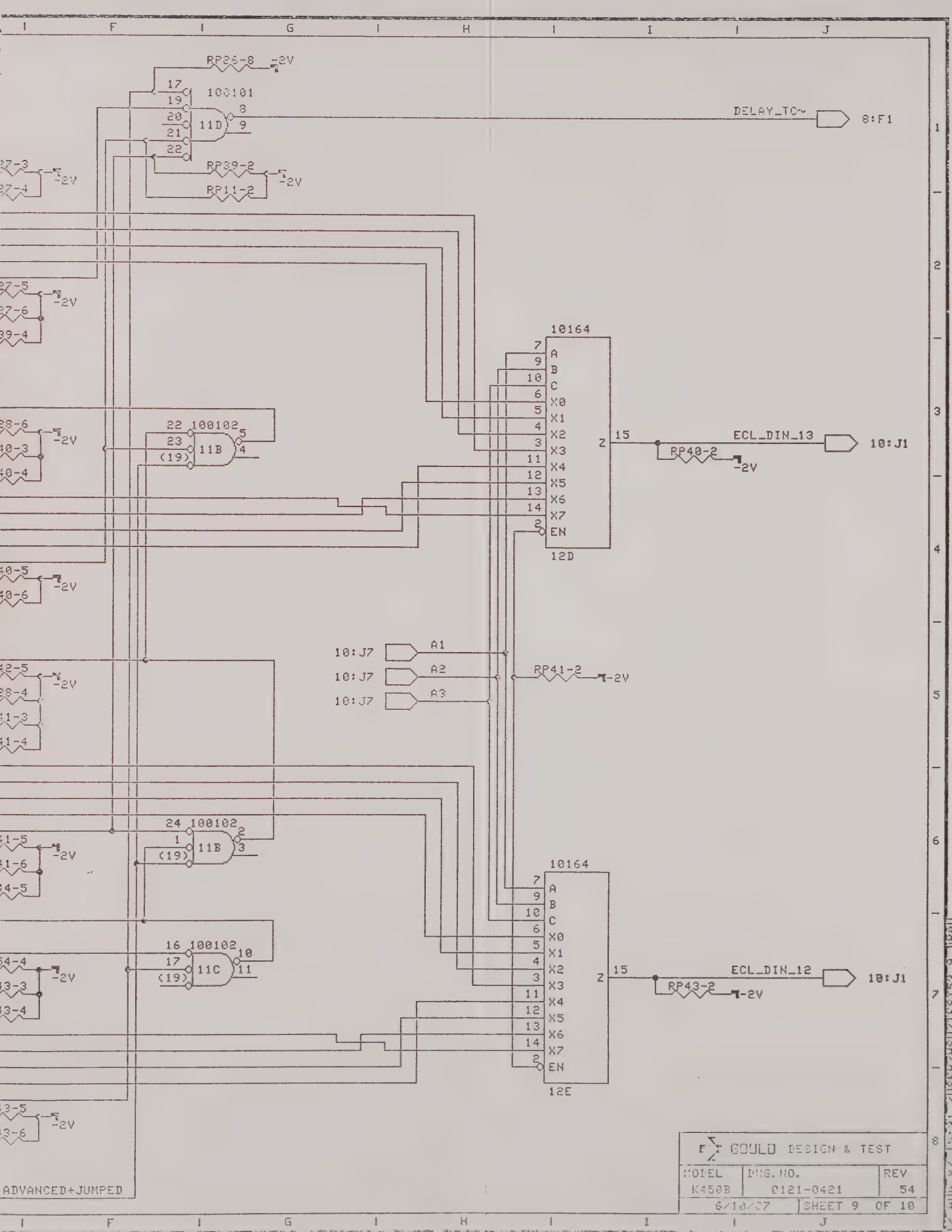
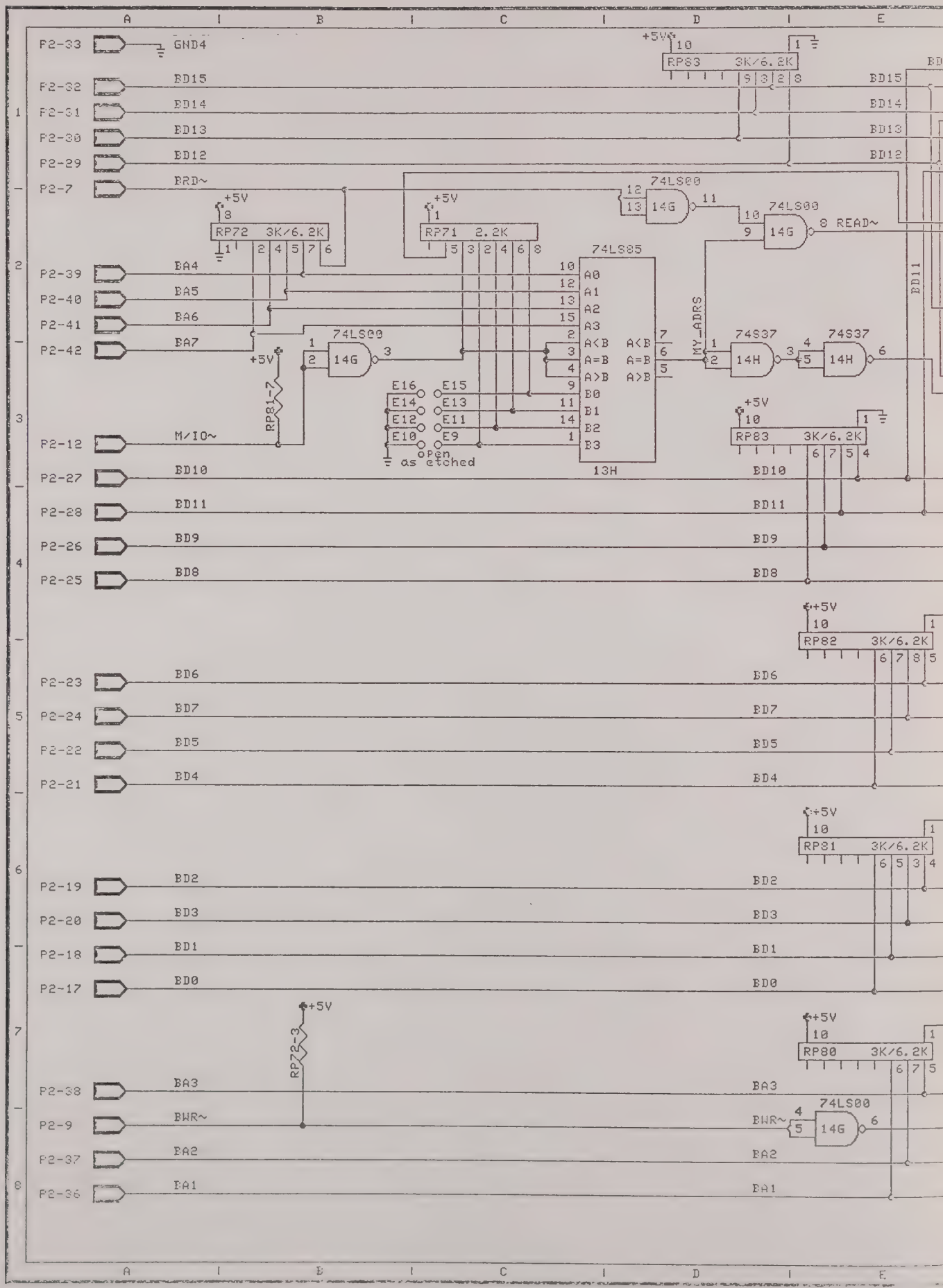


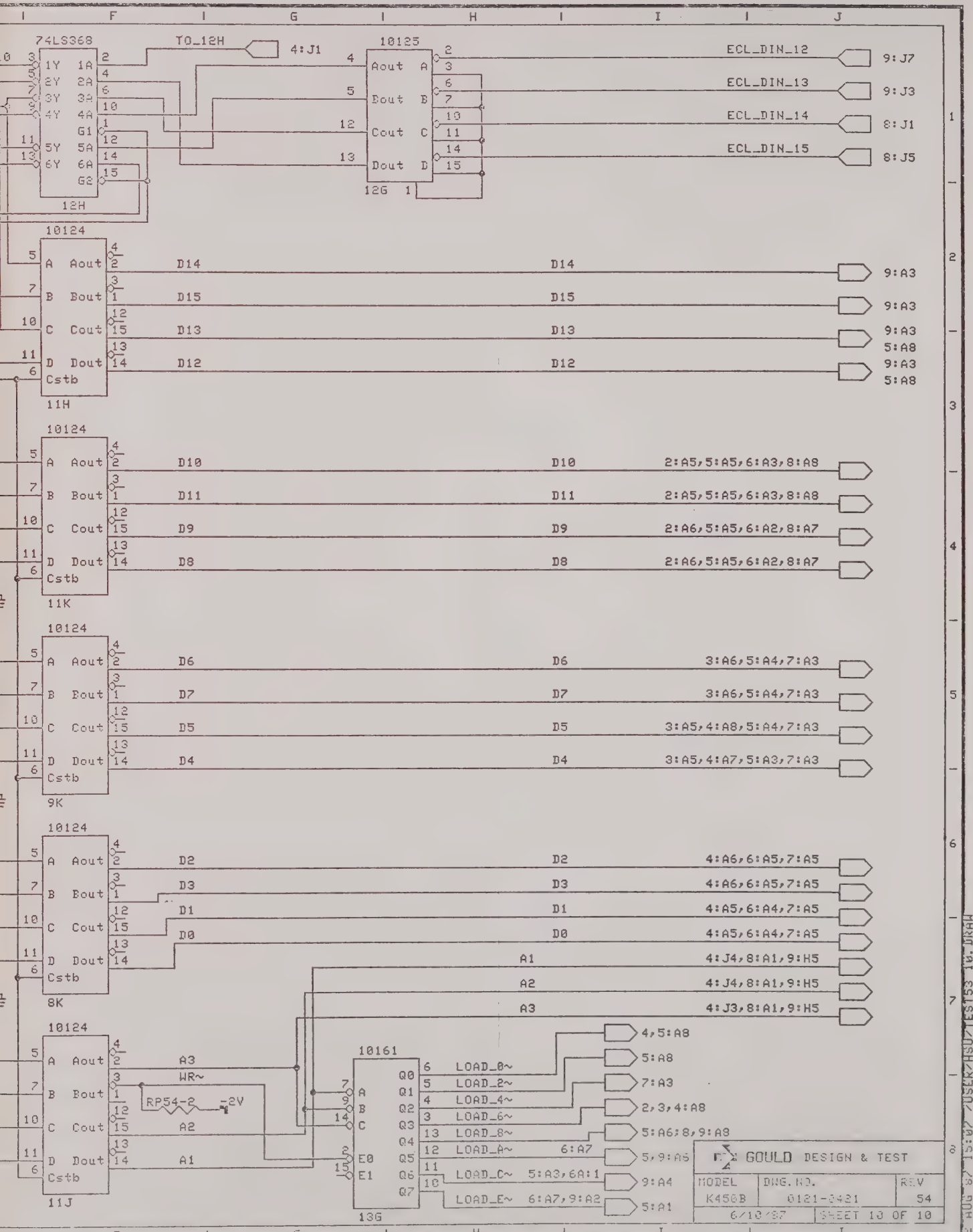
10164
12C
ECL_DIN_14
TRACE
STOP
JUMP
ADVANCE
D=1_IF_A~
D=1_IF_J~
E_L
E_M
RP12-9
-2V
D=1_IF_A~ RP7-8
D=1_IF_J~ RP7-5
100155
12B
EVENT~
ADVANCE~
JUMP
CLK_155~
RP12-10
RP12-2
RP12-3
RP13-4
EVENTED~
EVENTED
ADANCED~
ADVANCED
JUMPED
JUMPED~
RP26-6
100102
11C
DELAY_PE~
NOTE: SEE 9:B8 9:A8
ARMED*~
100155
14B
ADVANCE
TRACE
STOP
RP13-10
RP13-3
RP13-2
RP13-9
E_L
RP52-9
RP19-6
RP52-2
RP52-3
RP19-8
ADVANCED.ENDED~
4:J3
10103
11A
TRACED
100102
11F
7:A1
STOPPED~
R8
680
-5.2V
TRACED_EN
P1-55
RP52-3
100102
ADVANCED.ENDED
STOPPED
ARMED~
MEM.ARMED_C
P1-54
to H5
10145
13A
LEVEL_0E
LEVEL_1E
LEVEL_2E
LEVEL_3E
D8
D9
D10
D11
LOAD_8~
CLK_10016
CYCLE_RESET
CYCLE_RESET*
10176
12A
RP7-3
RP7-6
RP7-7
D=1_IF_JUMPED~
D=1_IF_ADVANCED~
OLD_T>D~
OLD_T=D~
OLD_T_<D~
OLD_CYCLE_RESET
RP6-6
RP6-5
RP13-6
RP26-3

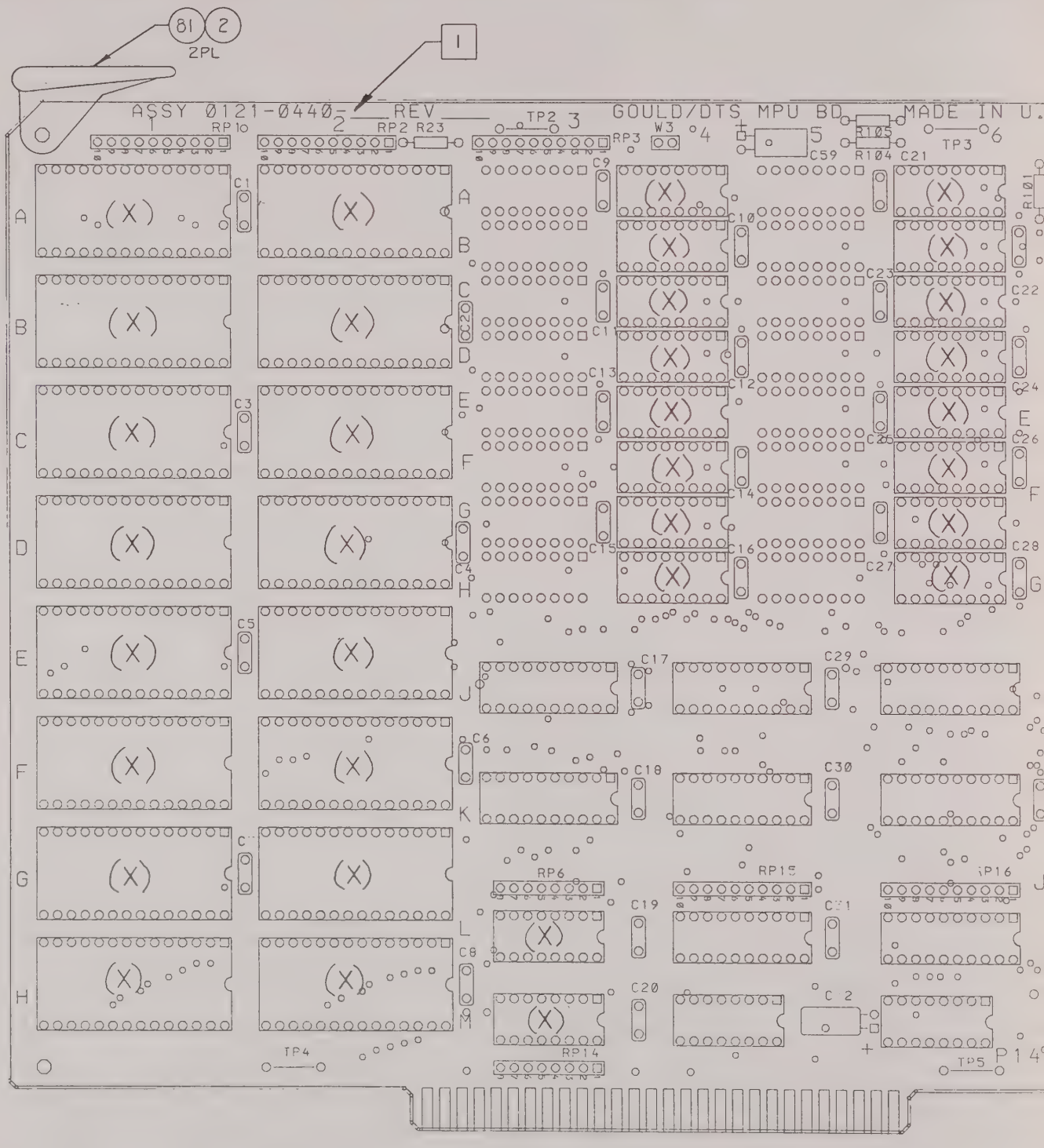

RP27-2 -2V
RP36-9 -2V
ECL_DIN_14
10:J1
DELAY_CE~
9:A8
9:J1
DELAY_TC~
RP39-7 -2V
ADVANCED+JUMPED
9:E8
(OLD_T<D).(ADVANCED+JUMPED).EVENTED.TC
OLD_T_<D~
100101
11D
100102
11C
RP10-3
RP10-2
RP10-5
RP10-4
RP52-10
RP53-3 -2V
T=D
T=D~
5:A6,6:A5
9B
D=1_IF_JUMPED~
(JUMPED).(D=1_IF_JUMPED)
T<D~
<D
JUMPED
(ADVANCED).(D=1_IF_ADVANCED).(JUMPED)~
RP53-4 -2V
RP53-5
T>D
T>D~
11F
RP39-9 -2V
(OLD_T=D).(EVENTED)~.(ADVANCED+JUMPED)~
(OLD_T=D).(EVENTED).(ADVANCED+JUMPED)~
RP13-5 -2V
** >=2 inches
ARMED~
7:A7
RP53-7 -2V
10164
A1
A2
A3
ARMED~
from A1
LEVEL_0E
LEVEL_1E
LEVEL_2E
LEVEL_3E
from B6
ECL_DIN_15
10:J1
RP53-2 -2V
12F
(OLD_T>D).(ADVANCED+JUMPED)~
VBB
(1)
(ARMED+TRACED)~
ARMED
R7
680
7:A1
-5.2V
13K
10125
P1-59
** GATE~ ** to
8253 timer, on
THRES/GPIB BD.
RP52-6 -2V
+5V
R3
180
R2
20
R4
330
2N3906
Q1
R5
51
P1-53
P1-56
P1-60
P2-96
TRIG_OUT
to rear Panel SNC
P2-95
RP11-4
RP11-9
RP36-10
T>D~
T<D~
T=D~
GOULD DESIGN & TEST
MODEL
K4500
DWG. NO.
0121-0431
REV
54
6/10/87
SHEET 8 OF 10
13 AUG 87 08:12 /USER/HSU/TESTS3 8.DRAW


10145
14C
14D
14E
14F
10H016
13C
13D
13E
13F
-2V
RP14-6
RP14-8
RP14-10
RP14-9
RP14-4
RP14-3
RP14-7
RP14-5
RP28-7
RP28-8
RP28-2
RP28-5
RP42-7
RP42-8
RP42-2
RP42-6
RP44-7
RP44-8
RP44-2
RP41-6
RP54-7
RP54-8
RP54-6
RP54-5
A0
A1
A2
A3
D0
D1
D2
D3
CS
WE
Q0
Q1
Q2
Q3
P0
P1
P2
P3
PE
TC
CE
MR
CLK
10:I8 LOAD_E~
10:J3 D12
10:J3 D13
10:J2 D14
10:J2 D15
10:I8 LOAD_C~
10:I8 LOAD_A~
7:I4 LEVEL_0E~
7:I3 LEVEL_1E~
7:I2 LEVEL_2E~
7:I2 LEVEL_3E~
10:I8 LOAD_8~
7:F7 CLK_10016
8:J1 DELAY_CE~
8:E4 DELAY_PE~
(MINIMUM TRACE LENGTH = 8 INCHES FROM 11C8 TO FIRST 10H016)
8:J1


RP36-8 -2V
100101
17
19
20
21
22
11D
8
9
DELAY_TC~
8:F1
RP39-2 -2V
RP11-2 -2V
10164
7 A
9 B
10 C
6 X0
5 X1
4 X2
3 X3
11 X4
12 X5
13 X6
14 X7
2 EN
Z 15
ECL_DIN_13
10:J1
RP40-2 -2V
12D
22 100102
23
(19)
11B
5
4
10:J7 A1
10:J7 A2
10:J7 A3
RP41-2 -2V
24 100102
1
(19)
11B
2
3
16 100102
17
(19)
11C
10
11
ECL_DIN_12
RP43-2 -2V
12E
ADVANCED+JUMPED
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0421
REV 54
6/10/87
SHEET 9 OF 10
12 AUG 87 15:31 /USER/HSU/TEST53 9.DRAW


P2-33
GND4
P2-32
BD15
P2-31
BD14
P2-30
BD13
P2-29
BD12
P2-7
BRD~
P2-39
BA4
P2-40
BA5
P2-41
BA6
P2-42
BA7
P2-12
M/IO~
P2-27
BD10
P2-28
BD11
P2-26
BD9
P2-25
BD8
P2-23
BD6
P2-24
BD7
P2-22
BD5
P2-21
BD4
P2-19
BD2
P2-20
BD3
P2-18
BD1
P2-17
BD0
P2-38
BA3
P2-9
BWR~
P2-37
BA2
P2-36
BA1
+5V
RP83 3K/6.2K
RP72 3K/6.2K
RP71 2.2K
RP82 3K/6.2K
RP81 3K/6.2K
RP80 3K/6.2K
RP81-7
RP72-3
74LS00
14G
74LS85
13H
A0
A1
A2
A3
A<B
A=B
A>B
B0
B1
B2
B3
74S37
14H
MY_ADRS
8 READ~
E16
E15
E14
E13
E12
E11
E10
E9
open
as etched


74LS368
12H
TO_12H
4:J1
10125
12G
ECL_DIN_12
9:J7
ECL_DIN_13
9:J3
ECL_DIN_14
8:J1
ECL_DIN_15
8:J5
10124
11H
D14
D15
D13
D12
9:A3
5:A8
11K
D10
D11
D9
D8
2:A5,5:A5,6:A3,8:A8
2:A6,5:A5,6:A2,8:A7
9K
D6
D7
D5
D4
3:A6,5:A4,7:A3
3:A5,4:A8,5:A4,7:A3
3:A5,4:A7,5:A3,7:A3
8K
D2
D3
D1
D0
4:A6,6:A5,7:A5
4:A5,6:A4,7:A5
A1
A2
A3
4:J4,8:A1,9:H5
4:J3,8:A1,9:H5
11J
WR~
RP54-2
-2V
10161
13G
LOAD_0~
LOAD_2~
LOAD_4~
LOAD_6~
LOAD_8~
LOAD_A~
LOAD_C~
LOAD_E~
4,5:A8
5:A8
7:A3
2,3,4:A8
5:A6;8,9:A8
6:A7
5,9:A5
5:A3,6A:1
9:A4
6:A7,9:A2
5:A1
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0421
REV 54
6/10/87
SHEET 10 OF 10
12 AUG 87 15:07 /USER/HSU/TEST53 10.DRAW



4 REWORK INSTRUCTIONS: ON SOLDER SIDE, ADD JUMPER WIRES;
FROM: 12J-8 TO 12J-11
8B-17 TO RP5-2
11D-14 TO RP5-3

3 RESISTORS NOT TO BE LOADED INTO R7 & R8 LOCATIONS

2. (X) INDICATES SOCKET LOCATIONS. - REF ONLY

1 MARK ASSY DASH NO. AND REV. LEVEL APPROX. WHERE SHOWN USING CONTRASTING INDELIBLE INK.

5 DETAIL OF Y1 FOR -10,-20 DO NOT S
GROUND STRAP TO THE CASE OF THE

INSULATE THE CRYSTAL FROM
TRACES WITH MYLAR TAPE.

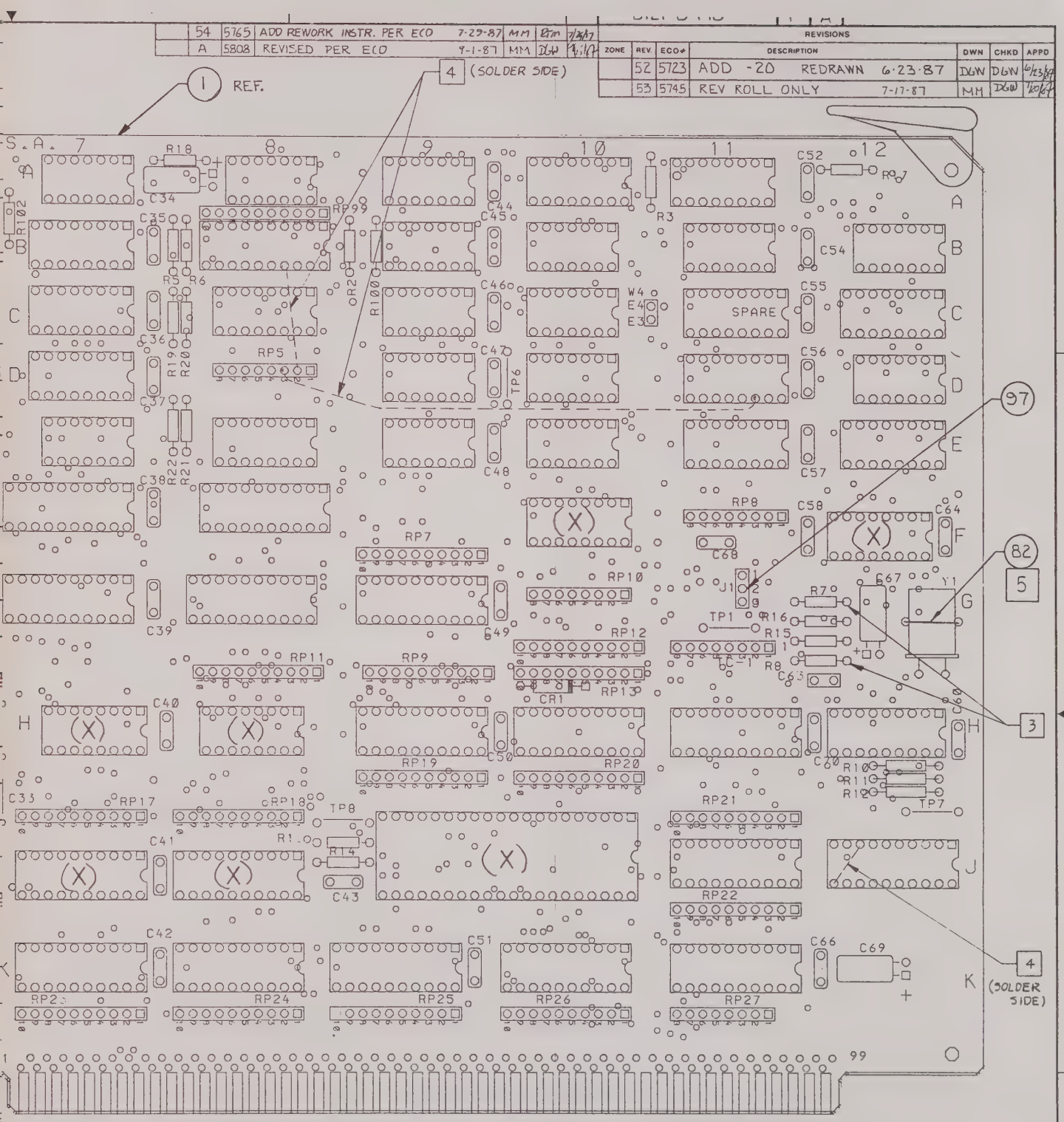
NOTES: (UNLESS OTHERWISE SPECIFIED)

DIETERICH POST REORDER NO 87993

54	5765	ADD REWORK INSTR. PER ECO	7-29-87	MM	
A	5808	REVISED PER ECO	9-1-87	MM	DGW

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	52	5723	ADD -20 REDRAWN 6-23-87	DGW	DGW	
	53	5745	REV ROLL ONLY 7-17-87	MM	DGW	



(97) REF. JUMPER AT SHORTING PLUG J1	-10	-20	CRT. VERT SCAN RATE SELECT
J1-1 TO J1-2	—	—	50Hz
J1-2 TO J1-3	YES	YES	60Hz

OLDER
CRYSTAL.
THE

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO.	NEXT ASSY	USED ON
-20	D1231-XXX	D1231
-10	K450B-XXX	K450 B

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE.
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN DGWRIGHT	6/23/87
CHECKED DGW	6/23/87
PROJ ENG	

GOULD Electronics

TITLE: ASSY PCB MPU (K450B) (D1231)

SIZE D | DWG. NO. 0121-0440 | REV A

SCALE 2:1 | MODEL | SHEET 1 OF 1

BILL OF MATERIAL

AS OF 10/30/87

0121-0440-10 ASSY,PCB,MPU,K450B
MODEL K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0441	SCHEM, PCB,MPU,K450B	0	EA	
0	D0121-0440	DWG,ASSY,PCB,MPU,K450B	0	EA	
1	0121-0442-10	FAB,PCB,MPU,K450B	1	EA	
2	7000-0120-10	CARD EJECTOR NYLON 6/6	2	EA	
3	8300-0002-10	TAPE,MYLAR,4500	0	FT	@Y1
11	0121-0050-10	SPEC,PROM,512X4,K450 MAP	1	EA	10F
12	0121-0055-10	SPEC,PROM,256X4 ROM SELEC (HI)	1	EA	3L
13	0121-0060-10	SPEC,PROM 256X4 ROM SELEC (LO)	1	EA	3M
15	1800-0321-10	IC D8086 16 BIT HMOS	1	EA	10J
18	0121-0665-10	ASSY,PROM,I/O WAIT STATE	1	EA	12F
19	1800-0327-10	IC D8284 CLK GEN & DR	1	EA	12H
20	1800-0581-10	IC DRAM 256KX1	16	EA	4A,4B,4C 4D,4E,4F 4G,4H,6A 6B,6C,6D 6E,6F,6G 6H
21	0100-0120-10	SKT 16 PIN DIP LO-PROFIL	20	EA	X10F,X12F X3L,X3M, X4A-X4H, X6A-X6H,
22	1800-0094-10	IC 74S175N QUAD D F/F	1	EA	12C
23	1400-0019-10	TRAN 2N3906	1	EA	Q1
24	1800-0122-10	IC 74LS192N UP/DWN CNTR	1	EA	12E
25	1800-0031-10	IC 74S00N 14 NAND X4	3	EA	10C,12B,9B
26	1800-0038-10	IC 74S20N 14 NAND X2	1	EA	9C
27	1800-0039-10	IC 74S112N DUAL J-K F/F	4	EA	10A,11A, 11D,11E
28	1800-0060-10	IC 74S10N 14 NAND X3	4	EA	12D 7A 8A 9D
29	1800-0092-10	IC 74S04N, 14, INV, X6	1	EA	10E 10E
30	1800-0107-10	IC 74LS04N HEX INV	1	EA	9E
31	1800-0125-10	IC 74LS161N 20CNTR, SYN, BIN	4	EA	7C,7D,8C 8E
32	1800-0133-10	IC 74S11N 3-INPUT AND G	1	EA	10B
33	1800-0136-10	IC 74S51N DUAL 2-WIDE	1	EA	10D
34	1800-0208-10	IC 74S161N 4BIT BIN CNTR	1	EA	7B
35	1800-0240-10	IC 74LS244N,20,BUFF,TRI-ST	9	EA	3J,3K,4J 6J,7F,7G 8F,8G,9G
36	1800-0243-10	IC 74S08N 14 AND X4	2	EA	11B,9A
37	1800-0268-10	IC 74LS245N BUS TRANS	2	EA	7K,8K
38	1800-0298-10	IC 74LS373N OCTAL D TYP	10	EA	10H,10K 11J,11K

BILL OF MATERIAL
AS OF 10/30/87

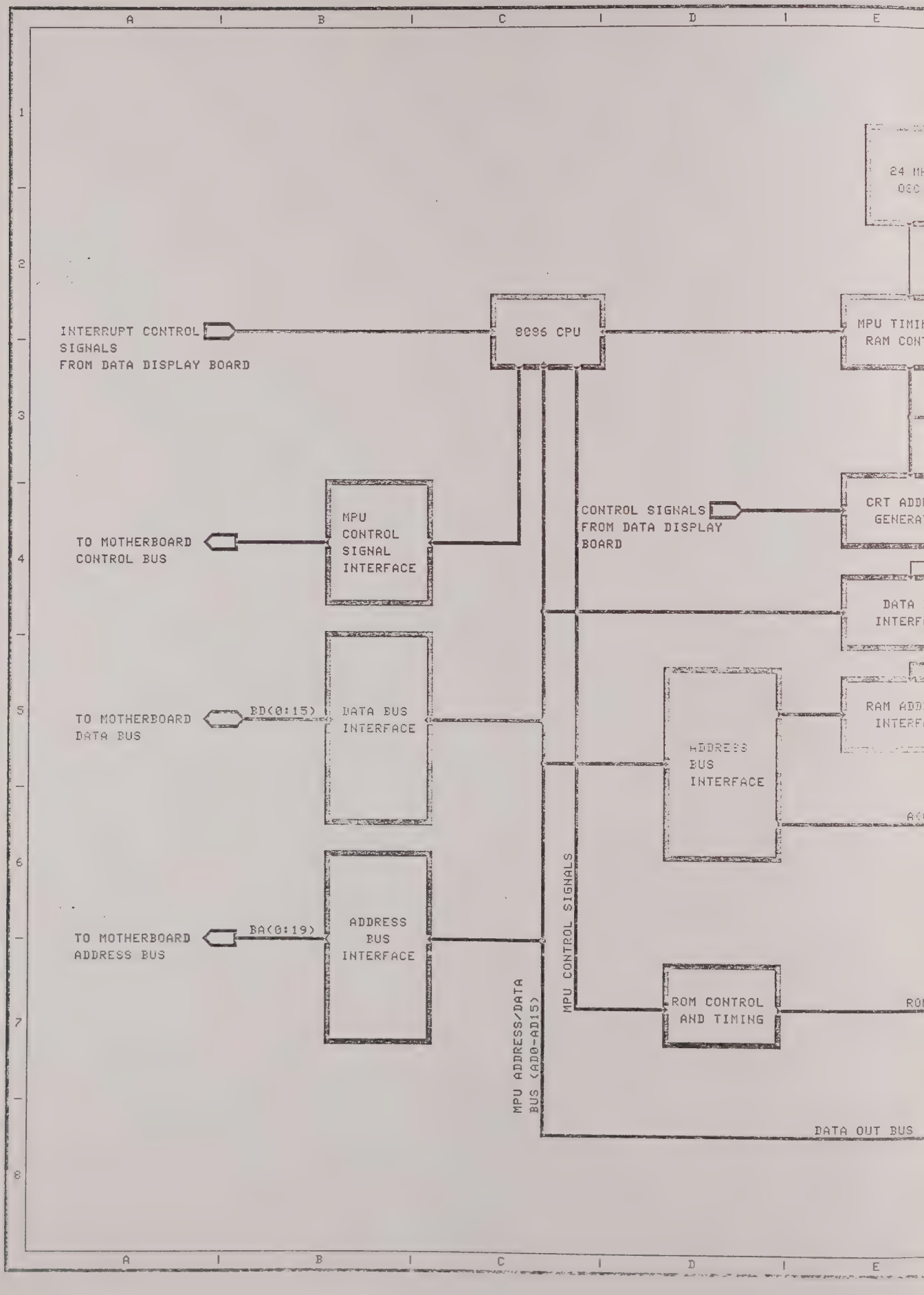
0121-0440-10 ASSY,PCB,MPU,K450B
MODEL: K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
38	1800-0298-10	IC 74LS373N OCTAL D TYP	10	EA	4K,4L,6K 6L,9H,9K
40	1800-0335-10	IC 74LS166N 8-BIT SHIFT	2	EA	4M,6M
42	1800-0261-10	IC 74S240N 20 BFR,INV,X8	3	EA	8B,11H,12J
43	2100-0009-10	IND 1025-24 FERRITE CORE	1	EA	L1
46	3000-1000-10	RES,100,5%,1/4W,C	1	EA	R11
46	3000-5600-10	RES,560,5%,1/4W,C	2	EA	R10,11
47	3000-1300-10	RES,130,5%,1/4W,C	1	EA	R9
47	3000-2400-10	RES,240,5%,1/4W,C	1	EA	R9
48	3000-1601-10	RES,1.6K,5%,1/4W,C	1	EA	R6 R6,R10
50	3000-2200-10	RES,220,5%,1/4W,C	4	EA	R104 R7,R19,R21
51	3000-2201-10	RES,2.2K,5%,1/4W,C	8	EA	R10 R15,R17 R18,R23 R2,R3,R5,
52	3000-2700-10	RES,270,5%,1/4W,C	1	EA	R13
53	3000-3300-10	RES,330,5%,1/4W,C	3	EA	R105 R105 R8,20,22 R8,20,22
54	3000-3301-10	RES,3.3K,5%,1/4W,C	1	EA	R12
55	3000-5100-10	RES,510,5%,1/4W,C	3	EA	R12 R16,R11,
56	3000-9106-10	RES,91,5%,1/4W,C	1	EA	R14
57	3700-0049-10	RPAK,3K/6.2K,1/8W,5%,10/16	16	EA	RP1,2,7,9 RP11,12,13 RP15,16,17 RP18,22,23 RP24,25,26
58	3700-0057-10	RPAK,2.2K,0.18W,2%,8/7	6	EA	RP14,27 RP5,6,8,10
59	3700-0065-10	RPAK,220/330,1/8W,5%,10/16	5	EA	RP11,12,13 RP3 RP3
60	3700-0066-10	RPAK,10K,0.18W,2%,10/9	3	EA	RP19,20,21
62	4000-0044-10	CAP,0.01UF,100V,20%,CER	1	EA	C68
63	4000-0040-10	CAP,470PF,50V,10%,CER	1	EA	C43
64	4000-0025-10	CAP,0.1UF,50V,20%,CER	59	EA	C1-31,C33 C35-42, C44-52, C54-58,C60 C63,64,66 C70
64	4000-0044-10	CAP,0.01UF,100V,20%,CER	61	EA	C1-31,C33

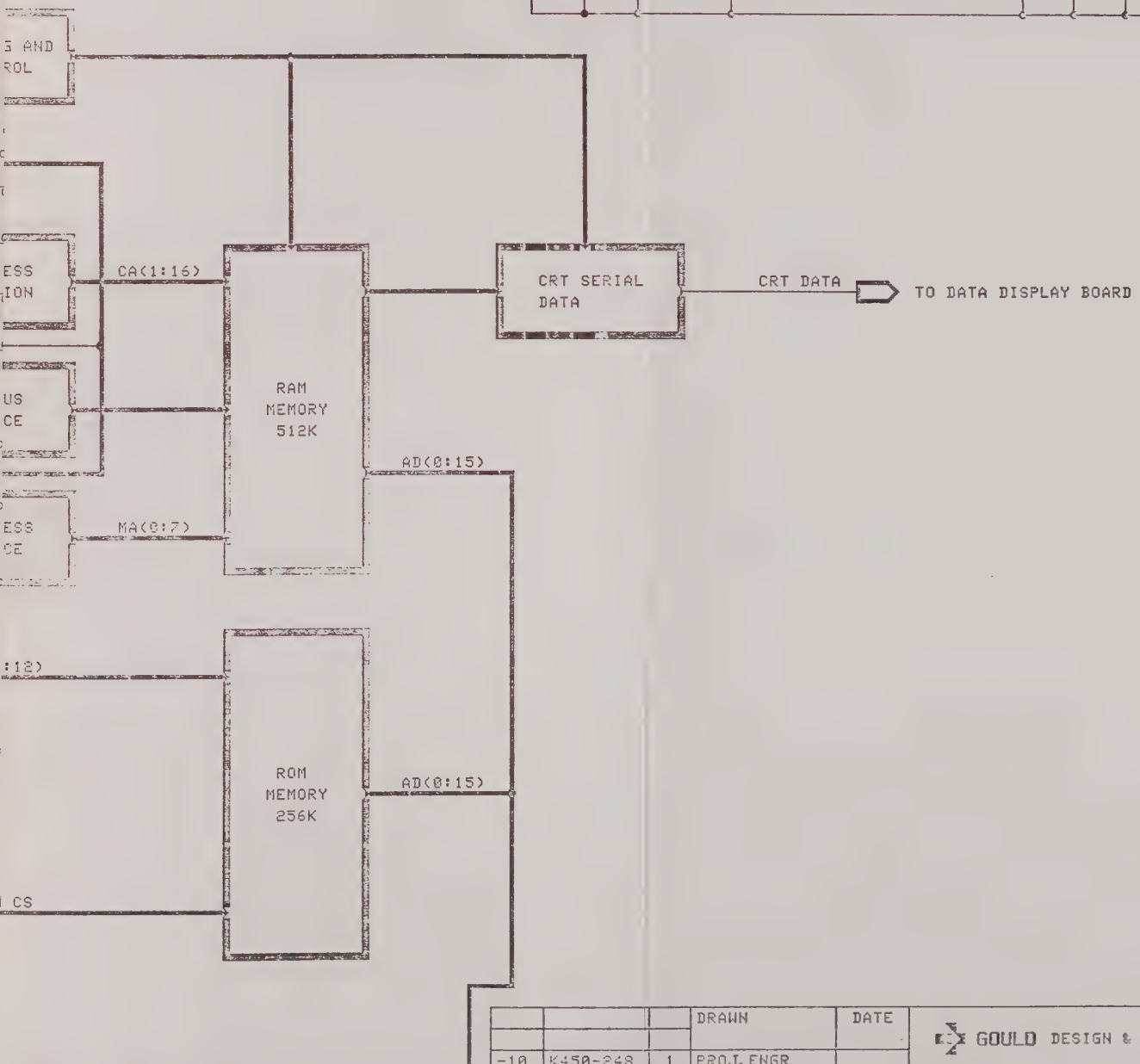
BILL OF MATERIAL
AS OF 10/30/87

0121-0440-10 ASSY,PCB,MPU,K450B
MODEL. K450

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
64	4000-0044-10	CAP,0.01UF,100V,20%,CER	59	EA	C1-31,C33 C1-31,C33 C35-42,C68 C35-42,C68 C35-42,C68 C44-52, C44-52, C44-52, C54-58, C54-58, C54-58,60 C61-66 C63,64,66 C63-66
68	4100-0029-10	CAP,30PF,500V,5%,MICA	1	EA	C60
70	4400-0043-10	CAP,47UF,20%,10V,ELCTLT	5	EA	67,69 C32,34,59,
72	5100-0016-10	XTAL 24.0MHZ,.015%	1	EA	Y1
72	5100-0039-10	CRYSTAL,24.00MHZ,FUND,HC80,AT	1	EA	Y1
74	6000-0190-10	CONN 8 PIN HDR ST SGL ROW	1	EA	TC1
78	6100-0123-10	SKT 40 PIN DIP	1	EA	X10J
79	6100-0151-10	SKT 28 PIN DIP LO PROFIL	16	EA	X1A-X1H X2A-X2H
81	7000-0412-10	CARD EJECTOR PIN 3/32X1/4	2	EA	
82	7100-0017-10	WIRE,BUS,22 GA,TINNED	0	FT	
88	0121-0075-10	ASSY,PROM SET,K450 MAIN CODE	1	ST	1A,1B,1C, 1D,1E,2A, 2B,2C,2D, 2E,1F,2F
88	0121-0400-10	ASSY,PROM SET,MAIN CODE,K450B	1	ST	1A,1B,1C, 1D,1E,2A, 1G,2G 2B,2C,2D, 2E,1F,2F
89	3000-3306-10	RES,33,5%,1/4W,C	3	EA	102 R100,101,
90	3700-0139-10	RPAK 33 OHM 10SIP	1	EA	RP99
95	1800-0324-10	IC 74LS125PC QUAD BUS BUF	1	EA	7E
96	6000-0293-03	CONN 3 POS HDR ST SGL ROW	1	EA	J1
97	6000-0571-10	CONN SHORTING PLUG	1	EA	XJ1
98	1000-0003-10	DIO,5082-2811	1	EA	CR1
99	3000-3001-10	RES,3K,5%,1/4W,C	3	EA	R104,R21, R20
100	3000-6201-10	RES,6.2K,5%,1/4W,C	3	EA	R105,R22, R19


A
B
C
D
E
1
2
3
4
5
6
7
8
24 MH
OSC
INTERRUPT CONTROL
SIGNALS
FROM DATA DISPLAY BOARD
8086 CPU
MPU TIMI
RAM CONT
MPU
CONTROL
SIGNAL
INTERFACE
TO MOTHERBOARD
CONTROL BUS
CONTROL SIGNALS
FROM DATA DISPLAY
BOARD
CRT ADD
GENERA
DATA
INTERF
TO MOTHERBOARD
DATA BUS
BD(0:15)
DATA BUS
INTERFACE
ADDRESS
BUS
INTERFACE
RAM ADD
INTERF
A
TO MOTHERBOARD
ADDRESS BUS
BA(0:19)
ADDRESS
BUS
INTERFACE
MPU CONTROL SIGNALS
ROM CONTROL
AND TIMING
RO
MPU ADDRESS/DATA
BUS (AD0-AD15)
DATA OUT BUS

REVISIONS							
ZONE	REV.	ECO#	DESCRIPTION	DRWN	CHKD	APVD	DATE
	50	5609	REVISED PER ECO				
	51	5649	REVISED PER ECO	H.SH			5/87
	52	5683	REVISED PER ECO	M.S.			6/24 1987
	54	5765	REVISED PER ECO	S.M.	DGW		7/23 1987
	A	5808	REVISED PER ECO	S.M.	DGW		9/9 1987



			DRAWN	DATE
-10	K450-248	1	PROJ. ENGR	5-12-86
-10	K450-232	1	R. MENKER	
-10	K450-216	1	MANUFACTURING	
-10	K450-248	1		
	K450-032	1	QUALITY ASSUR	
-10	K450-216	1		
DASH NO.	NUMBER	QTY	ECO NO.	
	NEXT ASSEMBLY			

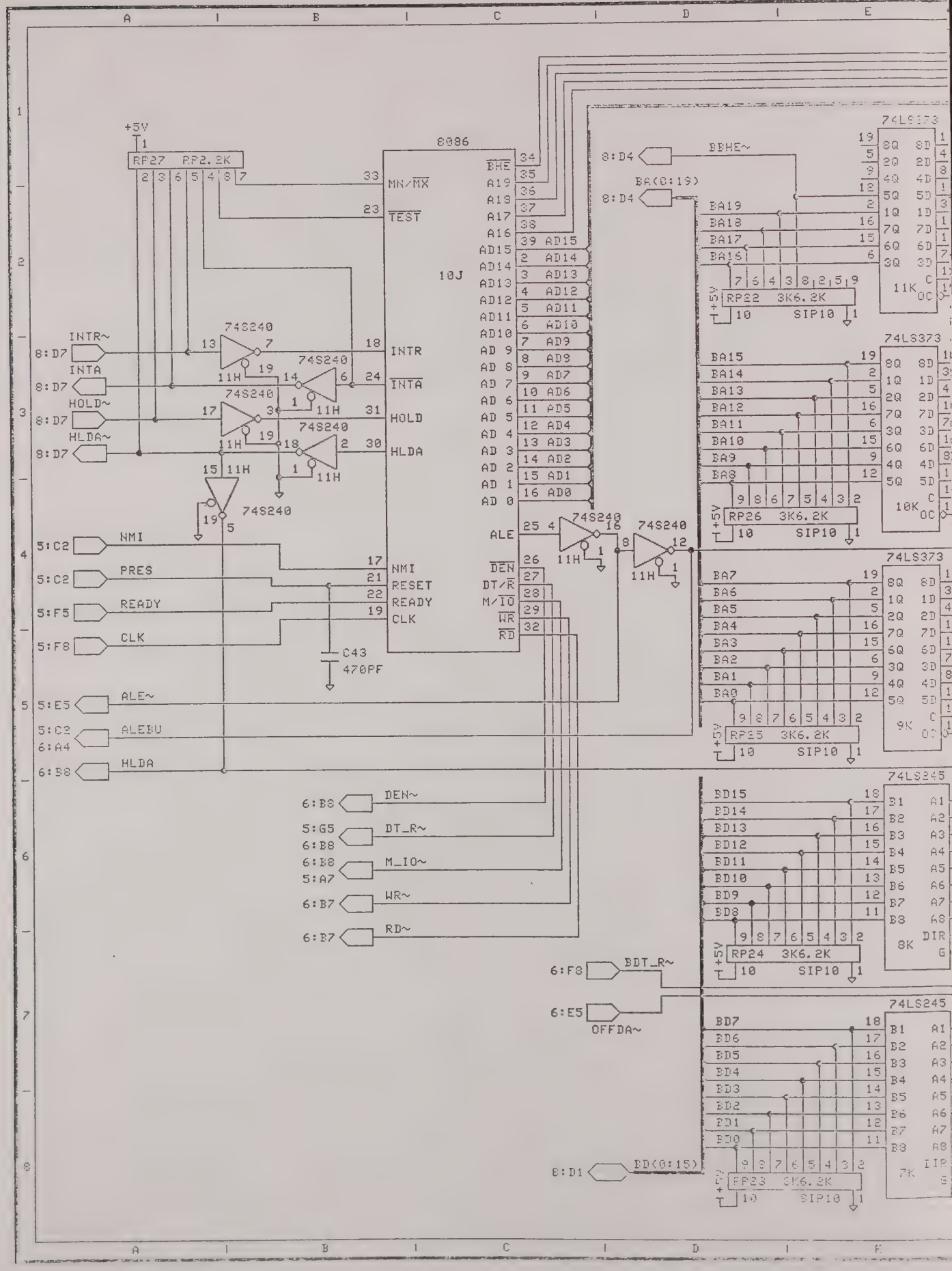
GOULD DESIGN & TEST

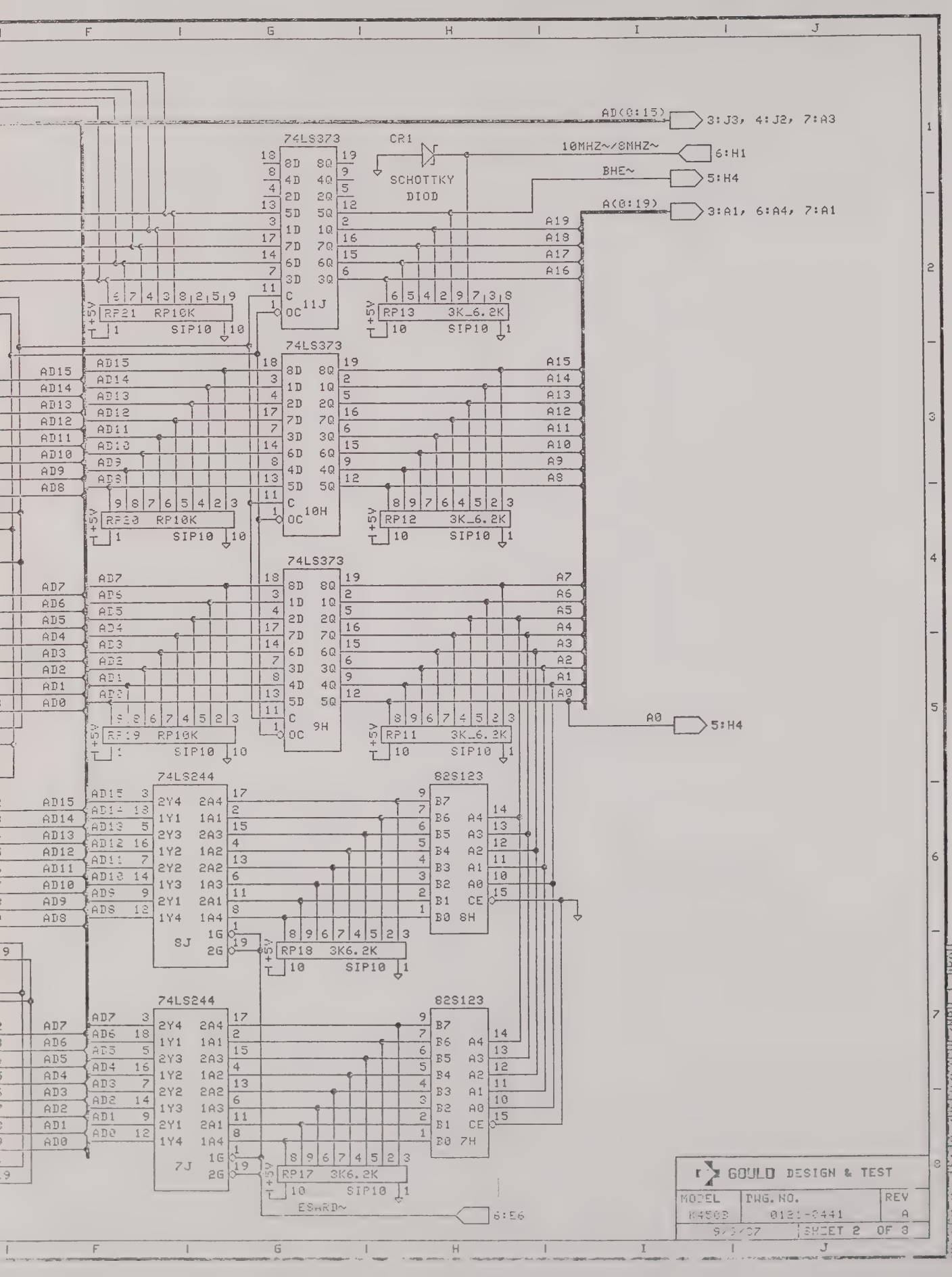
TITLE: SCHEMATIC, MPU BOARD

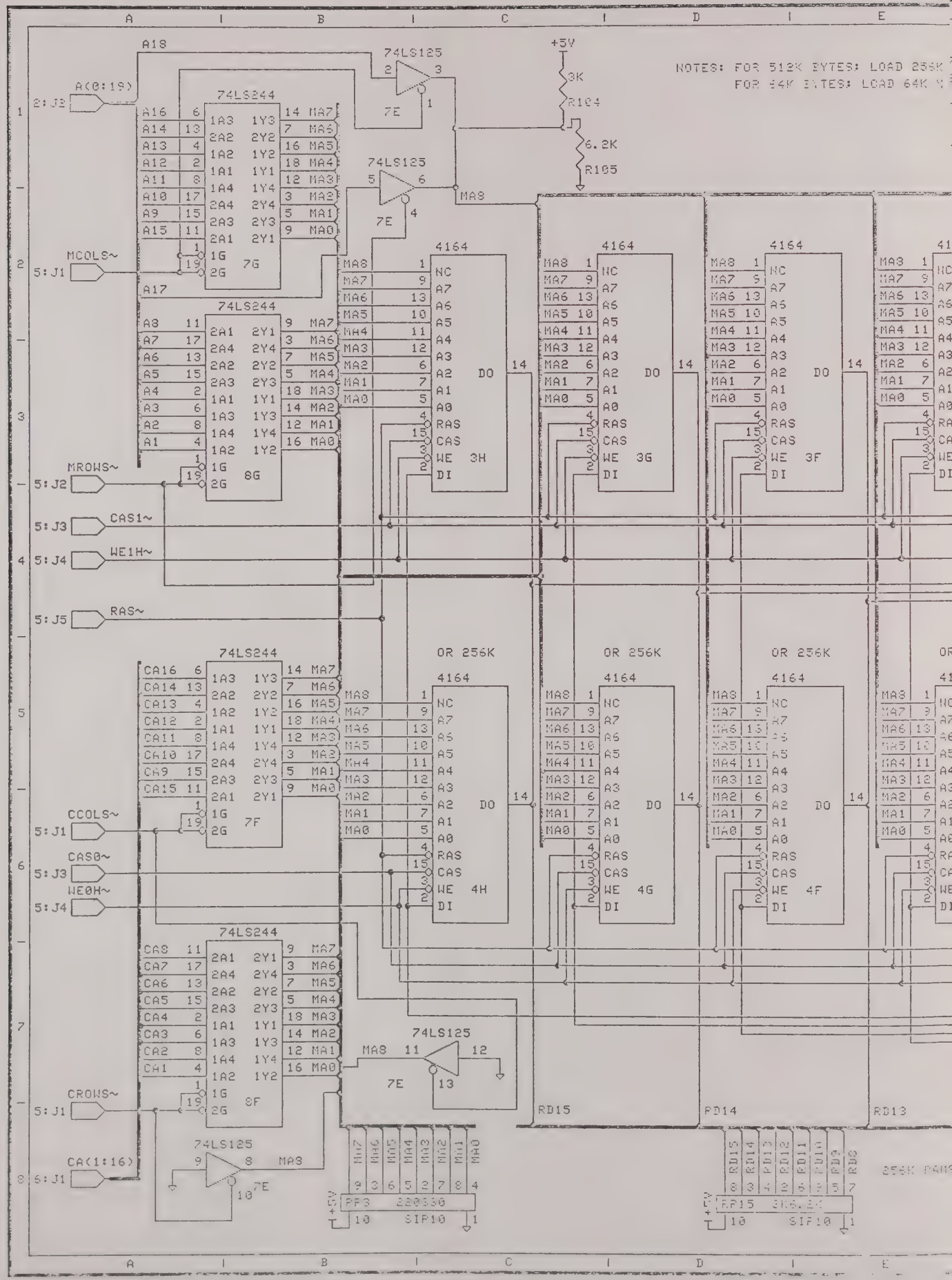
MODEL	PART NUMBER	REV
K4508	0121-0441	54

9/9/87 SHEET 1 OF 8

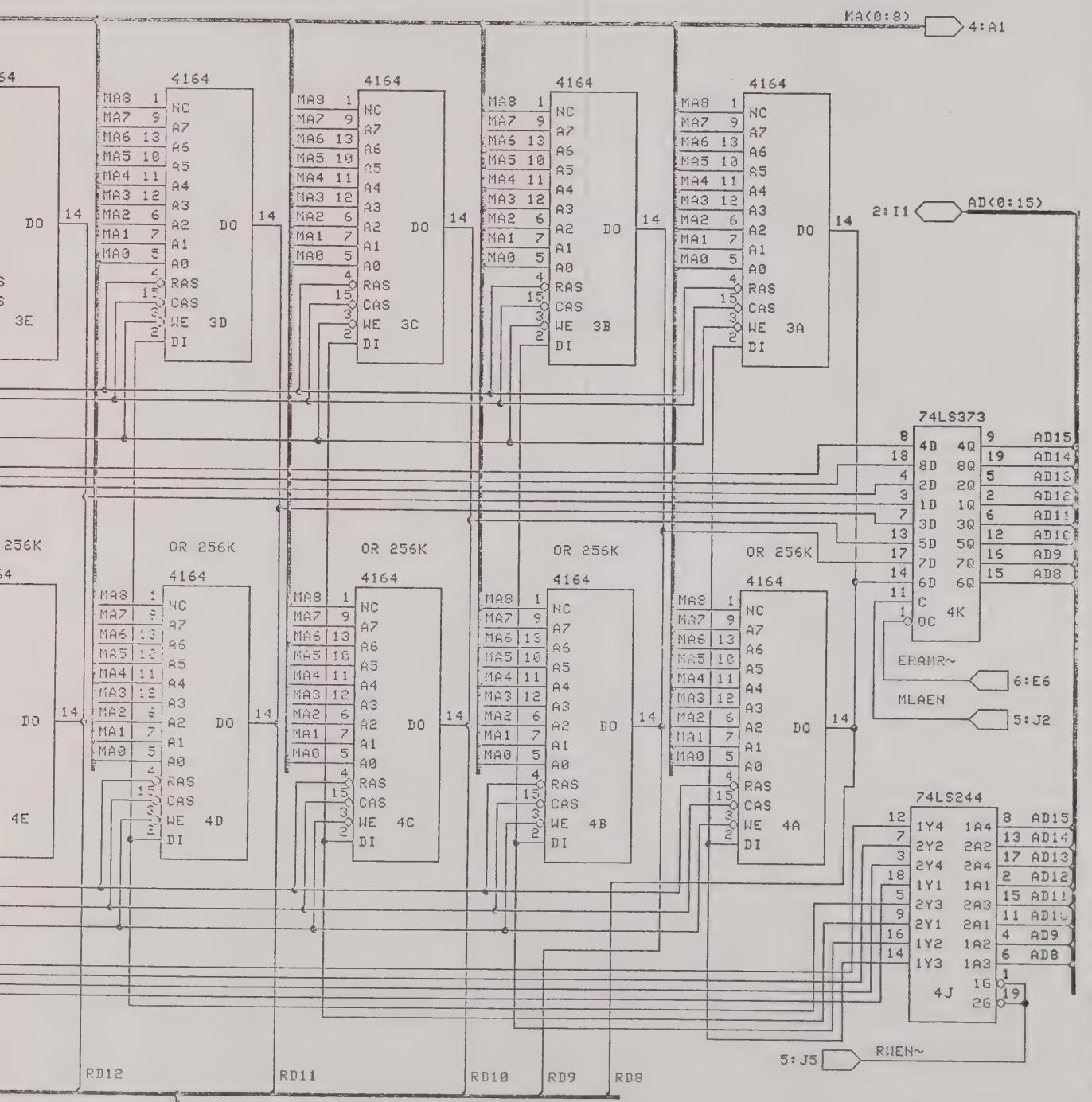
09 SEP 87 15:51 /USER/STEVE/MPU_BLOCK.DRAW


8086
10J
+5V
RP27 RP2.2K
MN/MX
TEST
INTR
INTA
HOLD
HLDA
NMI
RESET
READY
CLK
ALE
DEN
DT/R
M/IO
WR
RD
BHE
A19
A18
A17
A16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
74S240
11H
C43
470PF
INTR~
INTA
HOLD~
HLDA~
8:D7
5:C2
NMI
PRES
5:F5
READY
5:F8
CLK
5:E5
ALE~
5:C2
6:A4
ALEBU
6:B8
HLDA
6:B8
DEN~
5:G5
6:B8
DT_R~
6:B8
5:A7
M_IO~
6:B7
WR~
6:B7
RD~
8:D4
BHE~
BA(0:19)
74LS373
BA19
BA18
BA17
BA16
RP22 3K6.2K
SIP10
11K
BA15
BA14
BA13
BA12
BA11
BA10
BA9
BA8
RP26 3K6.2K
10K
BA7
BA6
BA5
BA4
BA3
BA2
BA1
BA0
RP25 3K6.2K
9K
74LS245
BD15
BD14
BD13
BD12
BD11
BD10
BD9
BD8
RP24 3K6.2K
8K
DIR
6:F8
BDT_R~
6:E5
OFFDA~
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
8:D1
BD(0:15)
RP23 3K6.2K
7K


AD(0:15)
3:J3, 4:J2, 7:A3
74LS373
CR1
SCHOTTKY DIOD
10MHZ~/8MHZ~
6:H1
BHE~
5:H4
A(0:19)
3:A1, 6:A4, 7:A1
A19
A18
A17
A16
RP21 RP10K
RP13 3K_6.2K
SIP10
11J
A15
A14
A13
A12
A11
A10
A9
A8
RP20 RP10K
RP12 3K_6.2K
10H
A7
A6
A5
A4
A3
A2
A1
A0
RP19 RP10K
RP11 3K_6.2K
9H
A0
5:H4
74LS244
82S123
RP18 3K6.2K
8J
RP17 3K6.2K
7J
ESMRD~
6:E6
GOULD DESIGN & TEST
MODEL
DWG. NO.
0121-0441
REV
A
SHEET 2 OF 3


NOTES: FOR 512K BYTES: LOAD 256K
FOR 64K BYTES: LOAD 64K
A18
A(0:19)
2:J2
74LS125
7E
+5V
3K
R104
6.2K
R105
74LS244
7G
MCOLS~
5:J1
A17
74LS244
8G
MROWS~
5:J2
CAS1~
5:J3
WE1H~
5:J4
RAS~
5:J5
4164
3H
3G
3F
4H
4G
4F
OR 256K
74LS244
7F
CCOLS~
5:J1
CAS0~
5:J3
WE0H~
5:J4
74LS244
8F
CROWS~
5:J1
74LS125
7E
CA(1:16)
6:J1
RD15
RD14
RD13
RP3 220/330
RP15 3K6.2K
SIP10

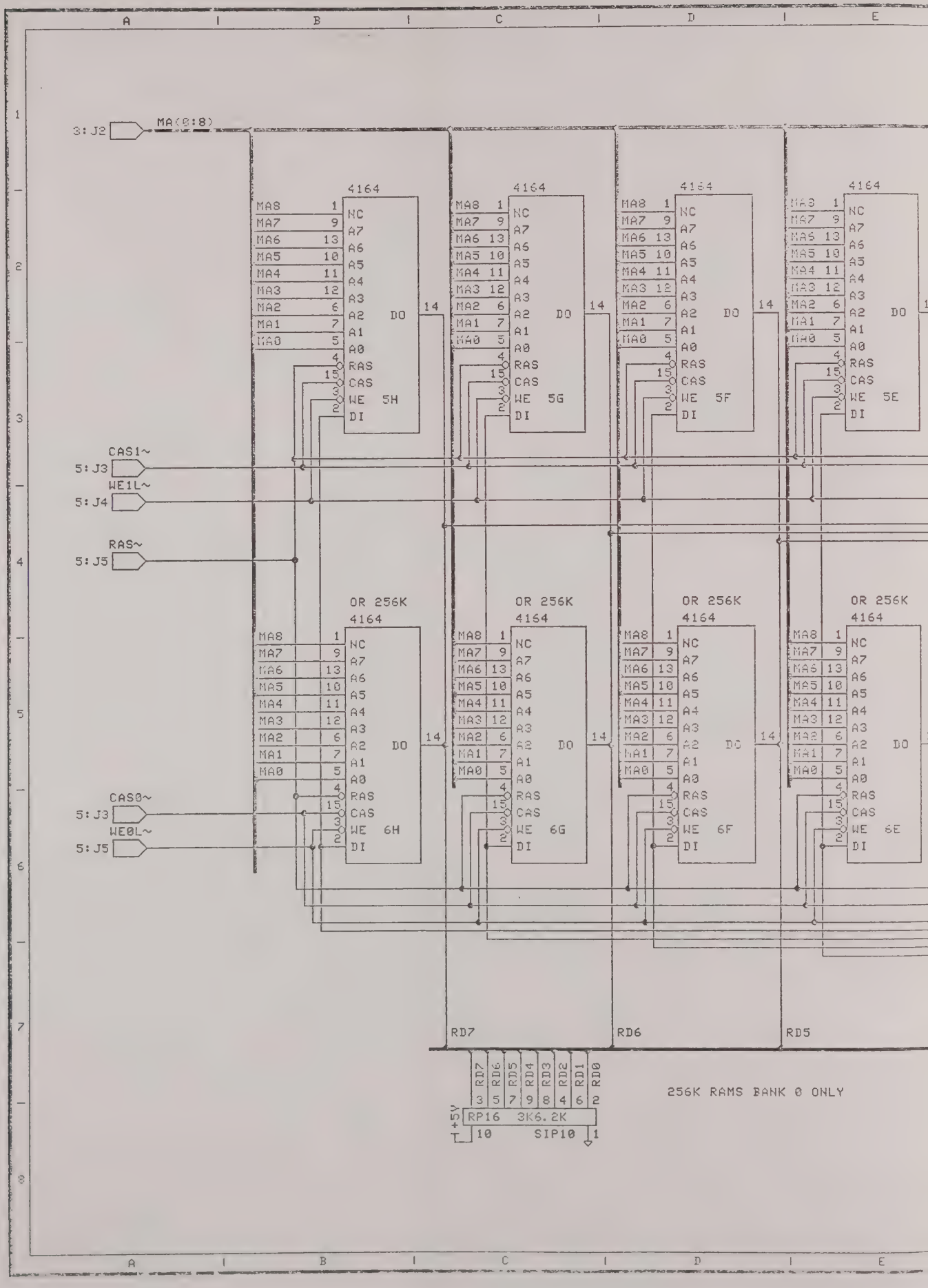
X 1 DRAMS IN LOCATIONS 4A-4H AND 6A-6H.
1 (4164) DRAMS IN LOCATIONS 3A-3H, 4A-4H, 5A-5H, 6A-6H.

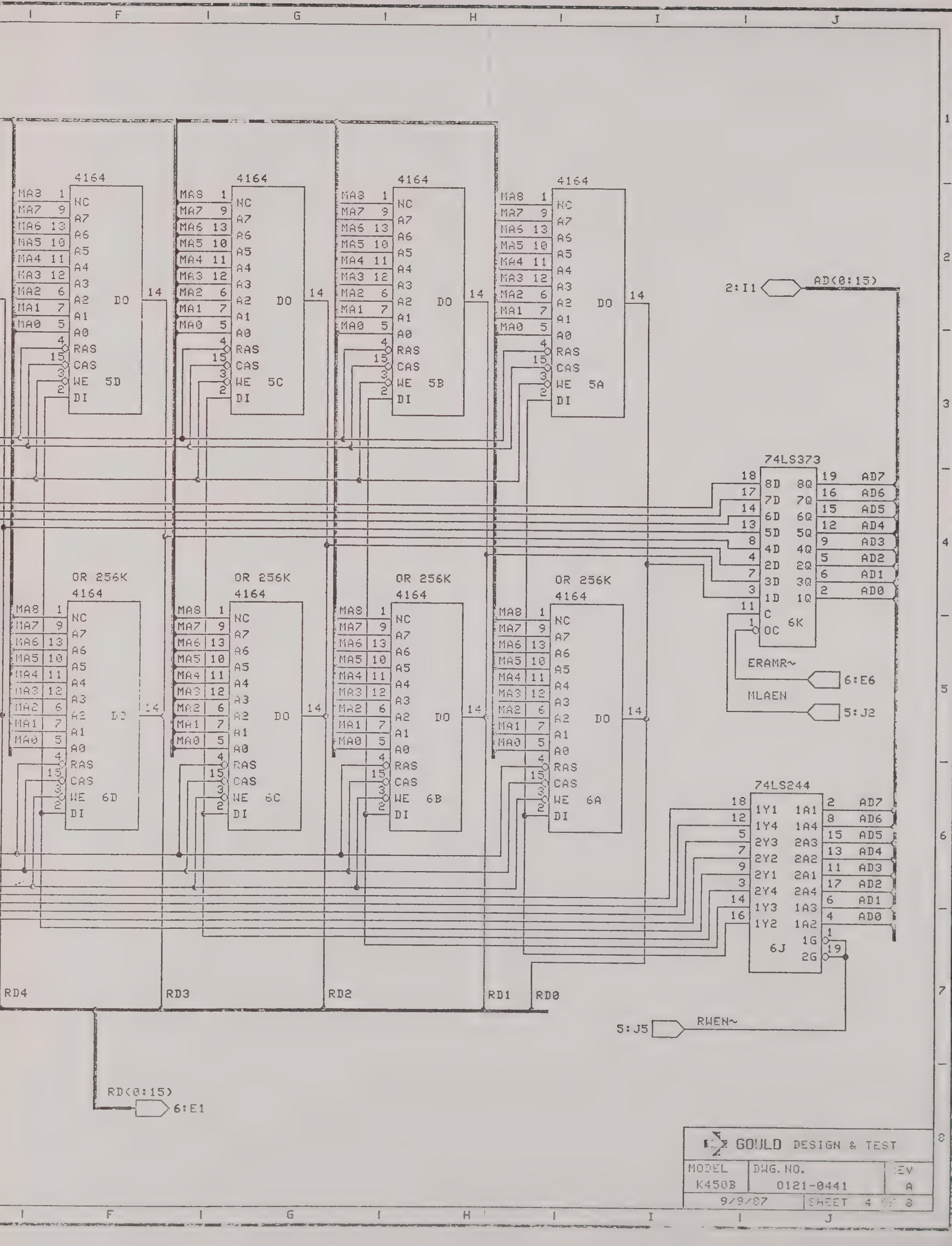


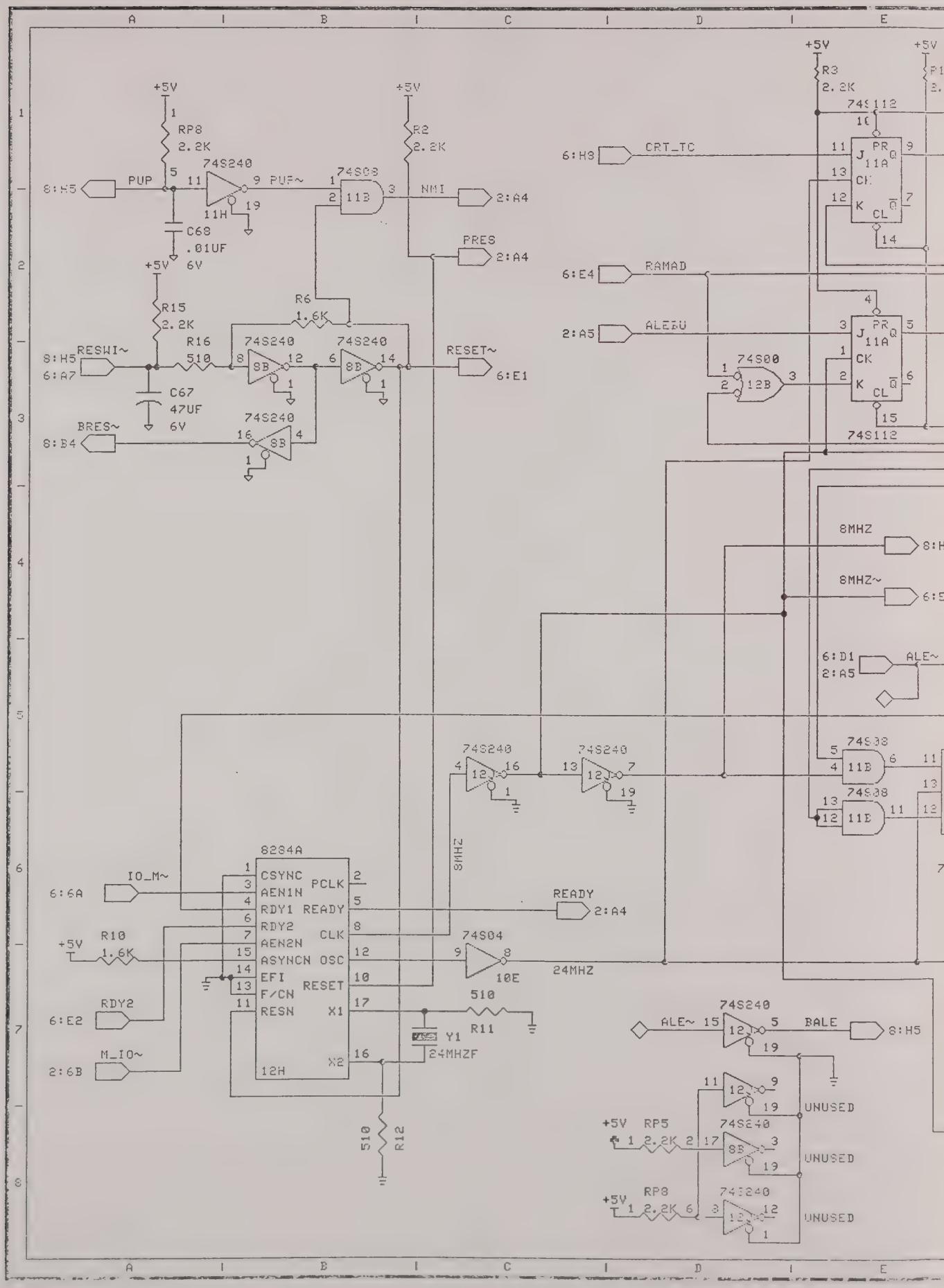
GOULD DESIGN & TEST

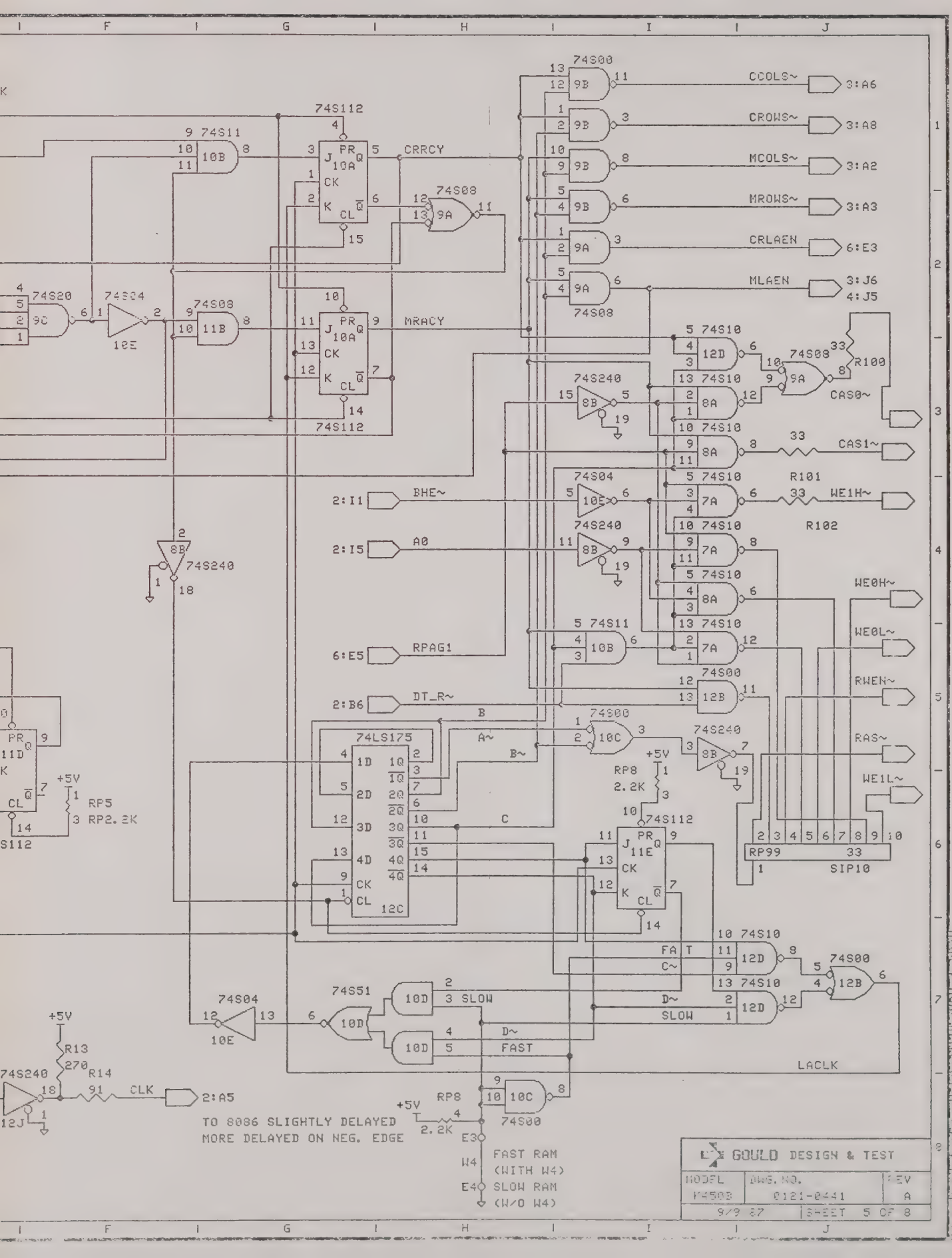
MODEL	DWG. NO.	REV
K455B	0121-0441	A
9/8/87	SHEET 3 OF 8	

09 SEP 87 15:53 /USER/STEVE/MPU 2.DRAW

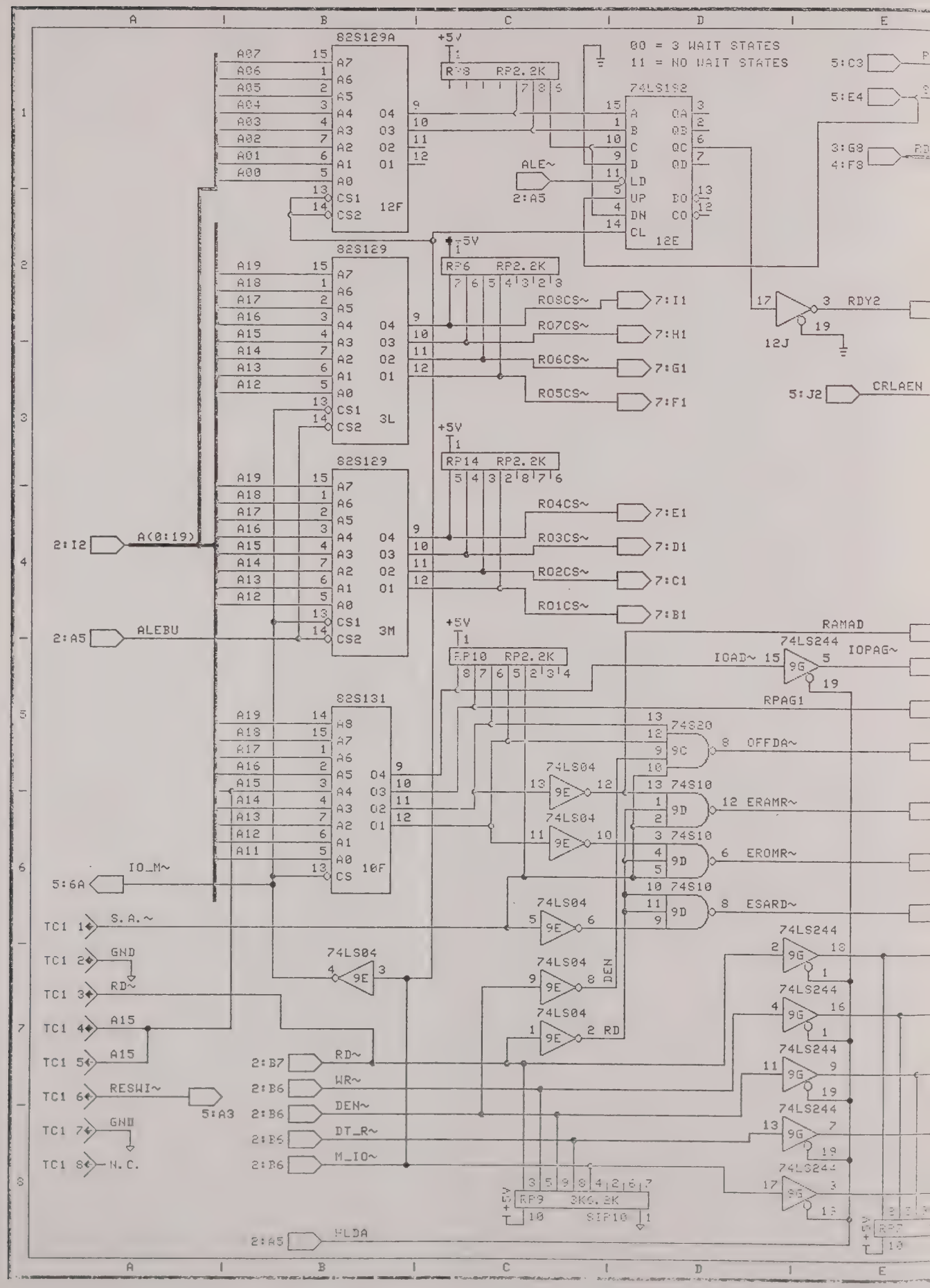

A
B
C
D
E
1
2
3
4
5
6
7
8
3:J2
MA(0:8)
4164
5H
5G
5F
5E
NC
A7
A6
A5
A4
A3
A2
A1
A0
RAS
CAS
WE
DI
DO
MA8
MA7
MA6
MA5
MA4
MA3
MA2
MA1
MA0
CAS1~
5:J3
WE1L~
5:J4
RAS~
5:J5
OR 256K
6H
6G
6F
6E
CAS0~
WE0L~
RD7
RD6
RD5
RD4
RD3
RD2
RD1
RD0
+5V
RP16 3K6.2K
SIP10
256K RAMS BANK 0 ONLY


4164
MA8 1 NC
MA7 9 A7
MA6 13 A6
MA5 10 A5
MA4 11 A4
MA3 12 A3
MA2 6 A2
MA1 7 A1
MA0 5 A0
4 RAS
15 CAS
3 WE
2 DI
DO 14
5D
5C
5B
5A
OR 256K
6D
6C
6B
6A
2:I1
AD(0:15)
74LS373
8D 8Q
7D 7Q
6D 6Q
5D 5Q
4D 4Q
2D 2Q
3D 3Q
1D 1Q
C
OC
6K
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
ERAMR~
6:E6
MLAEN
5:J2
74LS244
1Y1 1A1
1Y4 1A4
2Y3 2A3
2Y2 2A2
2Y1 2A1
2Y4 2A4
1Y3 1A3
1Y2 1A2
1G
2G
6J
RD4
RD3
RD2
RD1
RD0
5:J5
RWEN~
RD(0:15)
6:E1
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0441
REV A
9/9/87
SHEET 4 OF 8

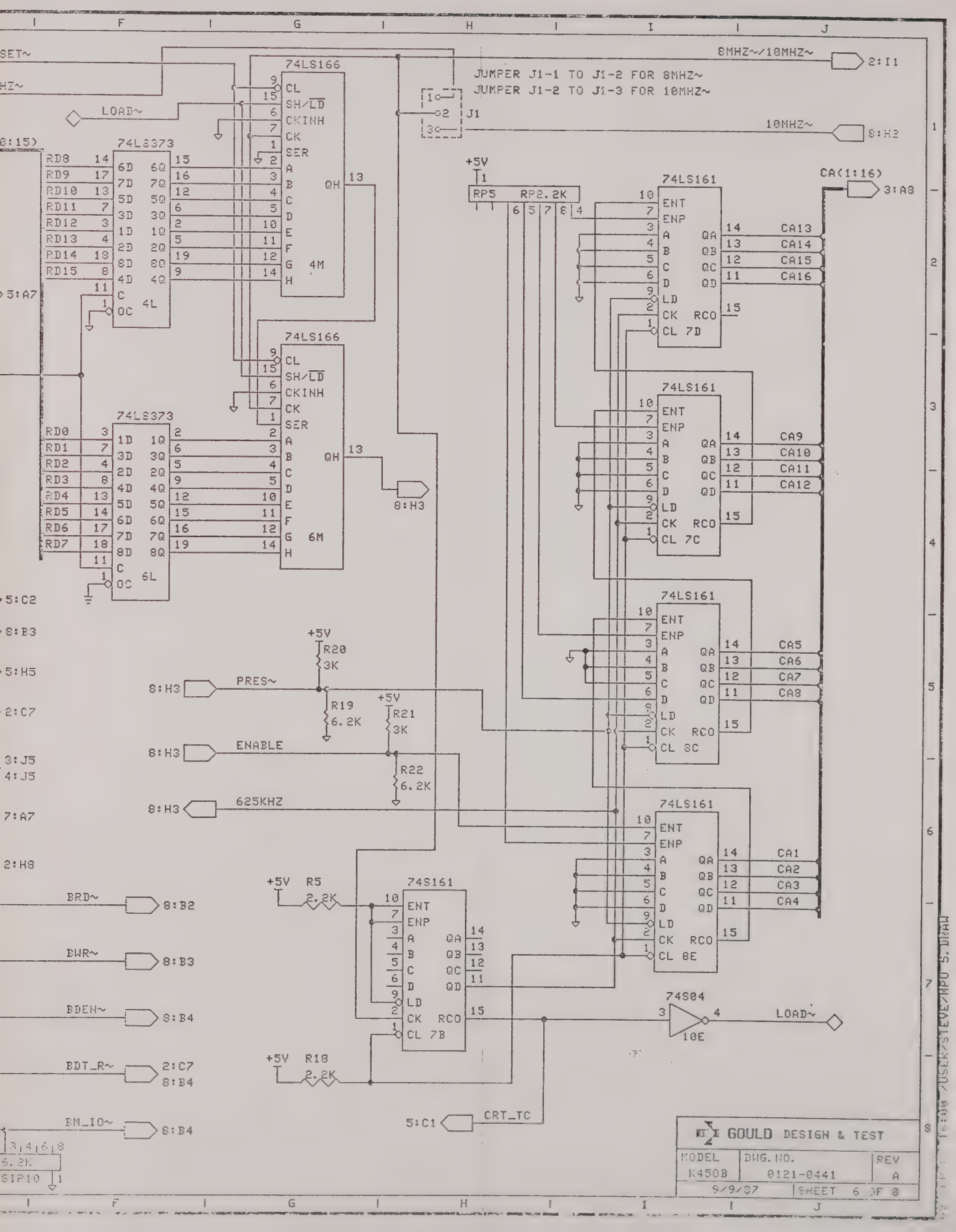

+5V
RP8
2.2K
74S240
PUP
8:H5
PUF~
74S08
NMI
2:A4
R2
2.2K
PRES
2:A4
C68
.01UF
6V
R15
2.2K
R16
510
R6
1.6K
RESWI~
8:H5
6:A7
C67
47UF
6V
RESET~
6:E1
BRES~
8:B4
CRT_TC
6:H3
RAMAD
6:E4
ALEBU
2:A5
74S00
74S112
R3
2.2K
8MHZ
8MHZ~
6:D1
2:A5
ALE~
74S38
82S84A
IO_M~
6:6A
CSYNC
AEN1N
RDY1
RDY2
AEN2N
ASYNCN
EFI
F/CN
RESN
PCLK
READY
CLK
OSC
RESET
X1
X2
12H
READY
2:A4
R10
1.6K
74S04
10E
24MHZ
RDY2
6:E2
M_IO~
2:6B
510
R11
Y1
24MHZF
510
R12
ALE~
BALE
8:H5
UNUSED
RP5
RP8

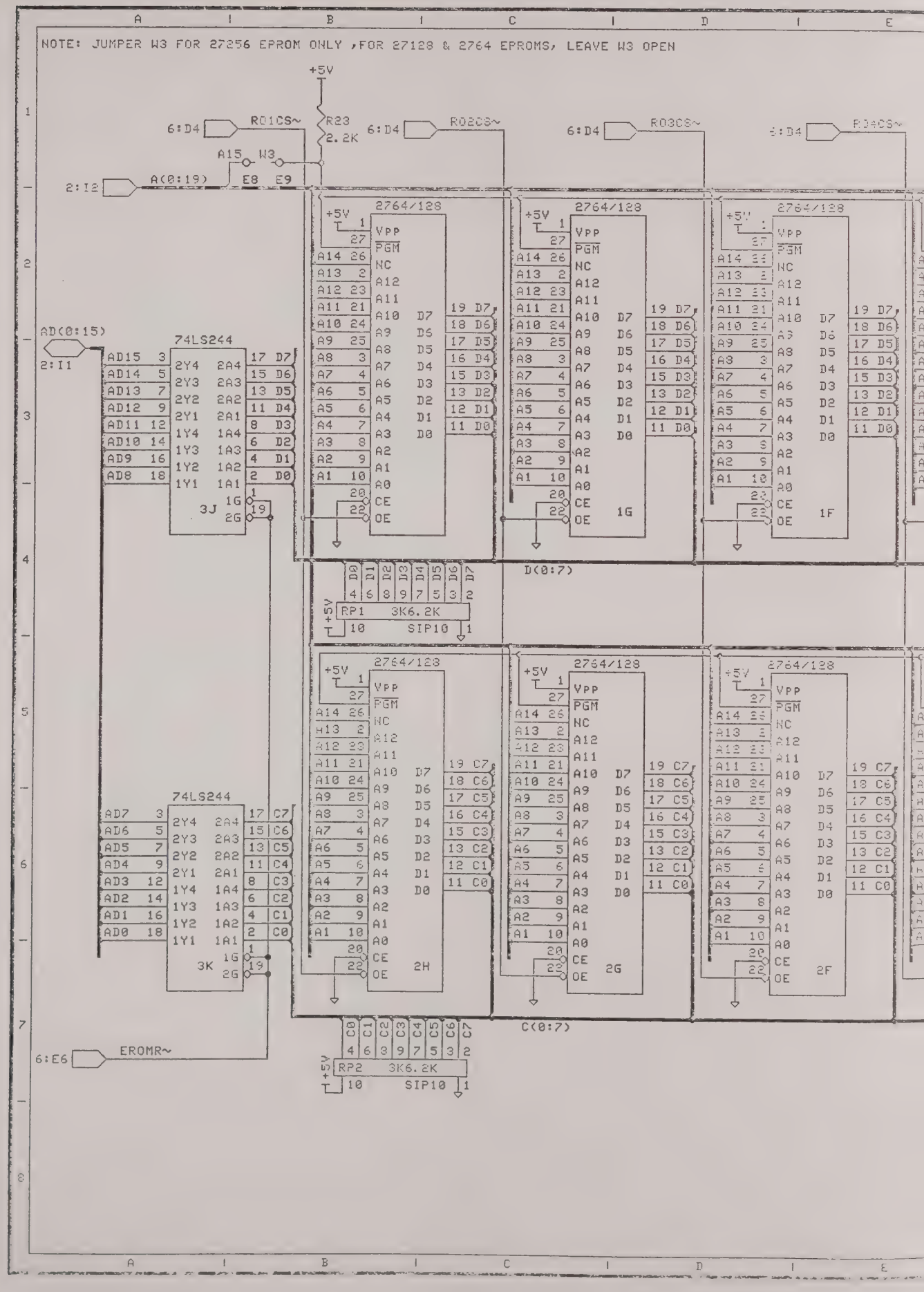


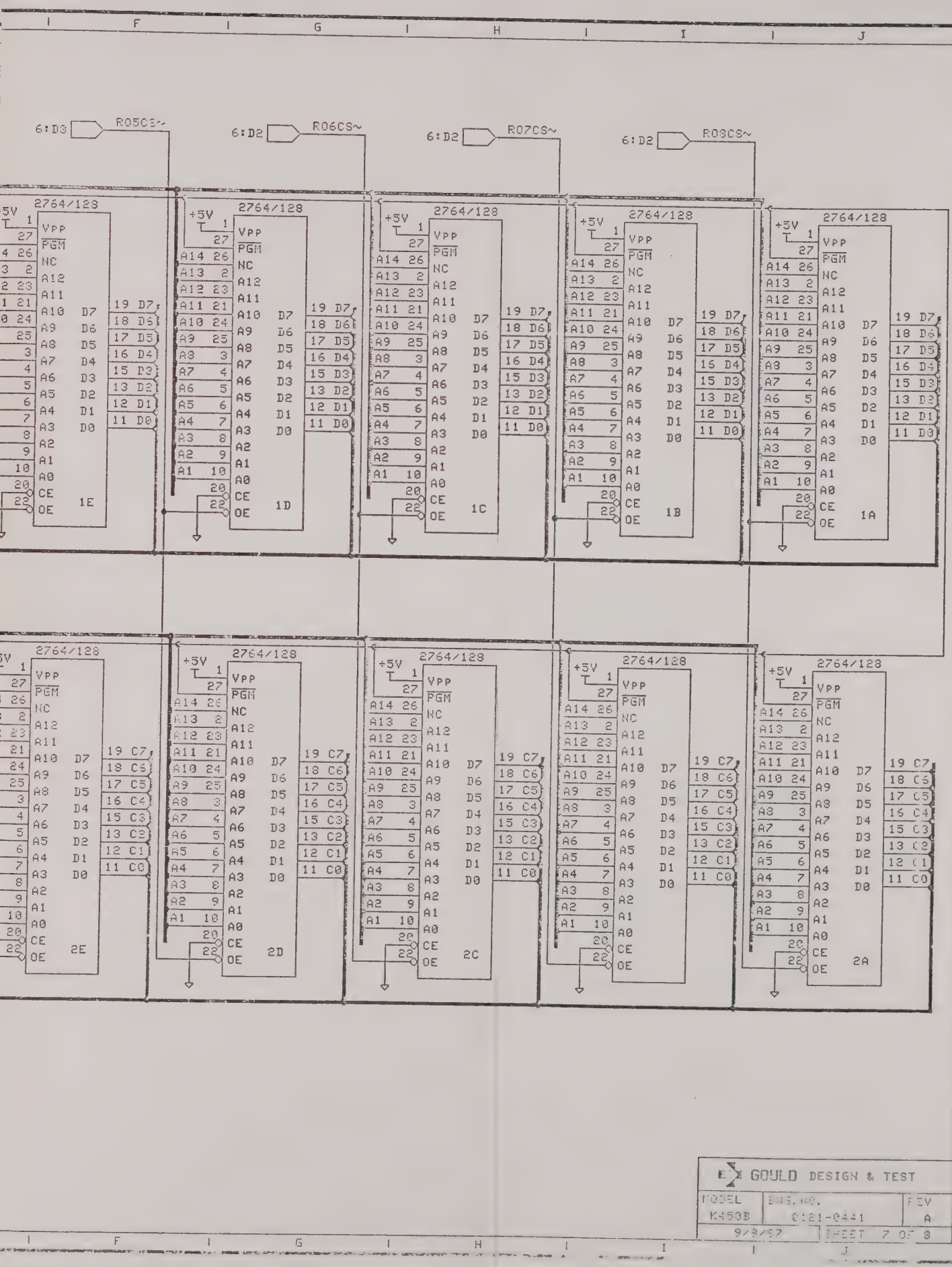
74S00
CCOLS~
3:A6
CROWS~
3:A8
MCOLS~
3:A2
MROWS~
3:A3
CRLAEN
6:E3
MLAEN
3:J6
4:J5
74S112
74S11
CRRCY
74S08
74S20
74S04
MRACY
74S10
R100
CAS0~
74S240
CAS1~
R101
WE1H~
R102
2:I1
BHE~
2:I5
A0
WE0H~
WE0L~
6:E5
RPAG1
RWEN~
2:B6
DT_R~
74LS175
RAS~
WE1L~
RP8
2.2K
RP5
RP2.2K
RP99
SIP10
74S51
SLOW
FAST
LACLK
R13
270
R14
91
CLK
2:A5
TO 8086 SLIGHTLY DELAYED
MORE DELAYED ON NEG. EDGE
E3
W4
E4
FAST RAM
(WITH W4)
SLOW RAM
(W/O W4)
GOULD DESIGN & TEST
MODEL
K450B
DWG. NO.
0121-0441
REV
A
9/9 87
SHEET 5 OF 8



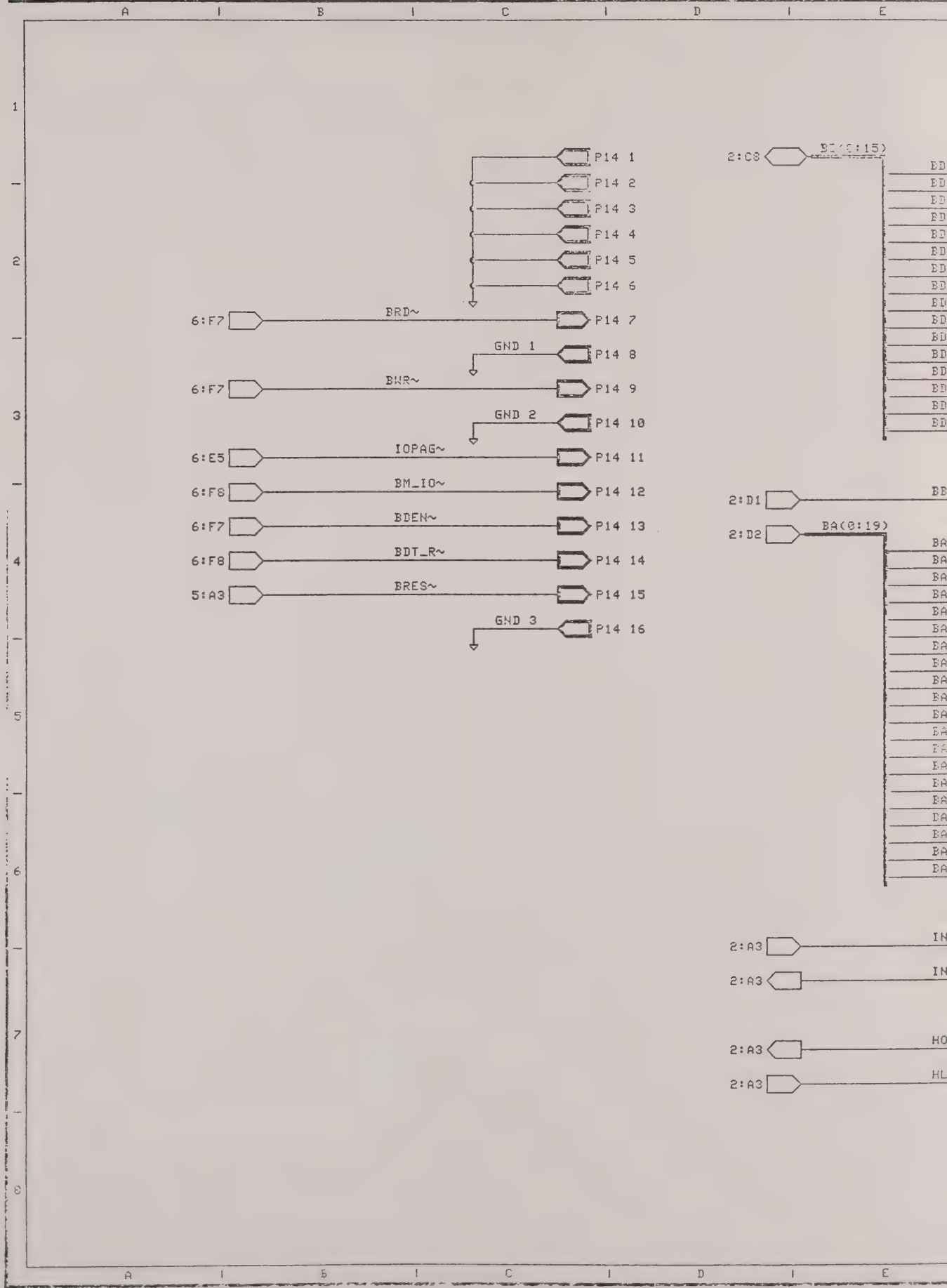
00 = 3 WAIT STATES
11 = NO WAIT STATES
82S129A
82S129
82S131
74LS192
74LS04
74LS244
74S20
74S10
RP8 RP2.2K
RP6 RP2.2K
RP14 RP2.2K
RP10 RP2.2K
RP9 3K6.2K
RP7
ALE~
RDY2
CRLAEN
RAMAD
IOAD~
IOPAG~
RPAG1
OFFDA~
ERAMR~
EROMR~
ESARD~
A(0:19)
ALEBU
IO_M~
S.A.~
GND
RD~
A15
RESWI~
N.C.
WR~
DEN~
DT_R~
M_IO~
HLDA
DEN
RD

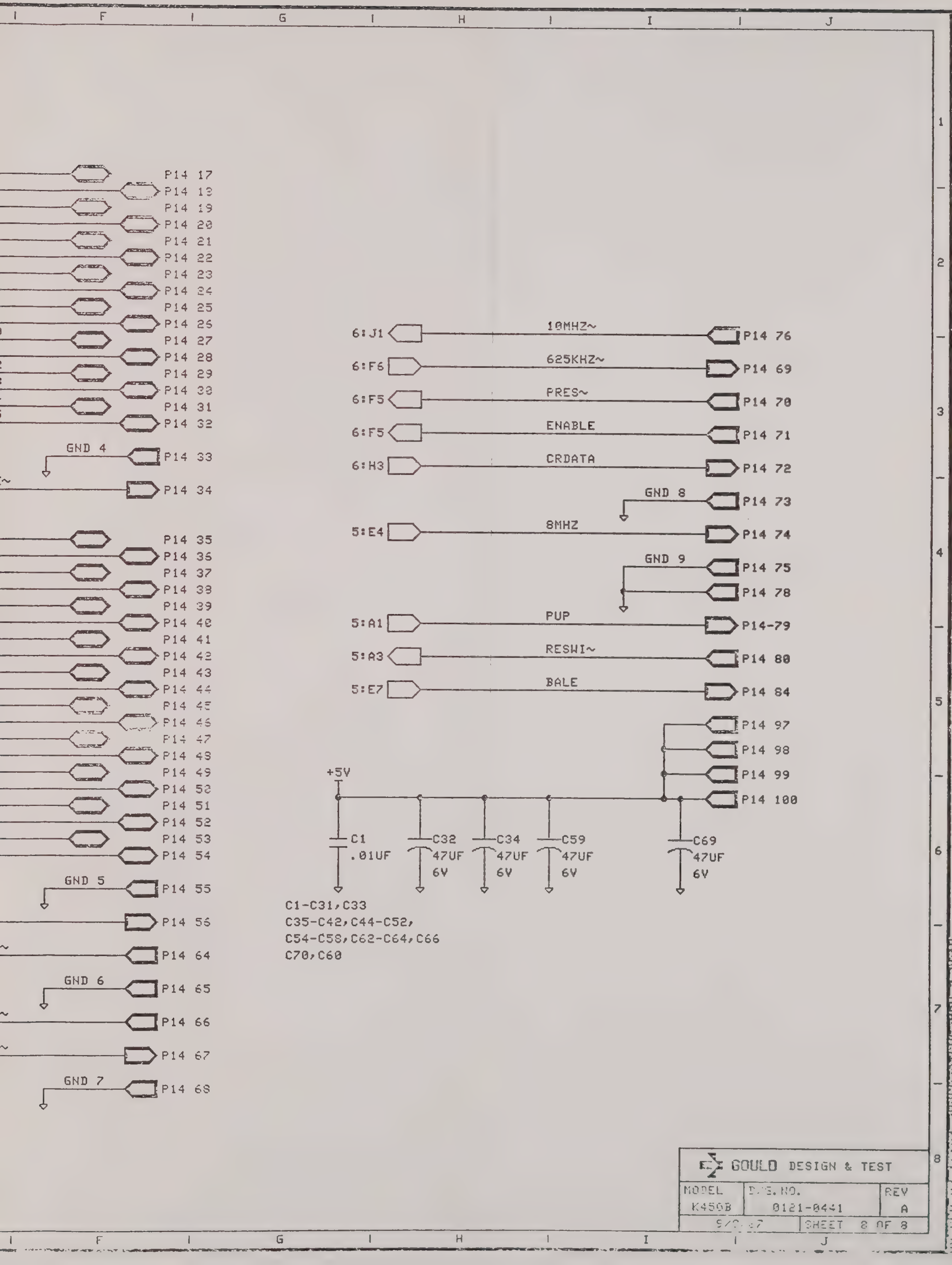

8MHZ~/10MHZ~
2:I1
JUMPER J1-1 TO J1-2 FOR 8MHZ~
JUMPER J1-2 TO J1-3 FOR 10MHZ~
J1
10MHZ~
8:H2
LOAD~
74LS166
74LS373
74LS161
74S161
74S04
+5V
RP5 RP2.2K
CA(1:16)
3:A8
CA13
CA14
CA15
CA16
CA9
CA10
CA11
CA12
CA5
CA6
CA7
CA8
CA1
CA2
CA3
CA4
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7
RD8
RD9
RD10
RD11
RD12
RD13
RD14
RD15
8:H3
PRES~
ENABLE
625KHZ
R20 3K
R19 6.2K
R21 3K
R22 6.2K
R5 2.2K
R18 2.2K
BRD~
BWR~
BDEN~
BDT_R~
BM_IO~
CRT_TC
5:C1
GOULD DESIGN & TEST
MODEL K450B
DWG. NO. 0121-0441
REV A
9/9/87
SHEET 6 OF 8

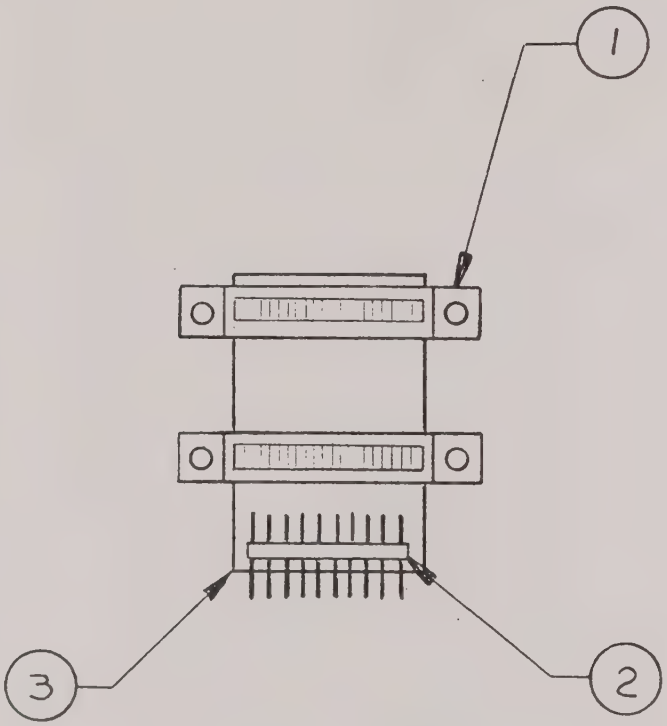

NOTE: JUMPER W3 FOR 27256 EPROM ONLY ,FOR 27128 & 2764 EPROMS, LEAVE W3 OPEN
+5V
R23
2.2K
6:D4
R01CS~
R02CS~
R03CS~
R04CS~
A15
W3
E8
E9
2:I2
A(0:19)
AD(0:15)
2:I1
74LS244
2764/128
VPP
PGM
NC
A12
A11
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
CE
OE
D7
D6
D5
D4
D3
D2
D1
D0
1G
2G
3J
D(0:7)
RP1
3K6.2K
SIP10
C(0:7)
3K
2H
2G
1F
RP2
6:E6
EROMR~



GOULD DESIGN & TEST		
MODEL K450B	DWG. NO. 0121-0441	REV A
9/8/87	SHEET 7 OF 8	


P14 1
P14 2
P14 3
P14 4
P14 5
P14 6
6:F7
BRD~
P14 7
GND 1
P14 8
6:F7
BWR~
P14 9
GND 2
P14 10
6:E5
IOPAG~
P14 11
6:F8
BM_IO~
P14 12
6:F7
BDEN~
P14 13
6:F8
BDT_R~
P14 14
5:A3
BRES~
P14 15
GND 3
P14 16
2:C8
2:D1
2:D2
BA(0:19)
2:A3
2:A3
2:A3
2:A3


F
G
H
I
J
P14 17
P14 18
P14 19
P14 20
P14 21
P14 22
P14 23
P14 24
P14 25
P14 26
P14 27
P14 28
P14 29
P14 30
P14 31
P14 32
GND 4
P14 33
P14 34
P14 35
P14 36
P14 37
P14 38
P14 39
P14 40
P14 41
P14 42
P14 43
P14 44
P14 45
P14 46
P14 47
P14 48
P14 49
P14 50
P14 51
P14 52
P14 53
P14 54
GND 5
P14 55
P14 56
P14 64
GND 6
P14 65
P14 66
P14 67
GND 7
P14 68
6:J1
10MHZ~
P14 76
6:F6
625KHZ~
P14 69
6:F5
PRES~
P14 70
6:F5
ENABLE
P14 71
6:H3
CRDATA
P14 72
GND 8
P14 73
5:E4
8MHZ
P14 74
GND 9
P14 75
P14 78
5:A1
PUP
P14-79
5:A3
RESWI~
P14 80
5:E7
BALE
P14 84
P14 97
P14 98
P14 99
P14 100
+5V
C1
.01UF
C32
47UF
6V
C34
47UF
6V
C59
47UF
6V
C69
47UF
6V
C1-C31, C33
C35-C42, C44-C52,
C54-C58, C62-C64, C66
C70, C60
GOULD DESIGN & TEST
MODEL
K450B
DWG. NO.
0121-0441
REV
A
SHEET 8 OF 8
/USER/STEVE/MPU 7.DRAW

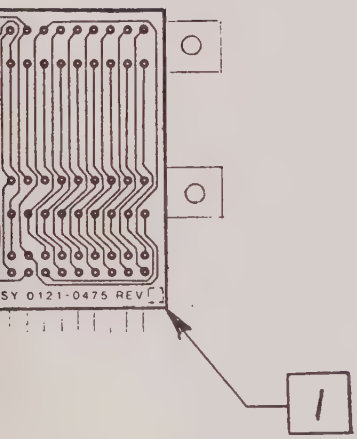


COMP. SIDE

DWG. NO. 0121-0475	SH 1	REV 50

REVISIONS

ZONE	REV	ECO #	DESCRIPTION	DWN	CHKD	APPD
	50	5644	PILOT RELEASE	MM	DGW	5/1/87



1

OLDER SIDE
(REF)

NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY REV. LEVEL WHERE SHOWN USING CONTRASTING INDELIBLE INK.
2. MANUFACTURE PER GOULD WORKMANSHIP STD. 87000012.

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

DASH NO	NEXT ASSY	USED ON
-10	0121-0405	K450B

FIRST APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN RTM	4/1/87
CHECKED DGW	5/1/87
PROJ ENG	

GOULD ELECTRONICS

TITLE: ASSY, PROBE TEST PCB, K450B

SIZE B | DWG NO 0121-0475 | REV 50

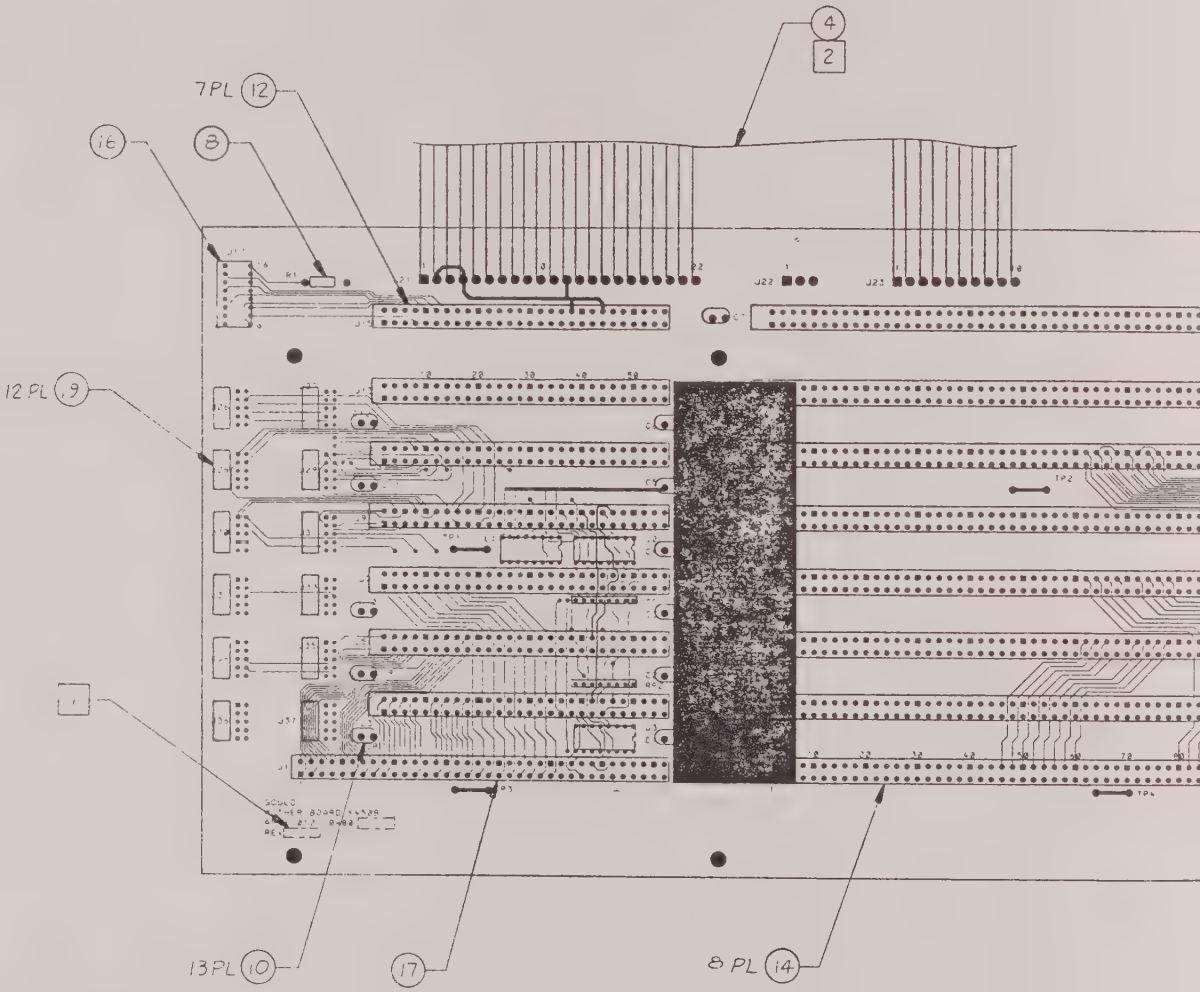
SCALE 1/1 MODEL K450B

BILL OF MATERIAL

AS OF 10/30/87

0121-0475-10 ASSY,PCB,PROBE TEST,K450B
MODEL: K450E

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	B0121-0475	DWG,ASSY,PCB,PROBE TEST	0	EA	REF
0	B0121-0476	SCHEM,PCB,PROBE TESTK450B	0	EA	REF
1	6000-0396-10	CONN 10/20 C-EDGE	2	EA	J7,J8
2	6000-0384-10	CONN 20 POS RT ANGLE HDR	1	EA	P6
3	0121-0477-10	FAB,PCB,PROBE TEST,K450E	0	EA	



NOTES: UNLESS OTHERWISE SPECIFIED

1. MARK ASSEMBLY DASH NO., & REV. LE
USING CONTRASTING INDELIBLE INK
2. SOLDER HARNESS (ITEM 4) TO NEARS
TO APPROPRIATE DESIGNATIONS (J21, J2
3. INSTALL LEADS PER TABLE 1.

DWG. NO.	SH	REV.
0121-0480	1	52

REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	5629	PILOT RELEASE	RTM	DLW	4/9/87
	52	5716	REVISED PER ECO 6-8-87	MM	DLW	6/7/87

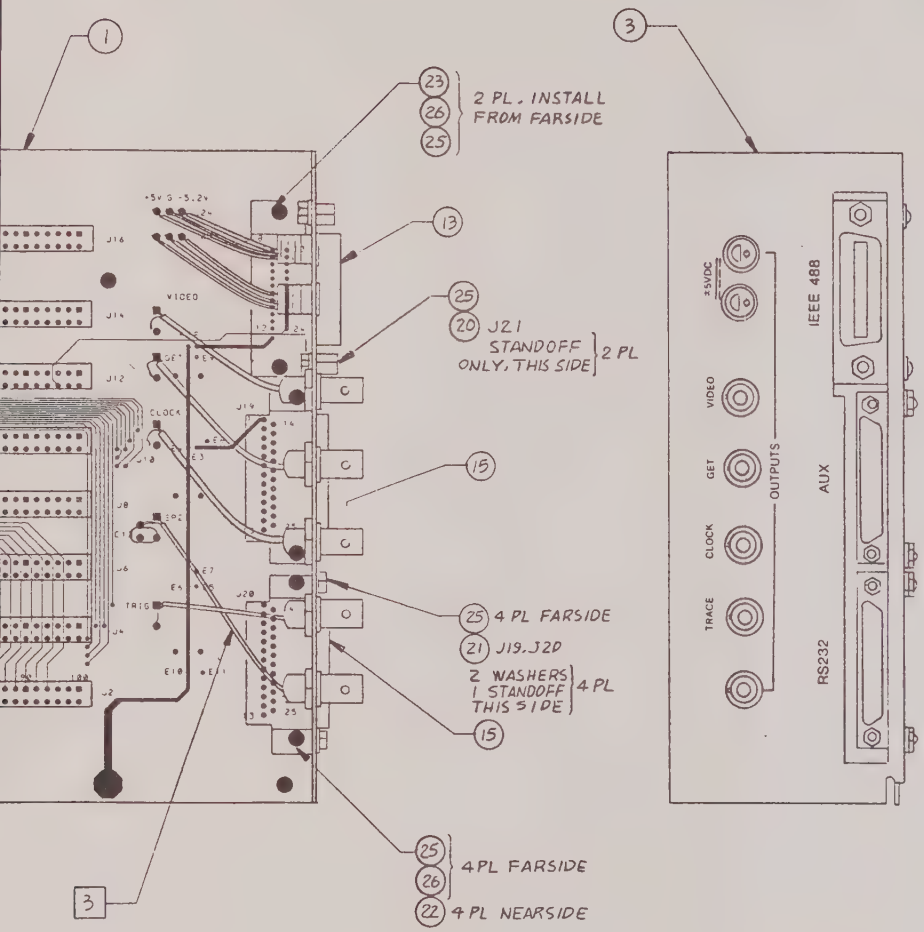


TABLE 1 [3]

PANEL WIRING		
PANEL		MOTHER BD
(SPARE)	BNC	SP2
	SHIELD	SP2
TRACE	BNC	TRIG
	SHIELD	TRIG
CLOCK	BNC	CLOCK
	SHIELD	CLOCK
GET	BNC	GET
	SHIELD	GET
VIDEO	BNC	VIDEO
	SHIELD	VIDEO
LEFT LEMO	GRN	J25 -5.2V
	BLK	J25 GND
	RED	J25 +5V
RIGHT LEMO	GRN	J24 -5.2V
	BLK	J24 GND
	RED	J24 +5V

VEL WHERE SHOWN

IDE OF BOARD
3 PADS).

-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± / DECIMALS XX ± / XXX ± / ANGLES ± /

MATERIAL

FINISH

DO NOT SCALE DRAWING

GOULD PART NO.

APPROVALS	DATE
DRAWN RTM	3/5/87
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: ASSEMBLY, MOTHER BD. K450B

SIZE	DWG NO	REV
D	0121-0480	52

SCALE 1/1 MODEL K450B SHEET 1 OF 1

DASH NO.	NEXT ASSY	USED ON
-10	0121-0406-10	K450B

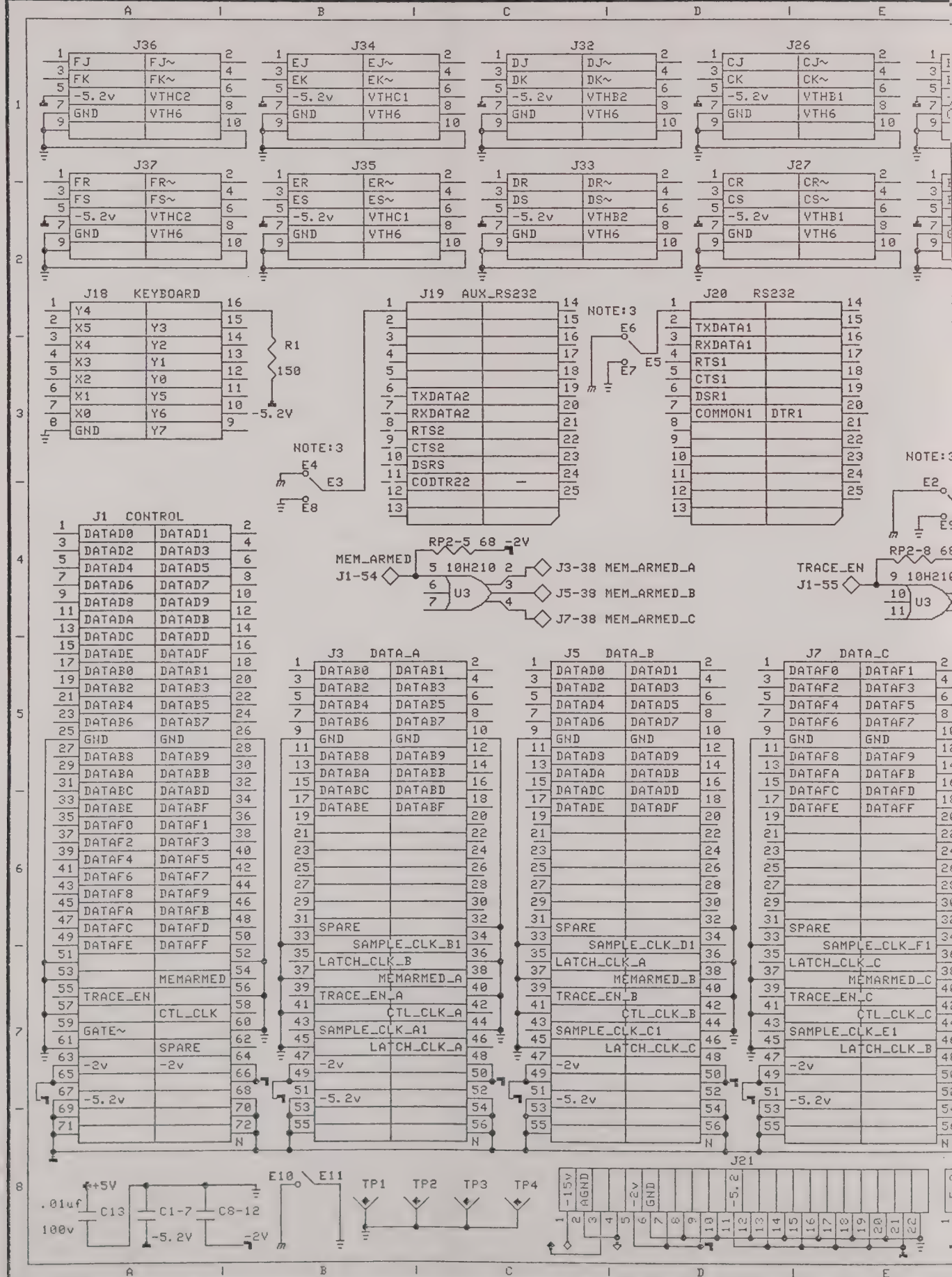
FIRST APPLICATION

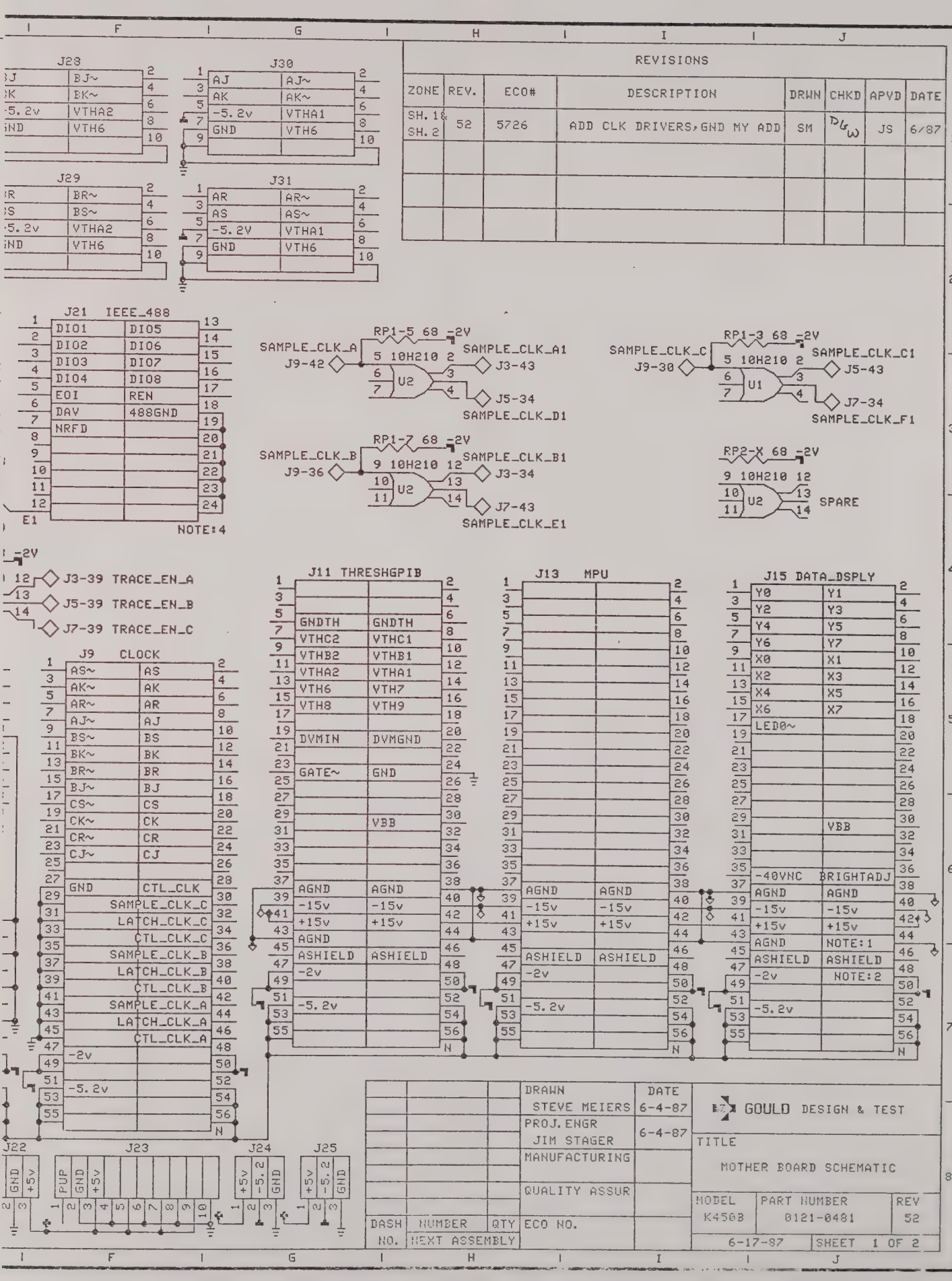
BILL OF MATERIAL

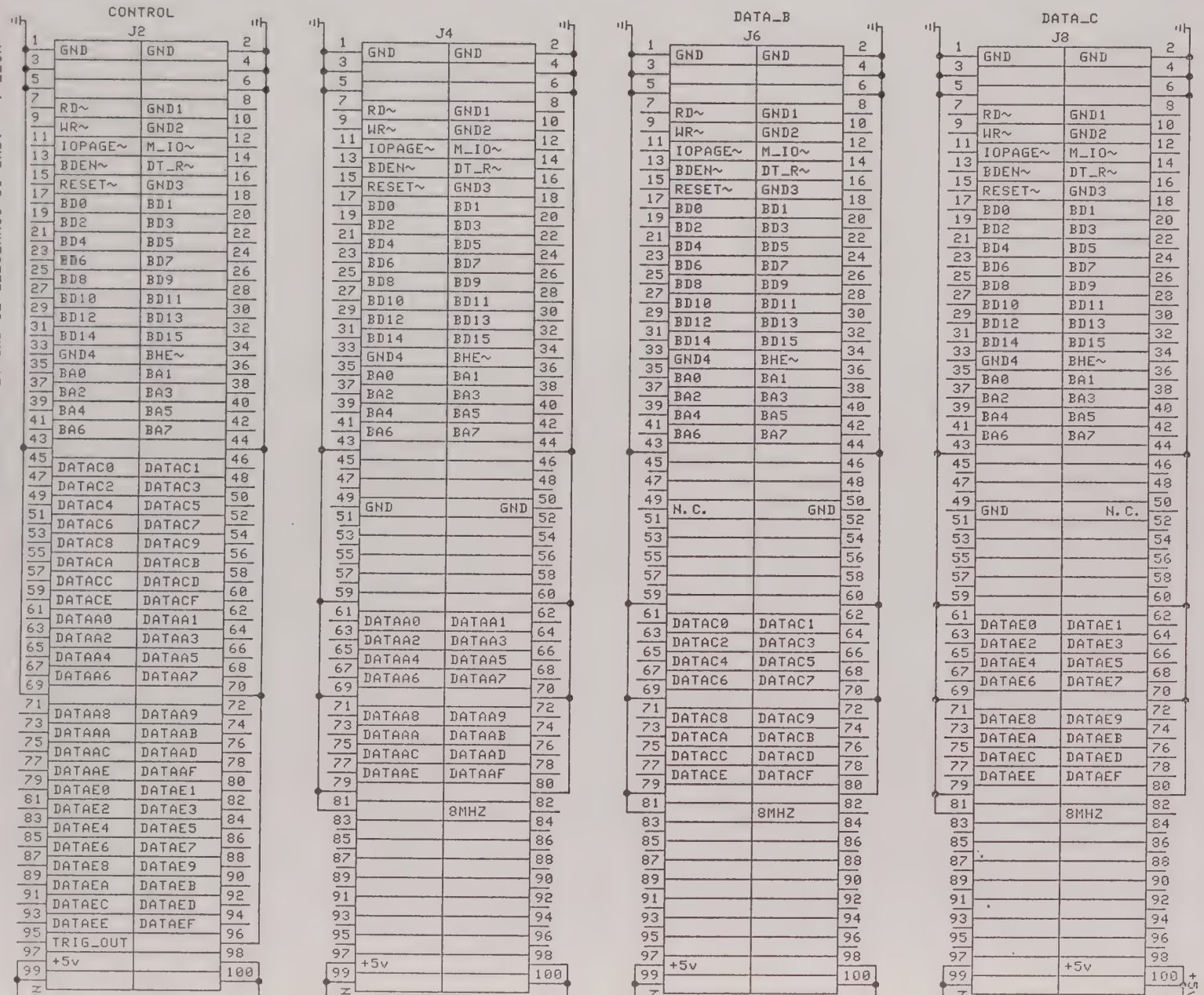
AS OF 10/30/87

0121-0480-10 ASSY,PCB,MOTHERBOARD,K450B
MODEL: K450B

ITEM #	PART NUMBER	DESCRIPTION	QTY PER ASSEMBLY	UM	REFERENCE DESIGNATOR
0	D0121-0480	DWG,ASSY,PCB,MOTHERBOARD,K450B	0	EA	REF
0	D0121-0481	SCHEM,PCB,MOTHERBOARD,K450B	0	EA	REF
1	0121-0482-10	FAB,PCB,MOTHERBOARD,K450B	1	EA	
3	0120-0092-10	ASSY PNL REAR MTHRBD K205	1	EA	
4	0121-0167-10	ASSY,HARNESS,PS TO MOTHER,K450	1	EA	
8	3000-1500-10	RES,150,5%,1/4W,C	1	EA	R1
10	4000-0025-10	CAP,0.1UF,50V,20%,CER	13	EA	C1-C13
12	6000-0198-10	CONN DUAL 28 PC	7	EA	J15 J3,J5,J7, J9,J11,J13
13	6000-0315-10	CONN 24 PIN RECEPT	1	EA	J18
14	6000-0333-10	CONN 50 PIN DUAL PC	8	EA	J14,J16 J2,J4,J6, J8,J10,J12
15	6000-0353-10	CONN 25 POS. PCB	2	EA	J19,J20
16	6100-0120-10	SKT 16 PIN DIP LO-PROFIL	1	EA	J17
17	6000-0333-20	CONN 36/72 DUAL PC	1	EA	J1
19	6000-0552-20	CONN RT ANGLE 5 PIN DUAL	12	EA	J26-J37
20	7000-0399-10	HDWR MTG HDWR FOR GPIB	1	EA	J21
21	7000-0620-10	JACK SCREW,4-40 X 5/16	4	EA	
22	7011-1440-12	SCR,X,PH,4-40 X 3/8,STZN	4	EA	
23	7011-1440-14	SCR,X,PH,4-40 X 7-16,STZN	2	EA	
25	7071-1440-00	NUT,S-LOCK,4-40,STD,STZN	12	EA	
26	7081-1004-00	WSHR,FLAT,#4,STD PAT,STZN	6	EA	
27	1850-0145-10	IC 10H210 3-IN 3-OUT OR	3	EA	U1,U2,U3
28	3700-0091-10	RPAK,68,0.2W,2%,8/7	2	EA	RP1,RP2


J36
FJ FJ~
FK FK~
-5.2v VTHC2
GND VTH6
J34
EJ EJ~
EK EK~
-5.2v VTHC1
GND VTH6
J32
DJ DJ~
DK DK~
-5.2v VTHB2
GND VTH6
J26
CJ CJ~
CK CK~
-5.2v VTHB1
GND VTH6
J37
FR FR~
FS FS~
-5.2v VTHC2
GND VTH6
J35
ER ER~
ES ES~
-5.2v VTHC1
GND VTH6
J33
DR DR~
DS DS~
-5.2v VTHB2
GND VTH6
J27
CR CR~
CS CS~
-5.2v VTHB1
GND VTH6
J18 KEYBOARD
Y4
X5 Y3
X4 Y2
X3 Y1
X2 Y0
X1 Y5
X0 Y6
GND Y7
R1
150
-5.2V
NOTE:3
E4
E3
E8
J19 AUX_RS232
TXDATA2
RXDATA2
RTS2
CTS2
DSRS
CODTR22
NOTE:3
E6
E5
E7
J20 RS232
TXDATA1
RXDATA1
RTS1
CTS1
DSR1
COMMON1 DTR1
NOTE:3
E2
J1 CONTROL
DATAD0 DATAD1
DATAD2 DATAD3
DATAD4 DATAD5
DATAD6 DATAD7
DATAD8 DATAD9
DATADA DATADB
DATADC DATADD
DATADE DATADF
DATAB0 DATAB1
DATAB2 DATAB3
DATAB4 DATAB5
DATAB6 DATAB7
GND GND
DATAB8 DATAB9
DATABA DATABB
DATABC DATABD
DATABE DATABF
DATAF0 DATAF1
DATAF2 DATAF3
DATAF4 DATAF5
DATAF6 DATAF7
DATAF8 DATAF9
DATAFA DATAFB
DATAFC DATAFD
DATAFE DATAFF
MEMARMED
TRACE_EN CTL_CLK
GATE~ SPARE
-2v -2v
-5.2v
RP2-5 68 -2V
MEM_ARMED
J1-54
5 10H210 2
6 3
7 U3 4
J3-38 MEM_ARMED_A
J5-38 MEM_ARMED_B
J7-38 MEM_ARMED_C
RP2-8 68
TRACE_EN
J1-55
9 10H210
10 11 U3
J3 DATA_A
DATAB0 DATAB1
DATAB2 DATAB3
DATAB4 DATAB5
DATAB6 DATAB7
GND GND
DATAB8 DATAB9
DATABA DATABB
DATABC DATABD
DATABE DATABF
SPARE
SAMPLE_CLK_B1
LATCH_CLK_B
MEMARMED_A
TRACE_EN_A
CTL_CLK_A
SAMPLE_CLK_A1
LATCH_CLK_A
-2v
-5.2v
J5 DATA_B
DATAD0 DATAD1
DATAD2 DATAD3
DATAD4 DATAD5
DATAD6 DATAD7
GND GND
DATAD8 DATAD9
DATADA DATADB
DATADC DATADD
DATADE DATADF
SPARE
SAMPLE_CLK_D1
LATCH_CLK_A
MEMARMED_B
TRACE_EN_B
CTL_CLK_B
SAMPLE_CLK_C1
LATCH_CLK_C
-2v
-5.2v
J7 DATA_C
DATAF0 DATAF1
DATAF2 DATAF3
DATAF4 DATAF5
DATAF6 DATAF7
GND GND
DATAF8 DATAF9
DATAFA DATAFB
DATAFC DATAFD
DATAFE DATAFF
SPARE
SAMPLE_CLK_F1
LATCH_CLK_C
MEMARMED_C
TRACE_EN_C
CTL_CLK_C
SAMPLE_CLK_E1
LATCH_CLK_B
-2v
-5.2v
J21
+5V
.01uf
100v
C13
C1-7
C8-12
-5.2V
-2V
E10
E11
TP1
TP2
TP3
TP4
-15v
AGND
-2v
GND
-5.2


REVISIONS
ZONE | REV. | ECO# | DESCRIPTION | DRWN | CHKD | APVD | DATE
SH. 1 & SH. 2 | 52 | 5726 | ADD CLK DRIVERS, GND MY ADD | SM | DLW | JS | 6/87
J23
J30
J29
J31
J21 IEEE_488
DIO1 DIO2 DIO3 DIO4 EOI DAV NRFD DIO5 DIO6 DIO7 DIO8 REN 488GND
NOTE:4
SAMPLE_CLK_A J9-42 RP1-5 68 -2V 5 10H210 2 U2 SAMPLE_CLK_A1 J3-43 J5-34 SAMPLE_CLK_D1
SAMPLE_CLK_C J9-30 RP1-3 68 -2V 5 10H210 2 U1 SAMPLE_CLK_C1 J5-43 J7-34 SAMPLE_CLK_F1
SAMPLE_CLK_B J9-36 RP1-7 68 -2V 9 10H210 12 U2 SAMPLE_CLK_B1 J3-34 J7-43 SAMPLE_CLK_E1
RP2-X 68 -2V 9 10H210 12 U2 SPARE
-2V
J3-39 TRACE_EN_A
J5-39 TRACE_EN_B
J7-39 TRACE_EN_C
J9 CLOCK
AS~ AS AK~ AK AR~ AR AJ~ AJ BS~ BS BK~ BK BR~ BR BJ~ BJ CS~ CS CK~ CK CR~ CR CJ~ CJ GND CTL_CLK SAMPLE_CLK_C LATCH_CLK_C CTL_CLK_C SAMPLE_CLK_B LATCH_CLK_B CTL_CLK_B SAMPLE_CLK_A LATCH_CLK_A CTL_CLK_A -2v -5.2v
J11 THRESHGPIB
GNDTH GNDTH VTHC2 VTHC1 VTHB2 VTHB1 VTHA2 VTHA1 VTH6 VTH7 VTH8 VTH9 DVMIN DVMGND GATE~ GND VBB AGND AGND -15v -15v +15v AGND ASHIELD ASHIELD -2v -5.2v
J13 MPU
AGND AGND -15v -15v +15v ASHIELD ASHIELD -2v -5.2v
J15 DATA_DSPLY
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7 X0 X1 X2 X3 X4 X5 X6 X7 LED0~ VBB -40VNC BRIGHTADJ AGND AGND -15v -15v +15v +15v AGND NOTE:1 ASHIELD ASHIELD -2v NOTE:2 -5.2v
J22 GND +5v
J23 PUP GND +5v
J24 +5v -5.2 GND
J25 +5v -5.2 GND
DRAWN STEVE MEIERS DATE 6-4-87
PROJ. ENGR JIM STAGER 6-4-87
MANUFACTURING
QUALITY ASSUR
DASH NO. | NUMBER NEXT ASSEMBLY | QTY | ECO NO.
GOULD DESIGN & TEST
TITLE
MOTHER BOARD SCHEMATIC
MODEL K4503 | PART NUMBER 0121-0481 | REV 52
6-17-87 | SHEET 1 OF 2
18 JUN 87 08:53 /USER/MAJID/MOTHER 1.DRAW

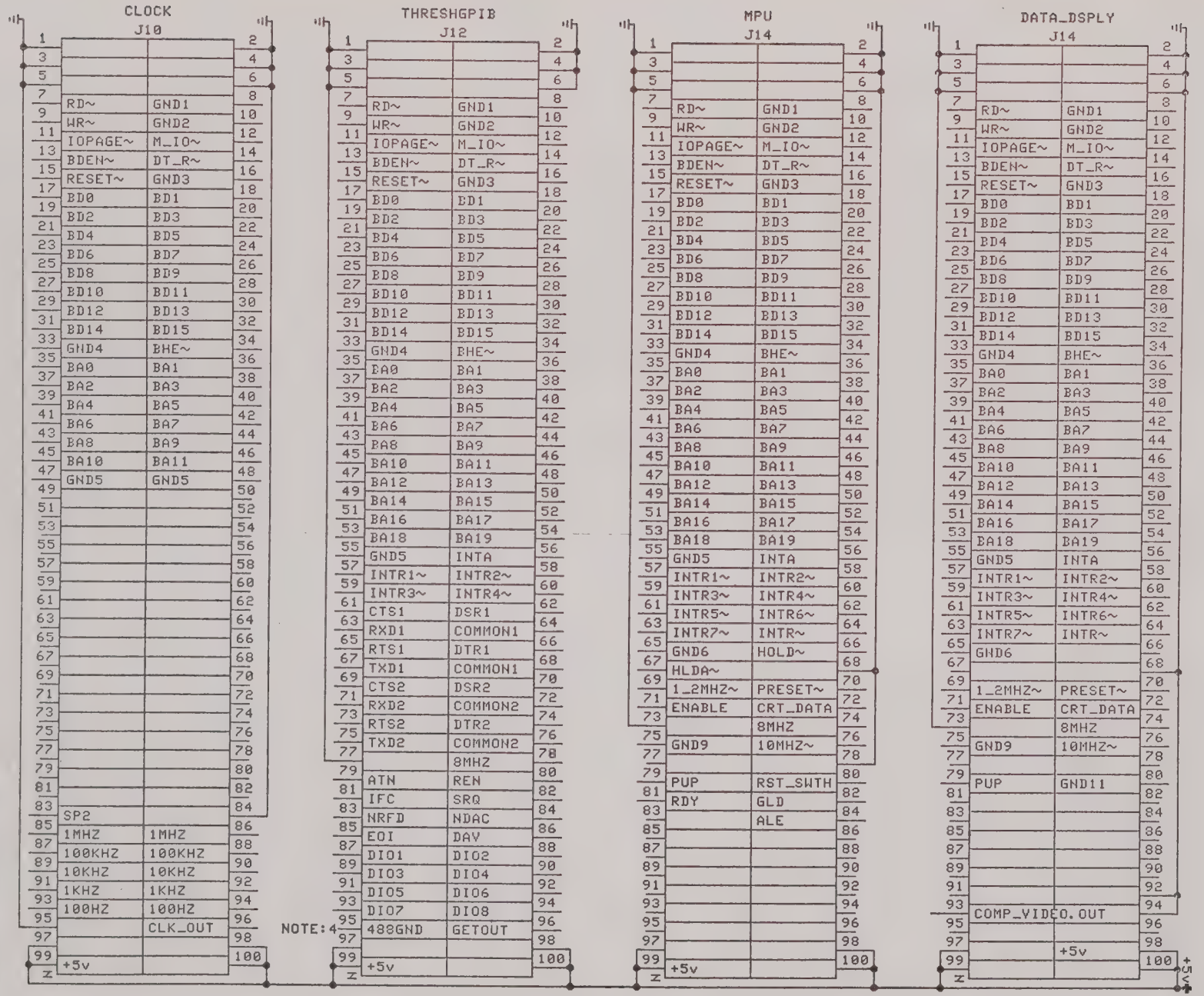


NOTE 1: AGND IS CONNECTED TO GND AT PINS J22-2,12.

NOTE 2: ASHIELD IS CONNECTED TO GND AT PIN J22-14.

NOTE 3: SHIELD IS CONNECTED TO GND BY TRACE TO E2(488), E4(449),E6(232).

NOTE 4: 488 GND IS CONNECTED TO GND AT J12-95.

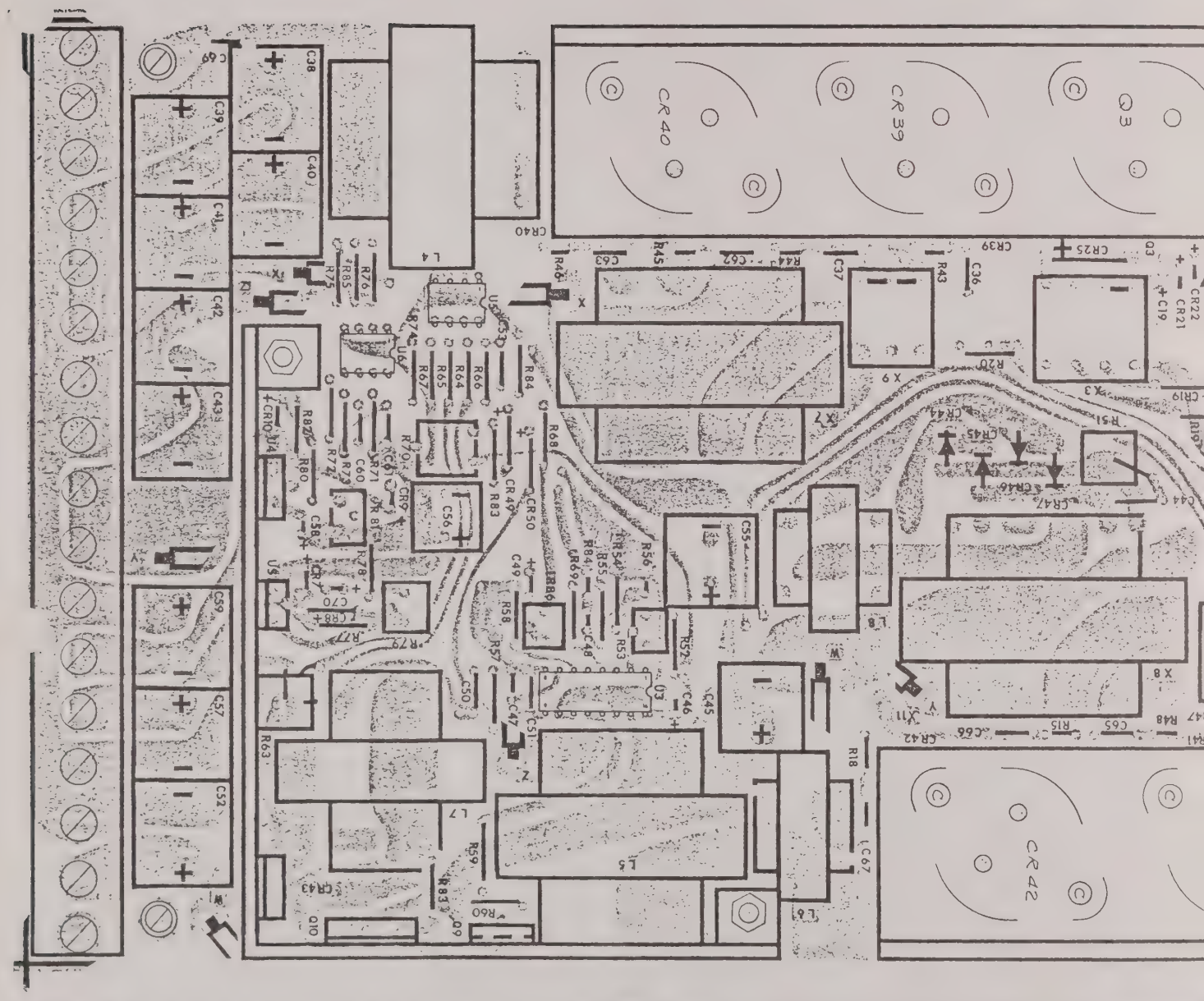


GOULD DESIGN & TEST

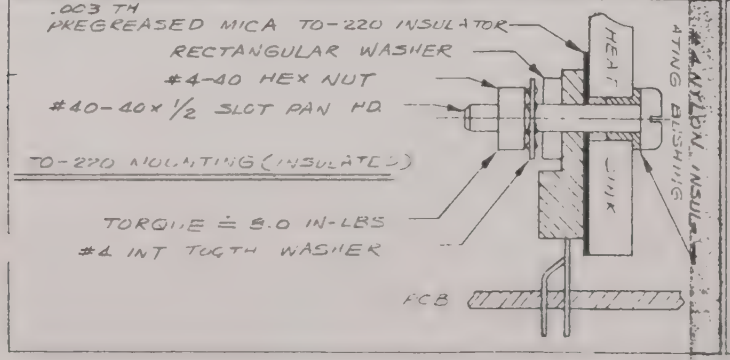
MODEL	DWG. NO.	REV
K-450B	0121-0481	52

JUNE 17, 1987 SHEET 2 OF 2

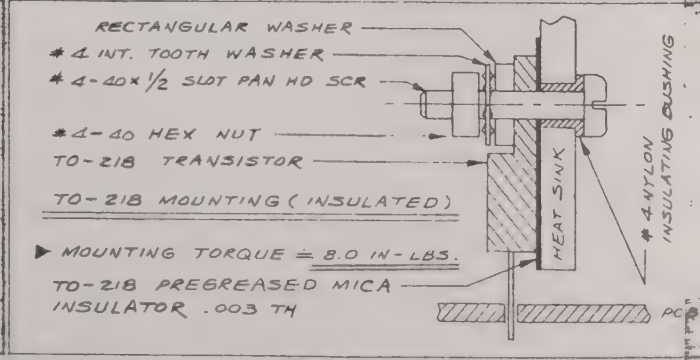
18 JUN 87 08:41 /USER/MAJID/MOTHER 2.DRAW



Q9, U4, U5 & CR43



Q10

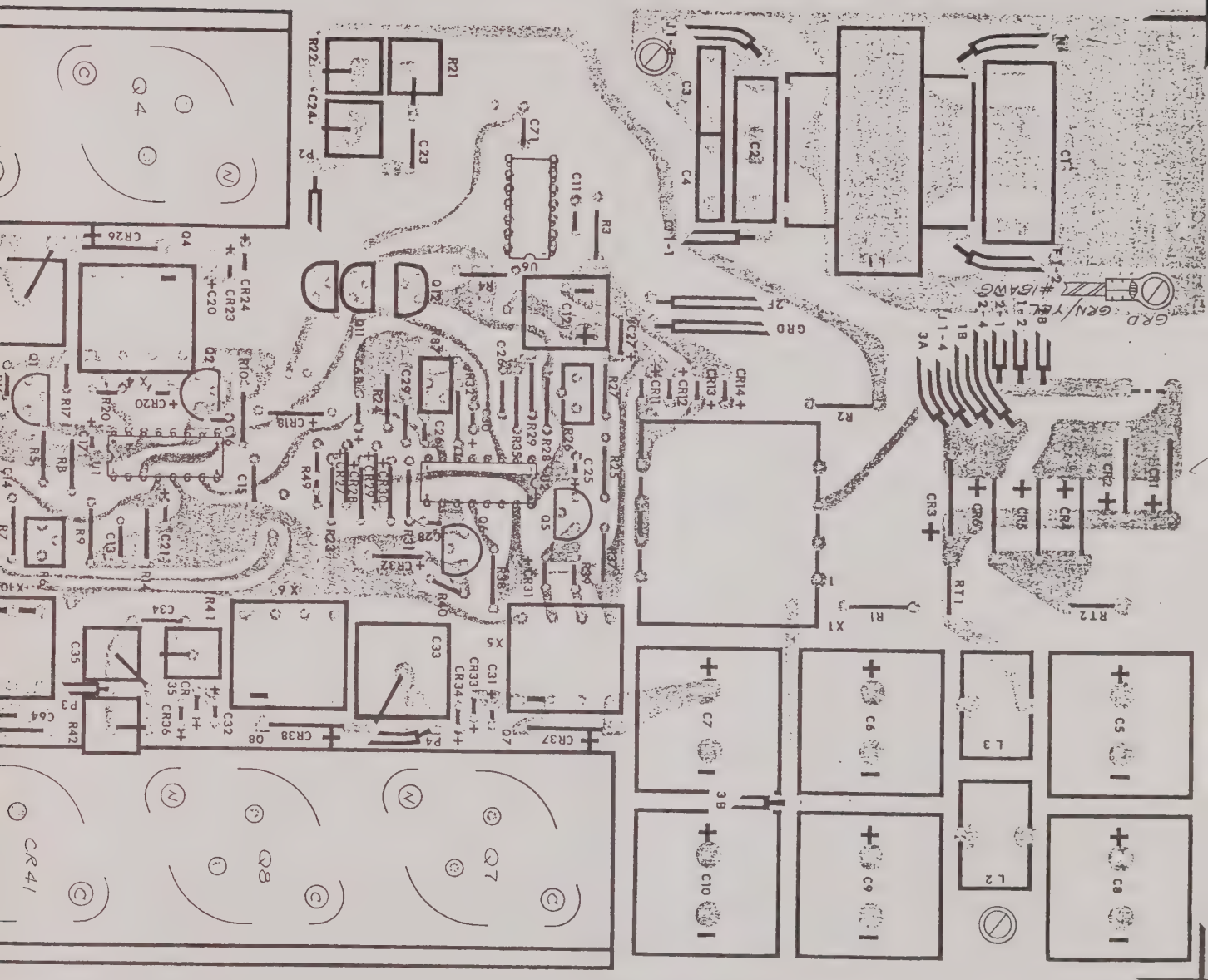


DWG. NO.	SH	REV.
D9000-0225	1	52

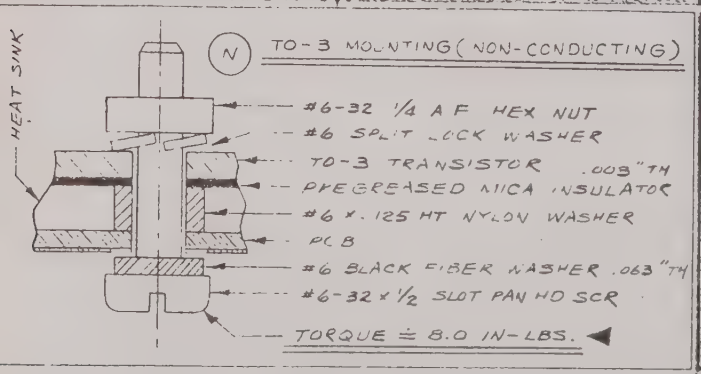
REVISIONS

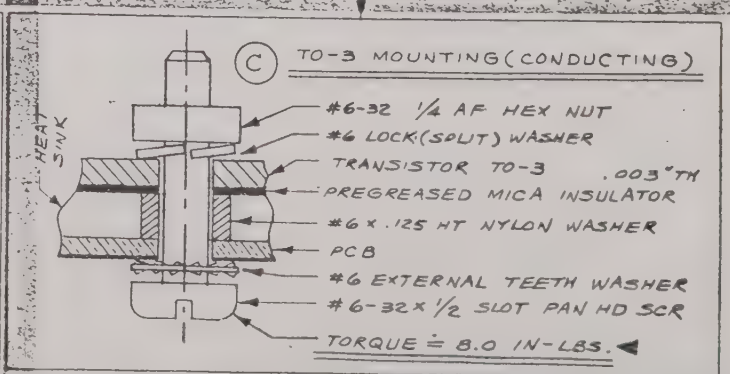
ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD
	51	5534A	REV ROLL ONLY 1-7-87	MM	DC	
	52	5643	REV ROLL ONLY 4-29-87	MM	DW	

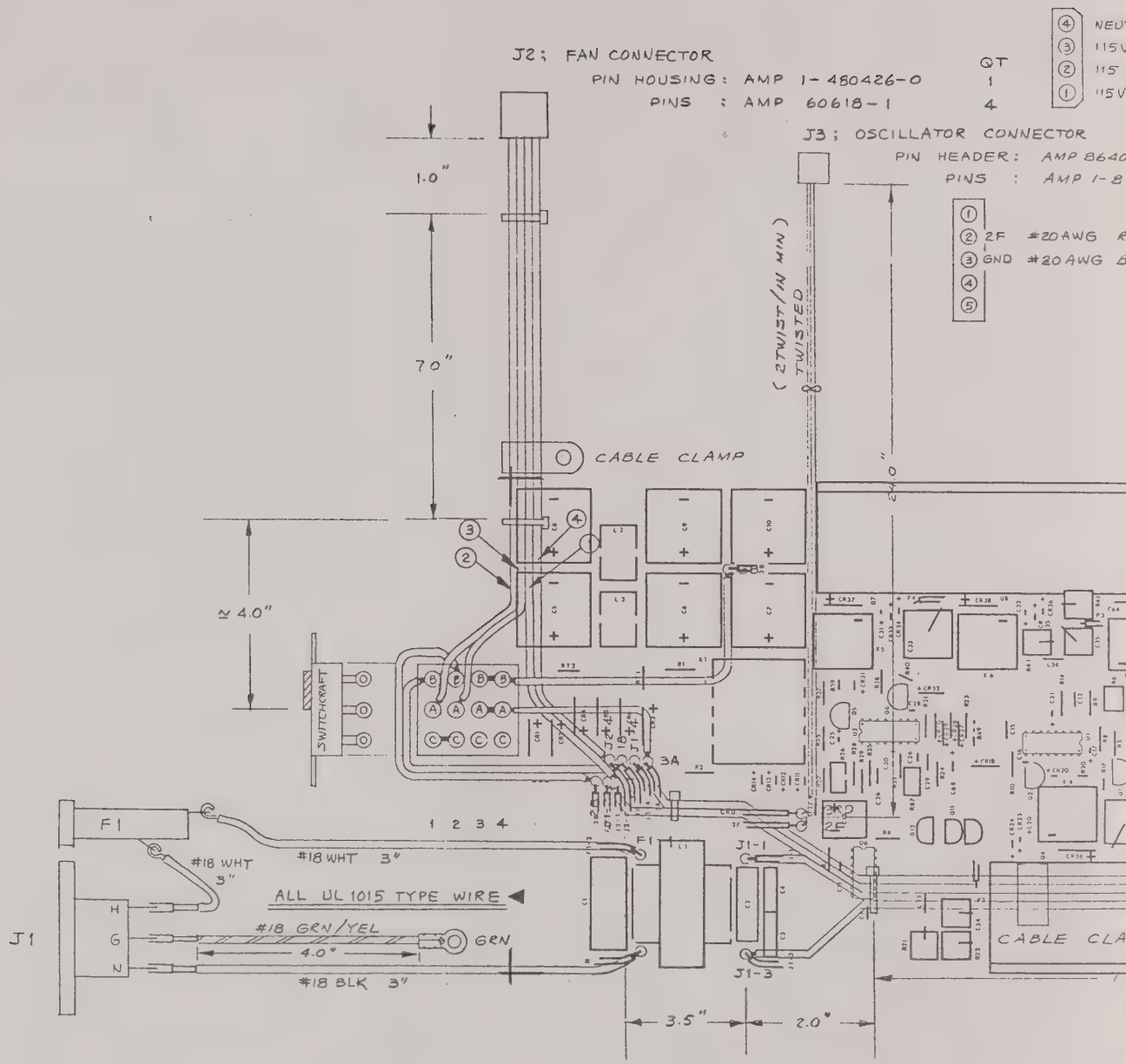
QS-402 ASSY DWG.
REV. B
6/26/86 BH



Q3, 4, 7, 8 & CR 39, 40, 41, 42



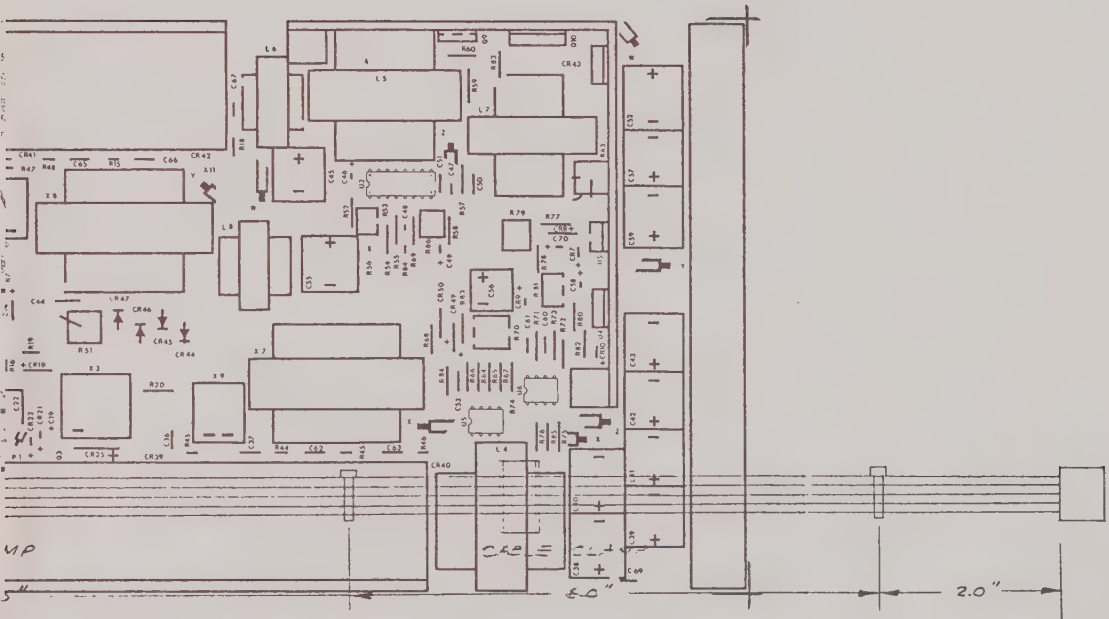



J2; FAN CONNECTOR
PIN HOUSING: AMP 1-480426-0
PINS : AMP 60618-1
QT
1
4
J3; OSCILLATOR CONNECTOR
PIN HEADER: AMP 8640
PINS : AMP 1-8
2F #20AWG
GND #20AWG
NEU
115V
115
115V
1.0"
7.0"
≥ 4.0"
(2TWIST/IN MIN)
TWISTED
CABLE CLAMP
SWITCHCRAFT
3A
F1
#18 WHT 3"
#18 WHT 3"
ALL UL 1015 TYPE WIRE
#18 GRN/YEL
4.0"
GRN
#18 BLK 3"
J1
H
G
N
J1-1
J1-3
3.5"
2.0"
CABLE CLA

S.W. YEL
BLK
S.W. RED
WHT
} #18 AWG INSULATED & STRANDED UL 1015 TYPE

	QT
?-6	1
1756-8	2

ED INSULATED (STRANDED) } WIRE TYPE
LACK " (") }



J1
4 YEL
3 BLK
2 RED
1 WHITE
} #18 AWG INS. STRANDED UL 1015 TYPE

J1; POWER SWITCH CONNECTOR

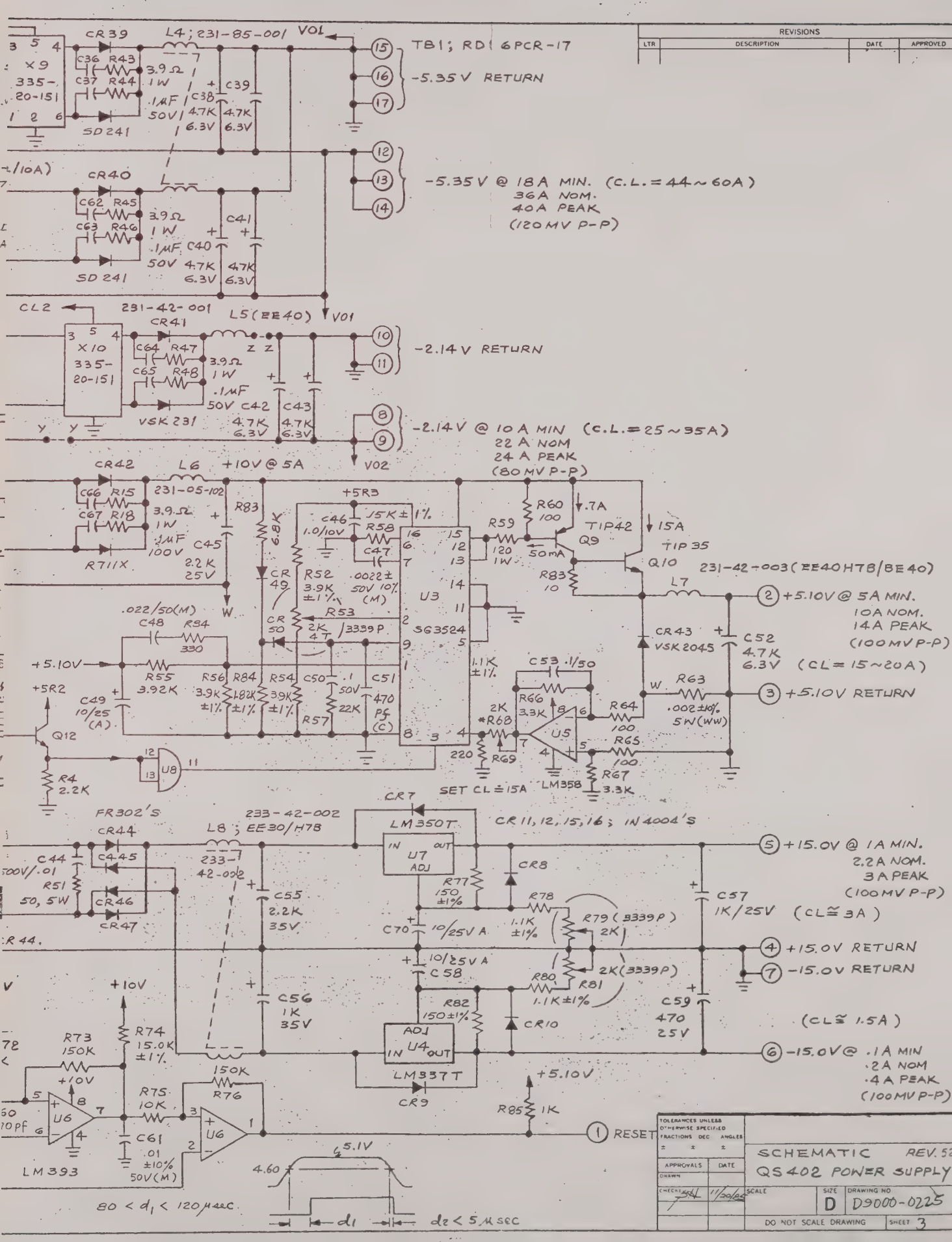
	QT.
SOCKET HOUSING: AMP 1-480425-0	1
SOCKETS: AMP 60617-1	4

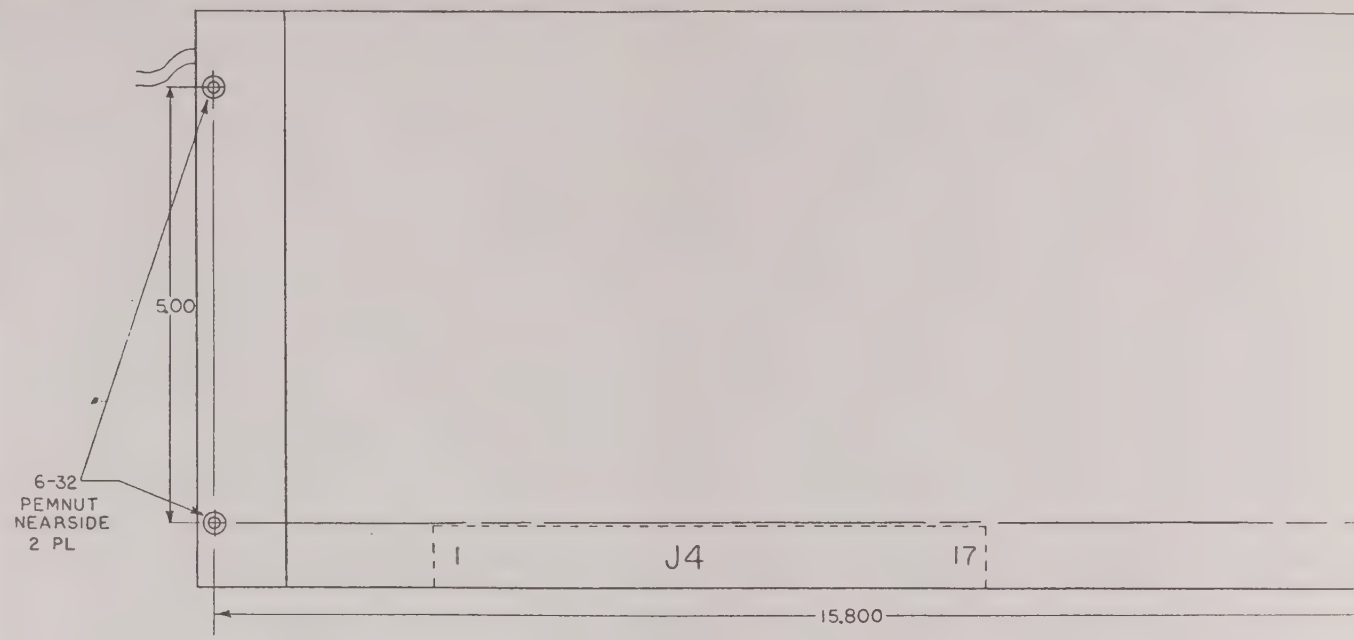
QS-402 WIRE HARNESS DWG.
6/27/86 BHL

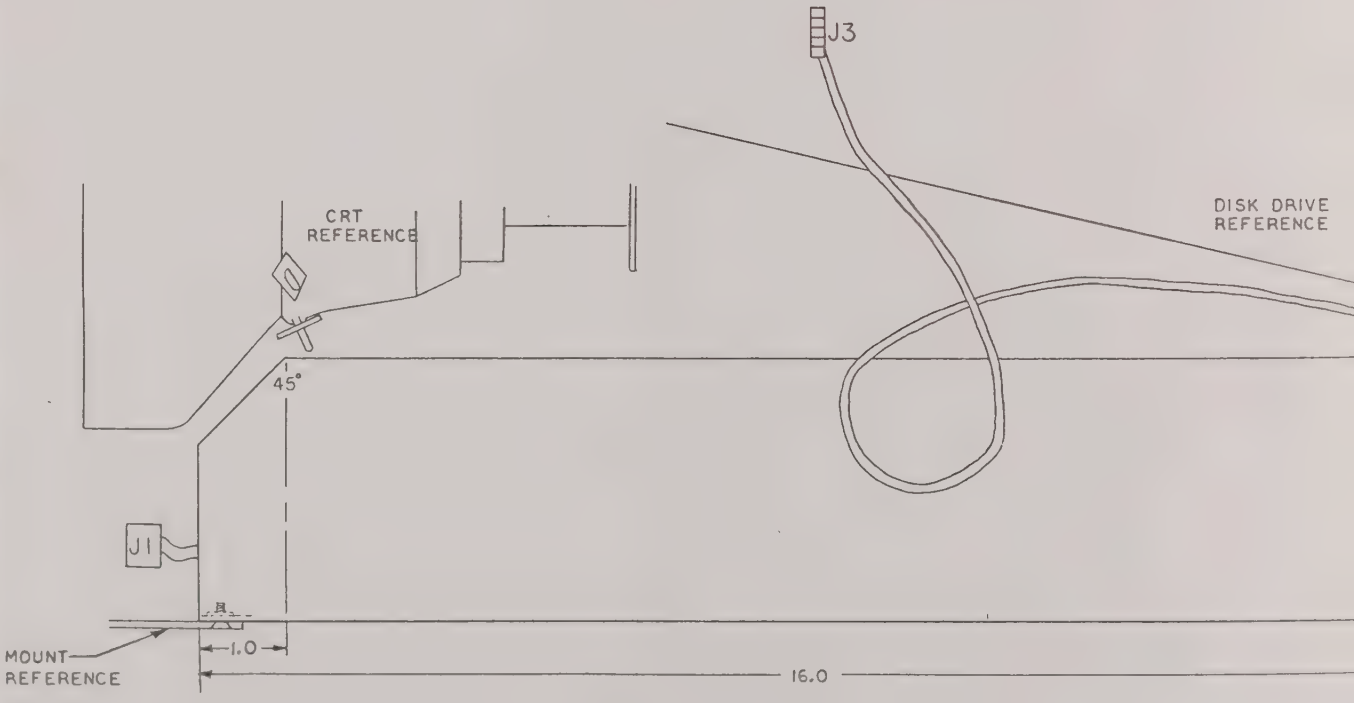
D9000-0225
REV 52
Sht. 2

NOTES: UNLESS SPECIFIED OTHERWISE

1) ALL RESISTORS ARE ±5%, ¼ W IN OHMS.
2) ALL CAPACITORS ARE ±20% IN MICRO FARADS.
3) ALL NPN TRANSISTORS ARE PN 3568
   ALL PNP TRANSISTORS ARE NP 3645
4) ALL DIODES ARE IN 4454 / IN 4148


REVISIONS
LTR
DESCRIPTION
DATE
APPROVED
TB1; RD1 6PCR-17
-5.35V RETURN
-5.35V @ 18A MIN. (C.L.=44~60A)
36A NOM.
40A PEAK
(120MV P-P)
-2.14V RETURN
-2.14V @ 10A MIN (C.L.=25~35A)
22A NOM
24A PEAK
(80MV P-P)
+10V @ 5A
231-42-003 (EE40H7B/BE40)
+5.10V @ 5A MIN.
10A NOM.
14A PEAK
(100MV P-P)
(CL=15~20A)
+5.10V RETURN
SET CL ≐ 15A
FR302'S
233-42-002
L8; EE30/H7B
CR11, 12, 15, 16; IN4004'S
+15.0V @ 1A MIN.
2.2A NOM.
3A PEAK
(100MV P-P)
(CL≅3A)
+15.0V RETURN
-15.0V RETURN
(CL≅1.5A)
-15.0V @ .1A MIN
.2A NOM
.4A PEAK
(100MV P-P)
RESET
80 < d1 < 120μsec
d2 < 5μsec
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS
DATE
DRAWN
CHECKED
11/20/85
SCHEMATIC REV. 52
QS402 POWER SUPPLY
SIZE D
DRAWING NO D9000-0225
DO NOT SCALE DRAWING
SHEET 3

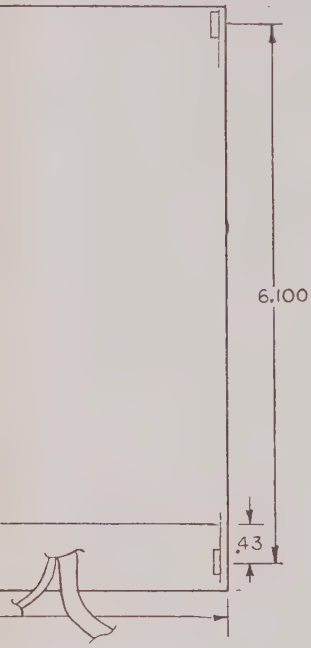

5.00
6-32
PEMNUT
NEARSIDE
2 PL
1
J4
17
15.800

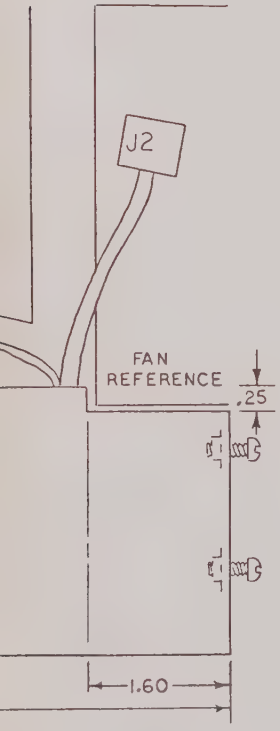

J3
CRT
REFERENCE
DISK DRIVE
REFERENCE
45°
J1
MOUNT
REFERENCE
1.0
16.0

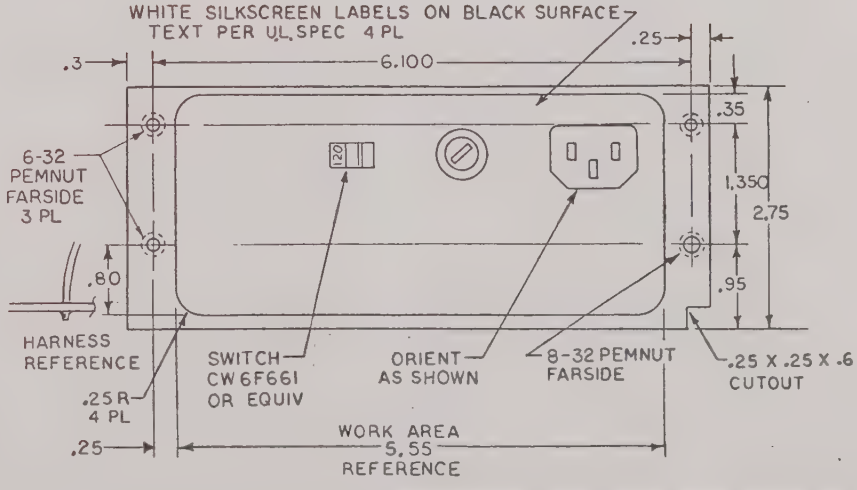
DWG. NO. D9000-0225 | SH 4 | REV 52

REVISIONS

ZONE	REV.	ECO#	DESCRIPTION	DWN	CHKD	APPD







-03	-02	-01	PART NUMBER	DESCRIPTION	ITEM NO.
QTY PER ASSY					

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
= XX = .02 ± 3°
XXX = .010

MATERIAL

FINISH

GOULD PART NO.

APPROVALS	DATE
DRAWN J. Wagner	5-6-86
CHECKED	
PROJ ENG	

GOULD Electronics

TITLE: OUTLINE DWG K450 POWER SUPPLY

DASH NO.	NEXT ASSY	USED ON

FIRST APPLICATION

DO NOT SCALE DRAWING

SIZE D | DWG NO. D9000-0225 | REV 52

SCALE | MODEL | SHEET 4 OF 4

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Reader Comments

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The manual's completeness, accuracy, organization, usability, and reliability _____

_____

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Did you find errors in this manual? _____ How can this manual be improved? _____

_____

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